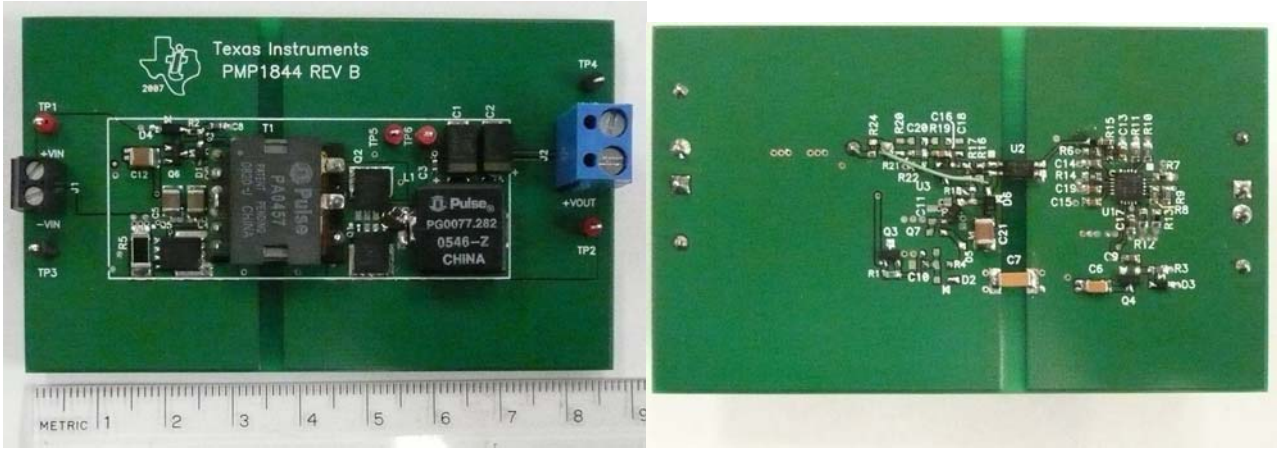
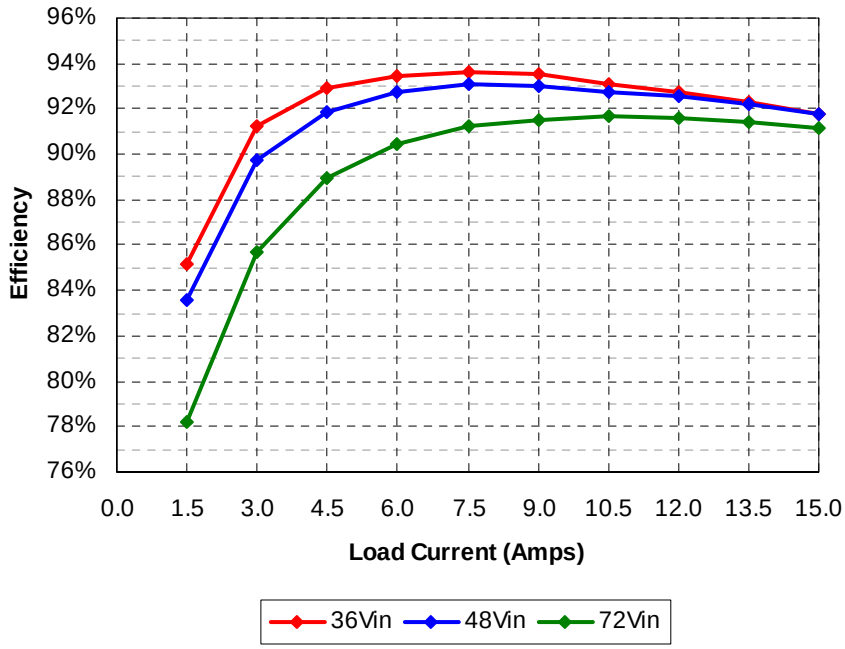
1 Photo

The photographs below show the top and bottom view of the PMP5454 Rev A demo board. This circuit was built using a PMP1844 Rev B circuit board.



2 Efficiency

The efficiency data is shown in the tables and graph below.



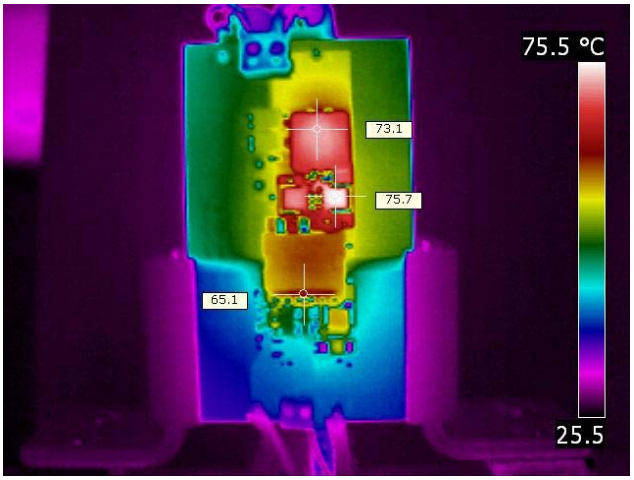
Vin	Iin	Iout	Vout	Pout	Losses	Efficiency
36.0	0.024	0.000	3.285	0.00	0.864	0.0%
36.0	0.161	1.502	3.285	4.93	0.861	85.1%
36.0	0.300	2.998	3.285	9.85	0.950	91.2%
36.0	0.442	4.50	3.285	14.78	1.128	92.9%
36.0	0.586	6.00	3.285	19.71	1.383	93.4%
36.0	0.731	7.50	3.285	24.64	1.675	93.6%
36.0	0.879	9.01	3.285	29.60	2.046	93.5%
36.0	1.030	10.50	3.286	34.50	2.572	93.1%
36.0	1.181	12.00	3.286	39.43	3.078	92.8%
36.0	1.335	13.50	3.286	44.36	3.692	92.3%
36.0	1.492	15.00	3.286	49.29	4.422	91.8%

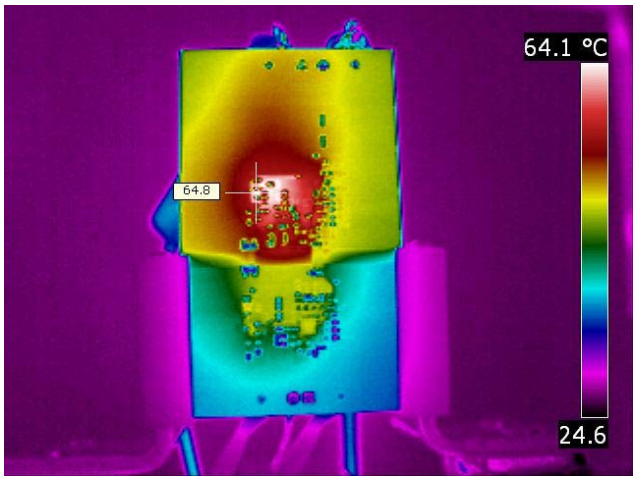
Vin	Iin	Iout	Vout	Pout	Losses	Efficiency
48.0	0.020	0.000	3.290	0.00	0.960	0.0%
48.0	0.123	1.500	3.289	4.93	0.970	83.6%
48.0	0.229	3.001	3.288	9.87	1.123	89.8%
48.0	0.335	4.49	3.288	14.76	1.315	91.8%
48.0	0.443	6.00	3.287	19.72	1.539	92.8%
48.0	0.552	7.50	3.287	24.65	1.840	93.1%
48.0	0.663	9.00	3.287	29.58	2.236	93.0%
48.0	0.775	10.50	3.286	34.50	2.691	92.8%
48.0	0.888	12.00	3.286	39.43	3.185	92.5%
48.0	1.003	13.51	3.286	44.39	3.742	92.2%
48.0	1.119	15.00	3.286	49.29	4.413	91.8%

Vin	Iin	Iout	Vout	Pout	Losses	Efficiency
72.0	0.018	0.000	3.290	0.00	1.296	0.0%
72.0	0.088	1.506	3.289	4.95	1.383	78.2%
72.0	0.160	3.001	3.289	9.87	1.650	85.7%
72.0	0.231	4.50	3.288	14.80	1.836	89.0%
72.0	0.303	6.00	3.288	19.73	2.088	90.4%
72.0	0.376	7.51	3.288	24.69	2.379	91.2%
72.0	0.449	9.00	3.287	29.58	2.745	91.5%
72.0	0.523	10.50	3.287	34.51	3.143	91.7%
72.0	0.598	12.00	3.287	39.44	3.612	91.6%
72.0	0.674	13.50	3.287	44.37	4.154	91.4%
72.0	0.752	15.01	3.287	49.34	4.806	91.1%

3 Thermal Images

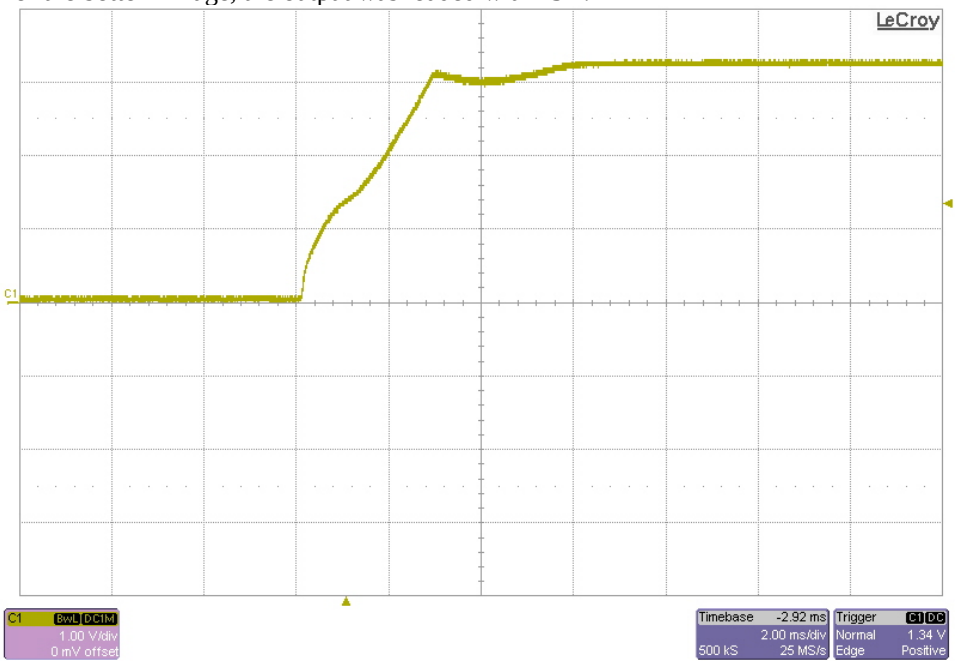
The thermal images below show a top view (left) and bottom view (right) of the board. The ambient temperature was 26ºC with no forced air flow. The input was 48VDC, and the output was loaded with 15A.

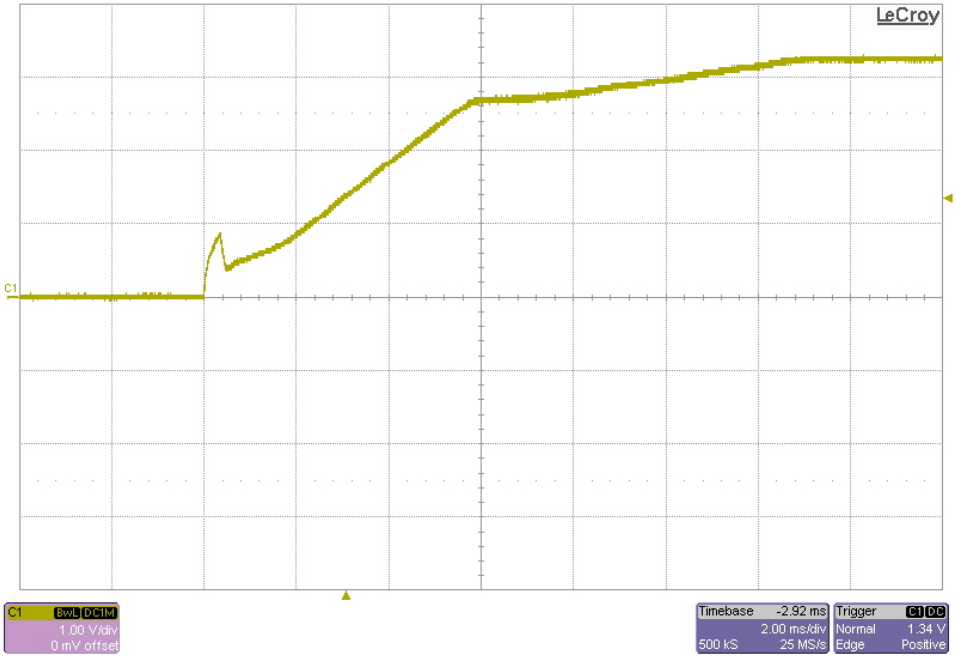




4 Startup

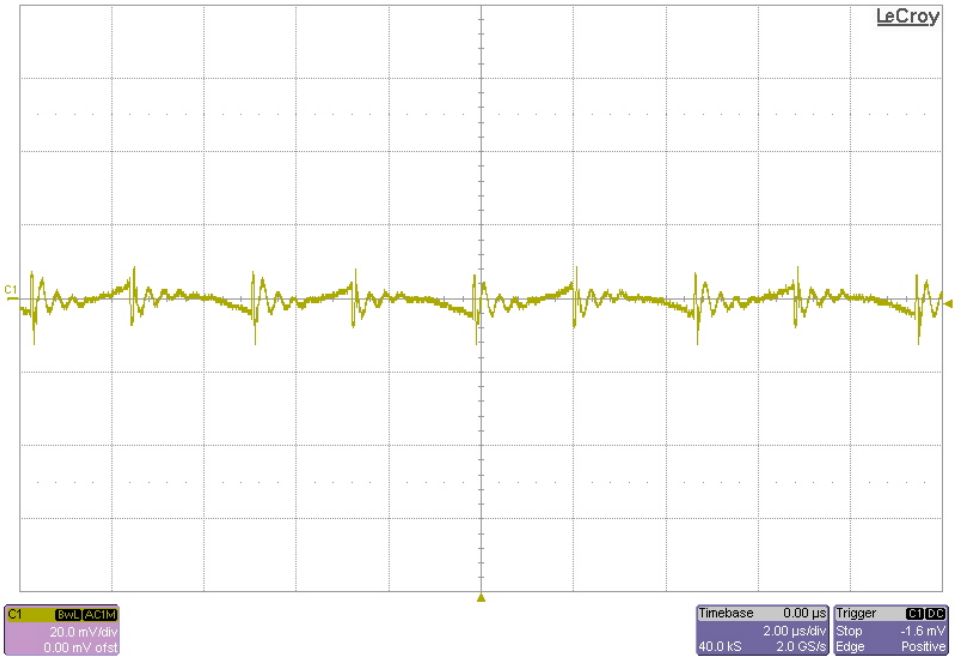
The output voltage at startup is shown in the images below. The input was set to 48V. For the top image, the output was unloaded. For the bottom image, the output was loaded with 15A.





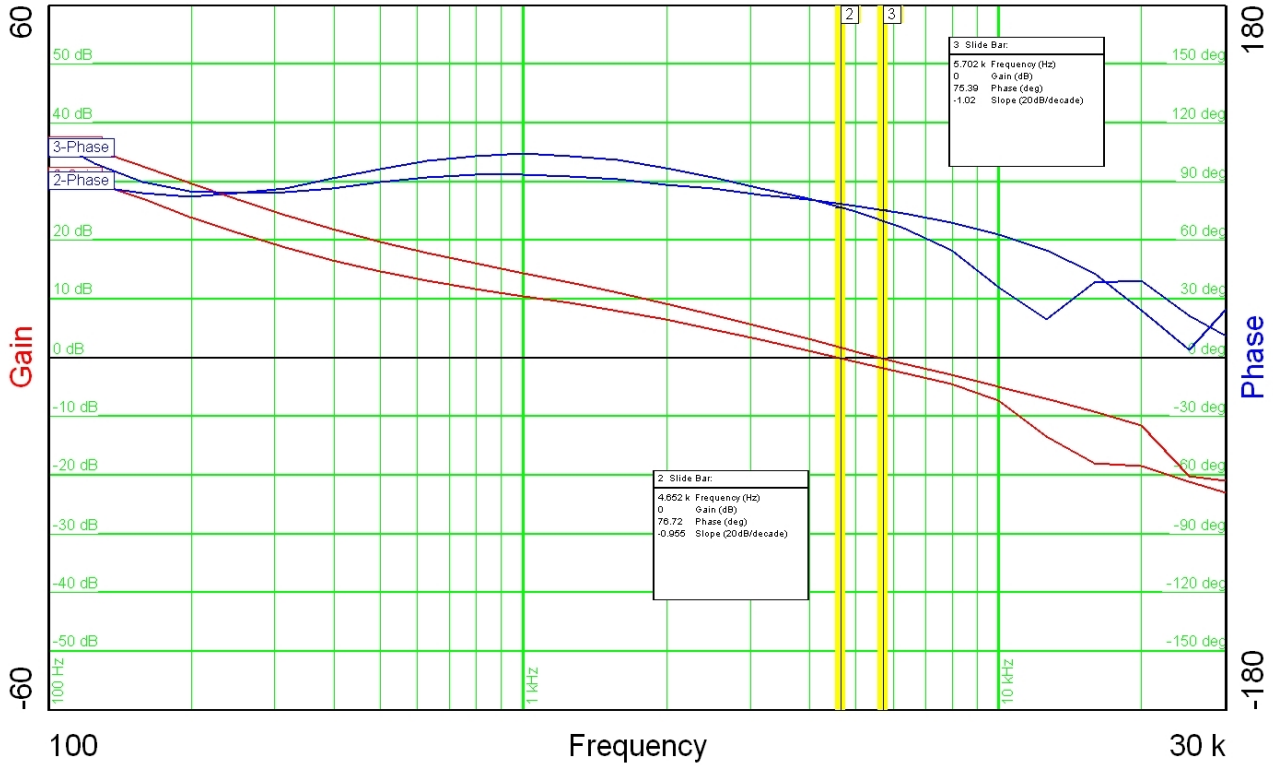
5 Output Ripple Voltage

The output ripple voltage during full load operation (15A load) is shown in the plot below. The input voltage was set to 48VDC.



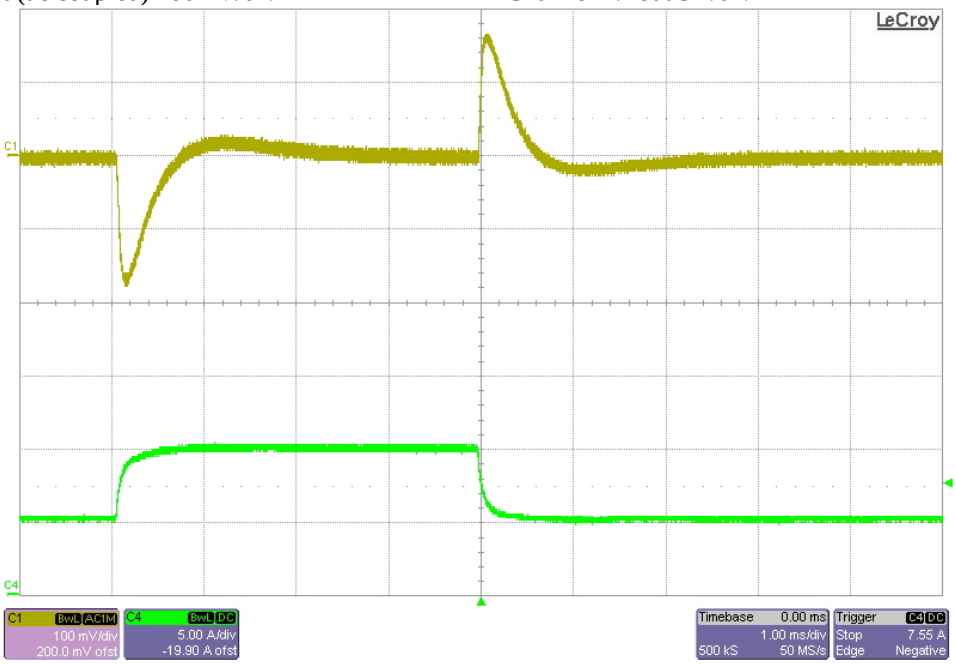
6 Loop Response

The image below shows the loop response of the converter. For the upper gain/phase plot, the input was 72Vdc. For the lower gain/phase plot, the input was 36Vdc. The output was loaded with 15A.



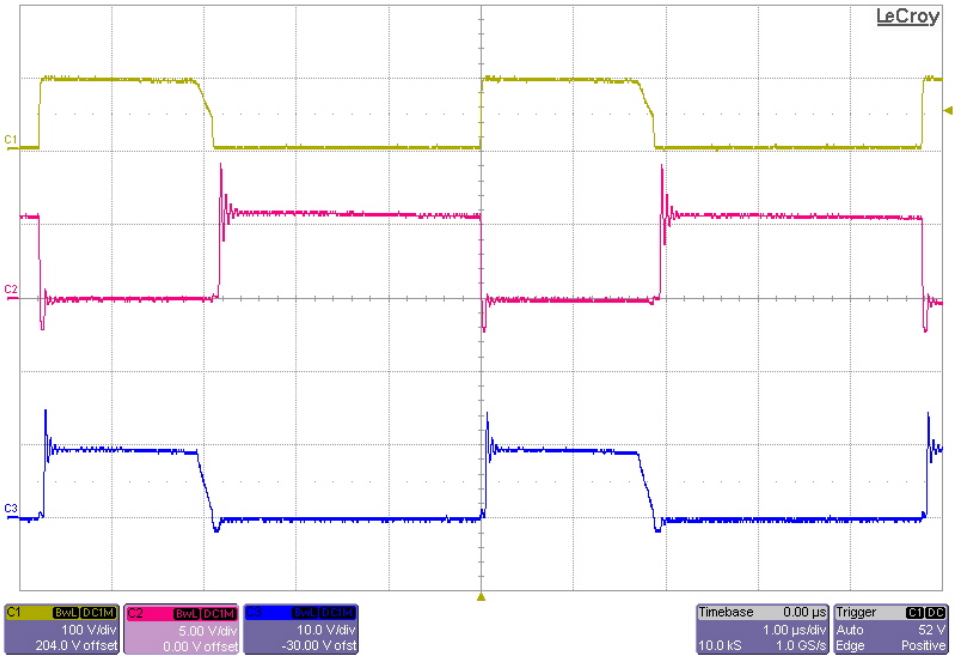
7 Load Transients

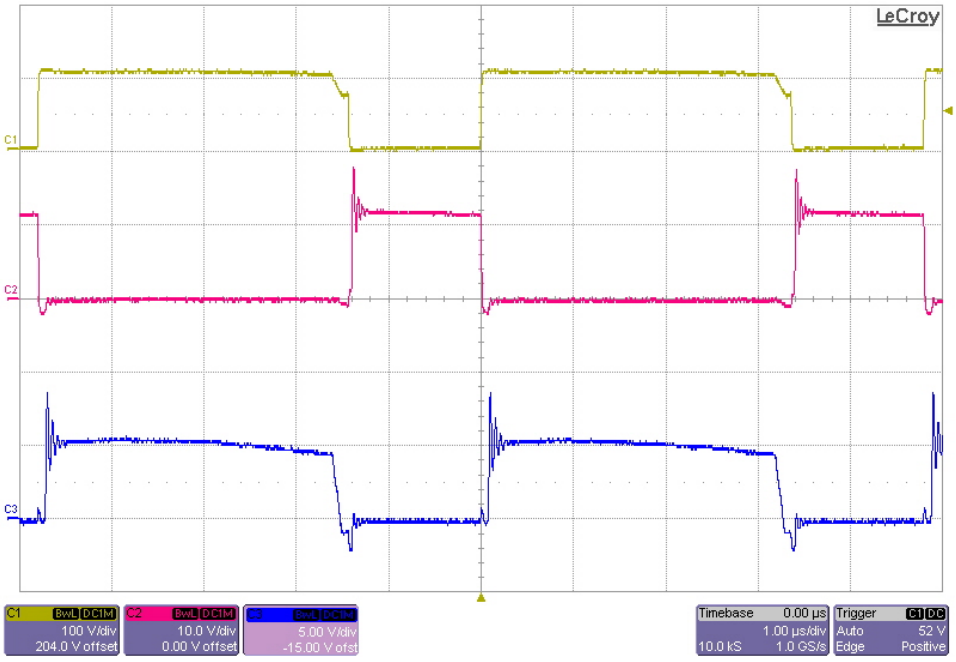
The image below shows the response to a 5A to 10A load transient. The input voltage was set to 48VDC.
Channel 1: Vout (ac coupled) 100mV/div Channel 4: Iout 5A/div



8 Switching Waveforms

The images below show the drain-to-source voltage waveforms on the switching MOSFETs. The output was loaded with 15A. For the top image, the input was set to 36V. For the bottom image, the input was set to 72V.
Channel 1: Q5 Vds Channel 2: Q1 Vds
Channel 3: Q2 Vds




LeCroy
C1
C2
C3
C1 BwL DC1M
100 V/div
204.0 V offset
C2 BwL DC1M
10.0 V/div
0.00 V offset
C3 BwL DC1M
5.00 V/div
-15.00 V ofst
Timebase 0.00 µs
1.00 µs/div
10.0 kS 1.0 GS/s
Trigger C1 DC
Auto 52 V
Edge Positive

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