1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 12.0V, with no load on the 1.2V output.

Channel C1: **input voltage**
2V/div, 2ms/div

Channel C2: **output voltage**
500mV/div, 2ms/div

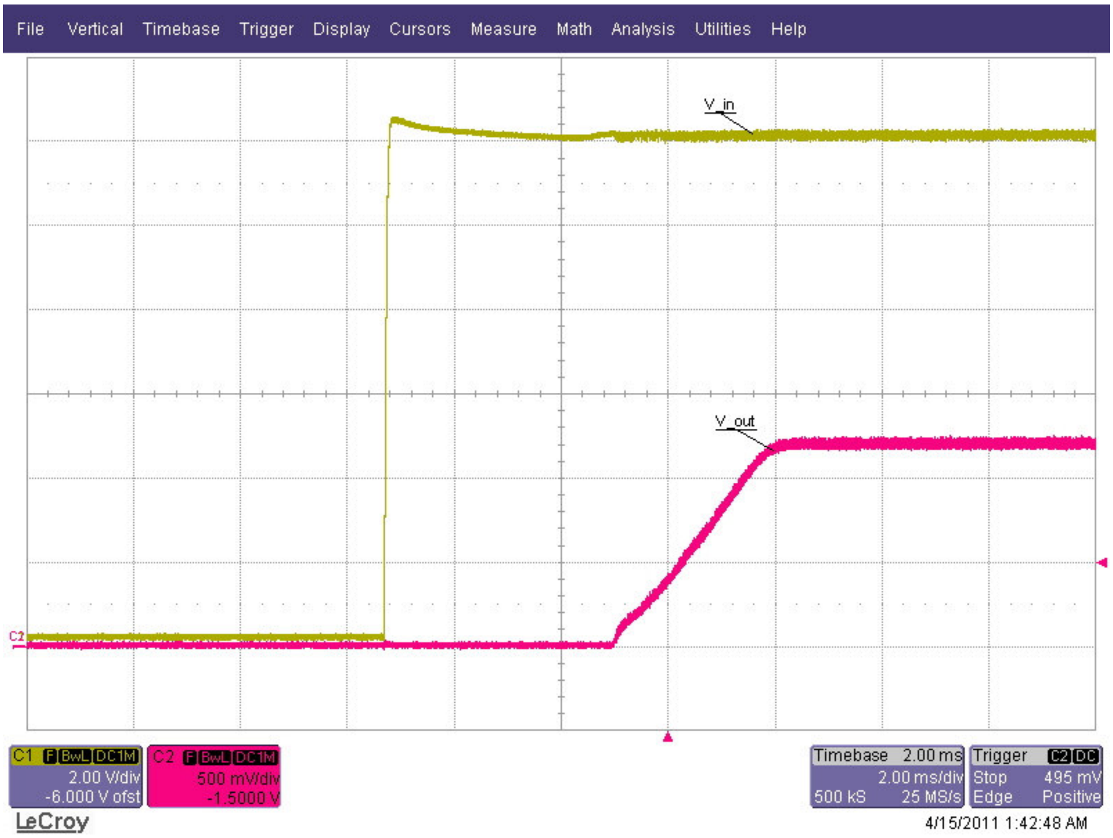


Figure 1

2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage is set at 12.0V with a 20.0A load on the 1.2V output.

Channel C1: **input voltage**
2V/div, 500us/div

Channel C2: **output voltage**
500mV/div, 500us/div

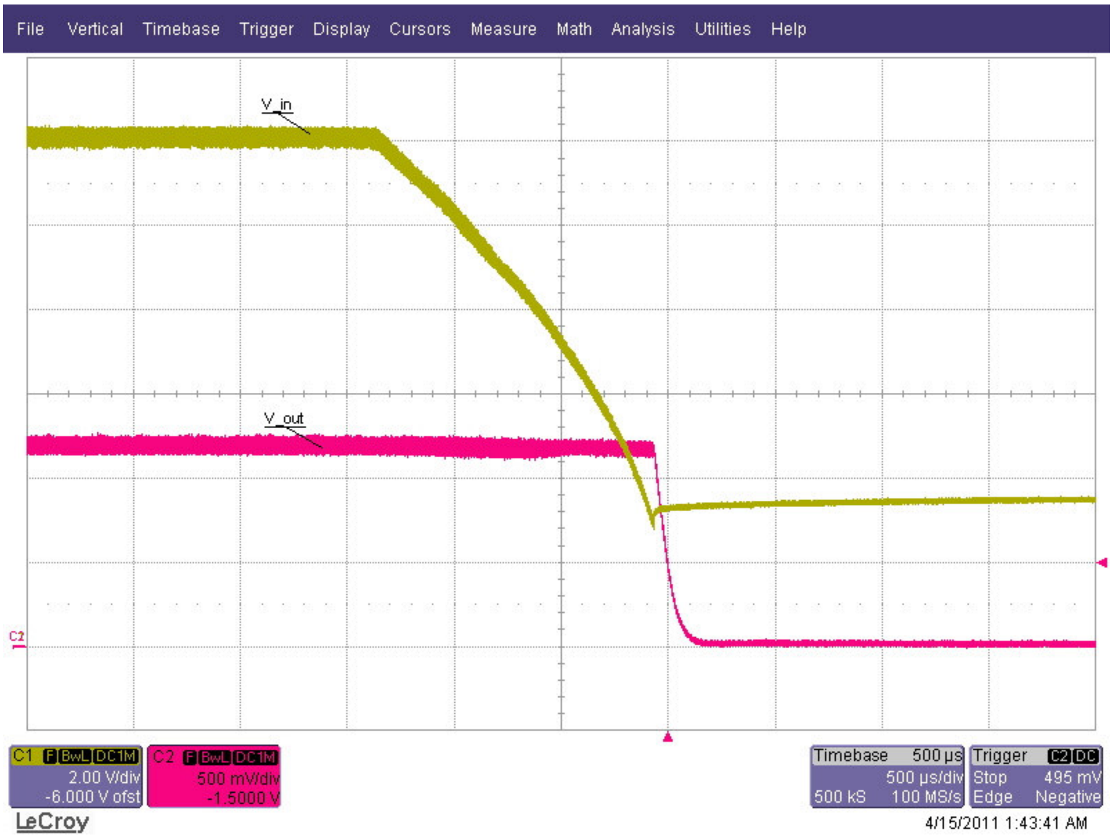


Figure 2

3 Efficiency

The efficiency is shown in Figure 3.

The measurements were done with two different inductors:

• **SER2009-601ML**	0.740mOhm max.	41A rms	49A sat
• **SER1408-501ME**	0.55mOhm max.	38A rms	30A sat

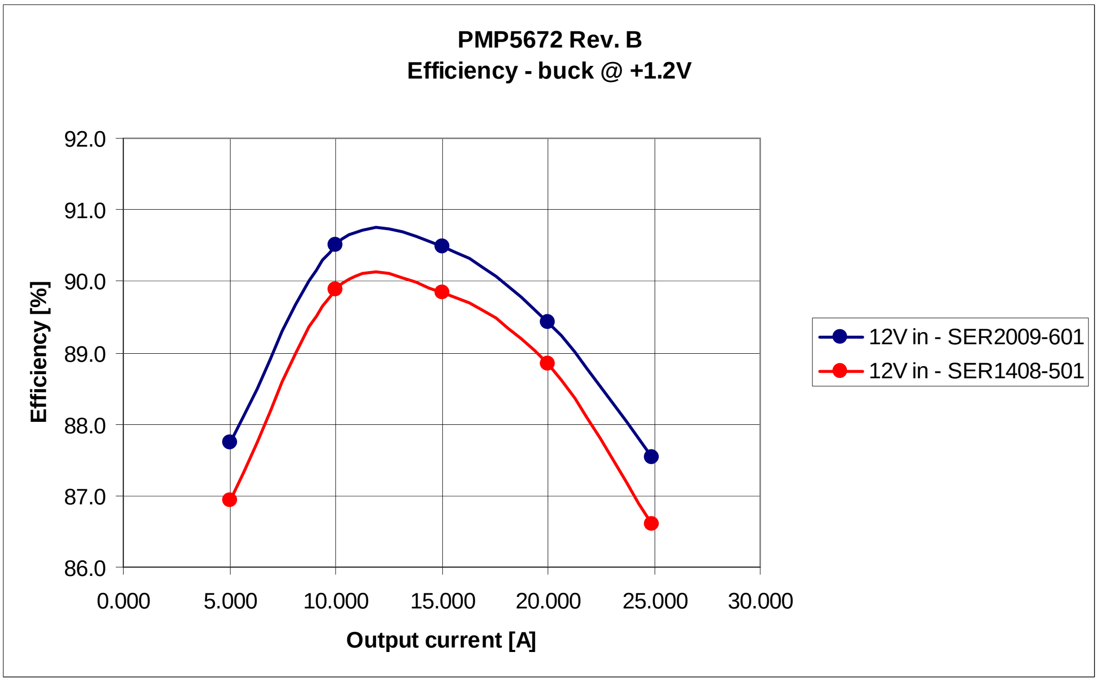


Figure 3

4 Load regulation

The load regulation of the 1.2V output is shown in Figure 4.

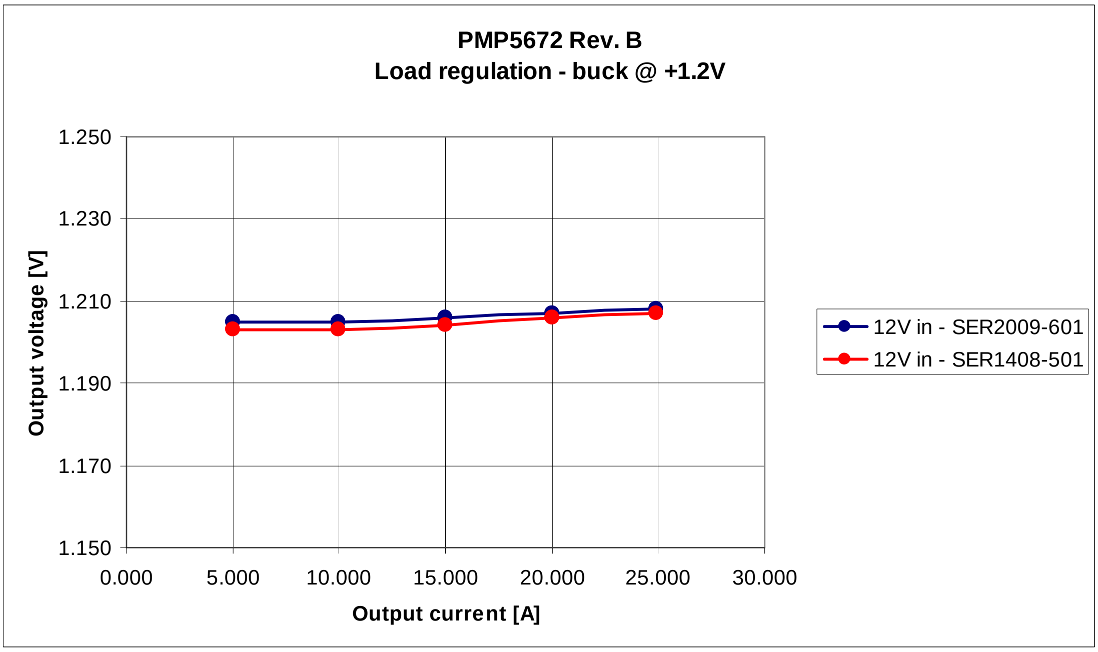


Figure 4

5 Output ripple voltage

The output ripple voltage at 20.0A load and 12.0V input voltage is shown in Figure 5.

Channel C1: **switching node**
10V/div, 1us/div

Channel C2: **output voltage**
20mV/div, 1us/div, AC coupled

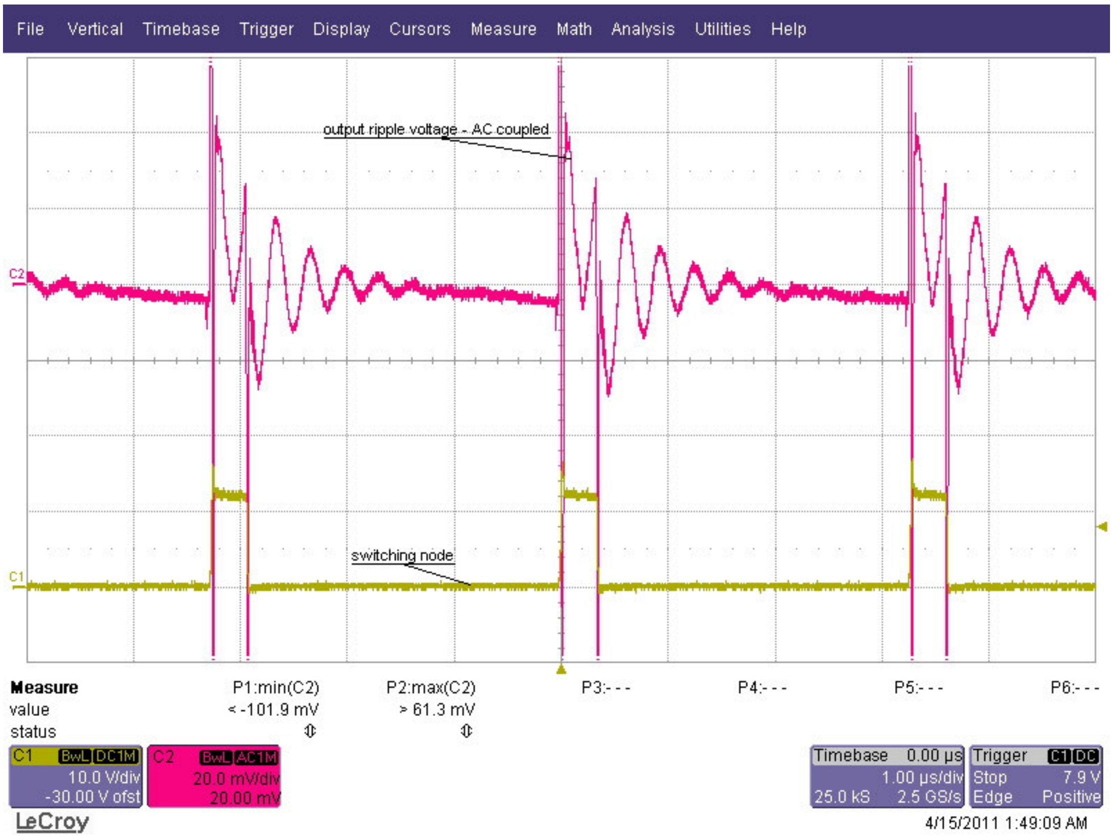


Figure 5

Due to high noise from the switching node and the low ESR of the output capacitors it is very difficult to measure the exact output ripple.
The output ripple is approximately 5mV peak-peak.

6 Load transients

The response to a load step and a load dump at an input voltage of 12.0V is shown in Figure 6 and Figure 7.

Channel C2: **output voltage**, -15mV undershoot
20mV/div, 50us/div, AC coupled

Channel C1: **load current**, load step 10.0A to 20.0A
10A/div, 50us/div

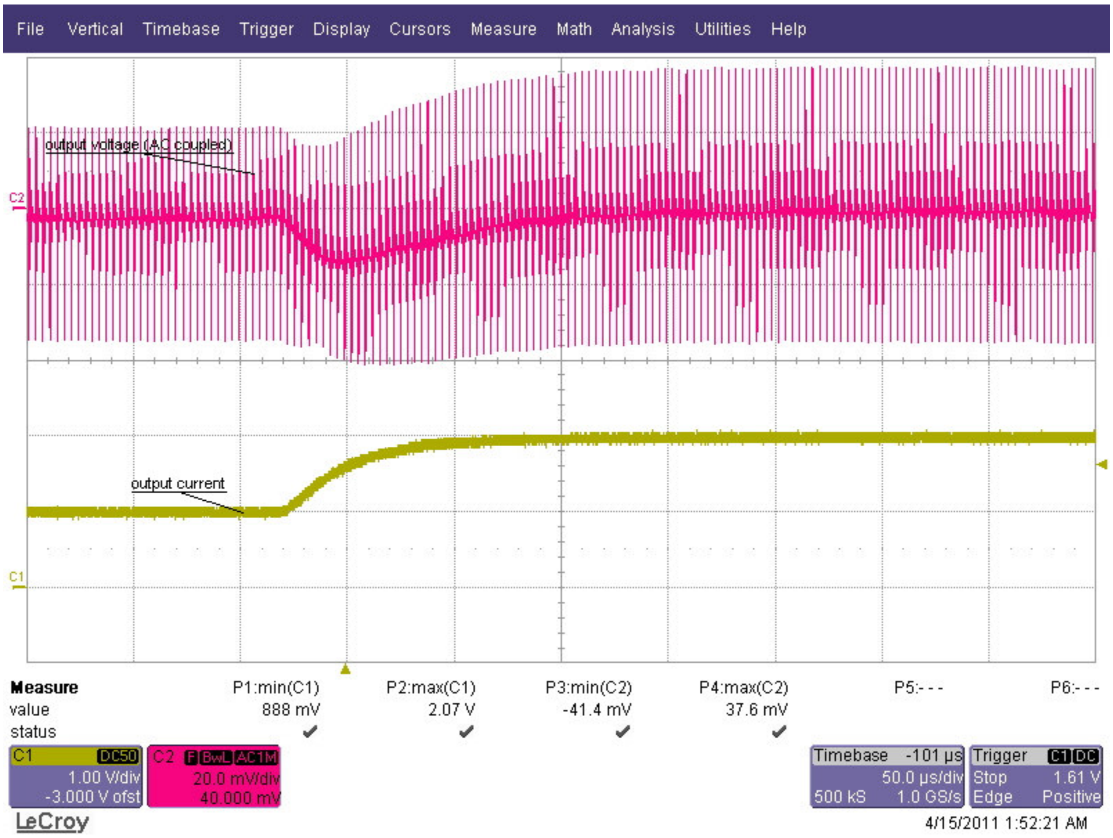


Figure 6

Channel C2: **output voltage**, 10mV overshoot
20mV/div, 50us/div, AC coupled

Channel C1: **load current**, load dump 20.0A to 10.0A
10A/div, 50us/div

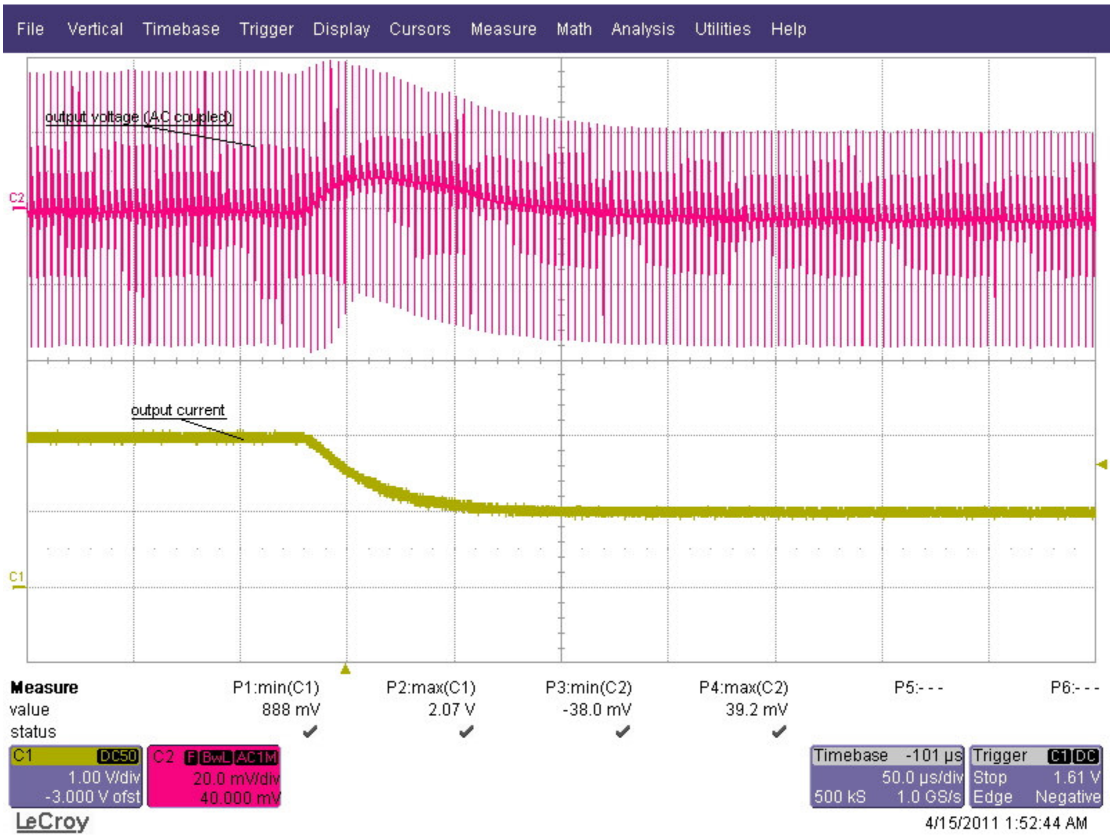


Figure 7

7 Frequency response

Figure 8 shows the loop response of the 1.2V output with 12.0V input and a 20.0A load.

67 deg phase margin @ crossover frequency 27.0 kHz

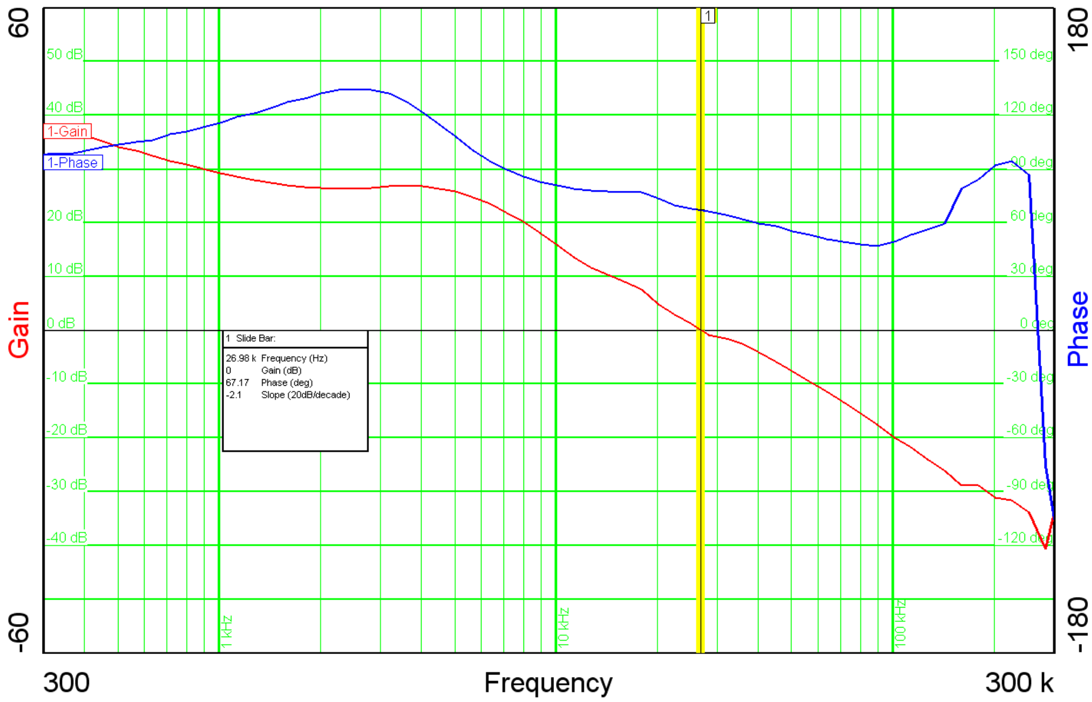


Figure 8

8 Miscellaneous waveforms

The drain-source voltage on the switching node is shown in Figure 9. The image was captured with a 12.0V input and a 25.0A load.

Channel C2: **drain-source voltage**, -1.2V minimum voltage, 26.5V maximum voltage
5V/div, 50ns/div

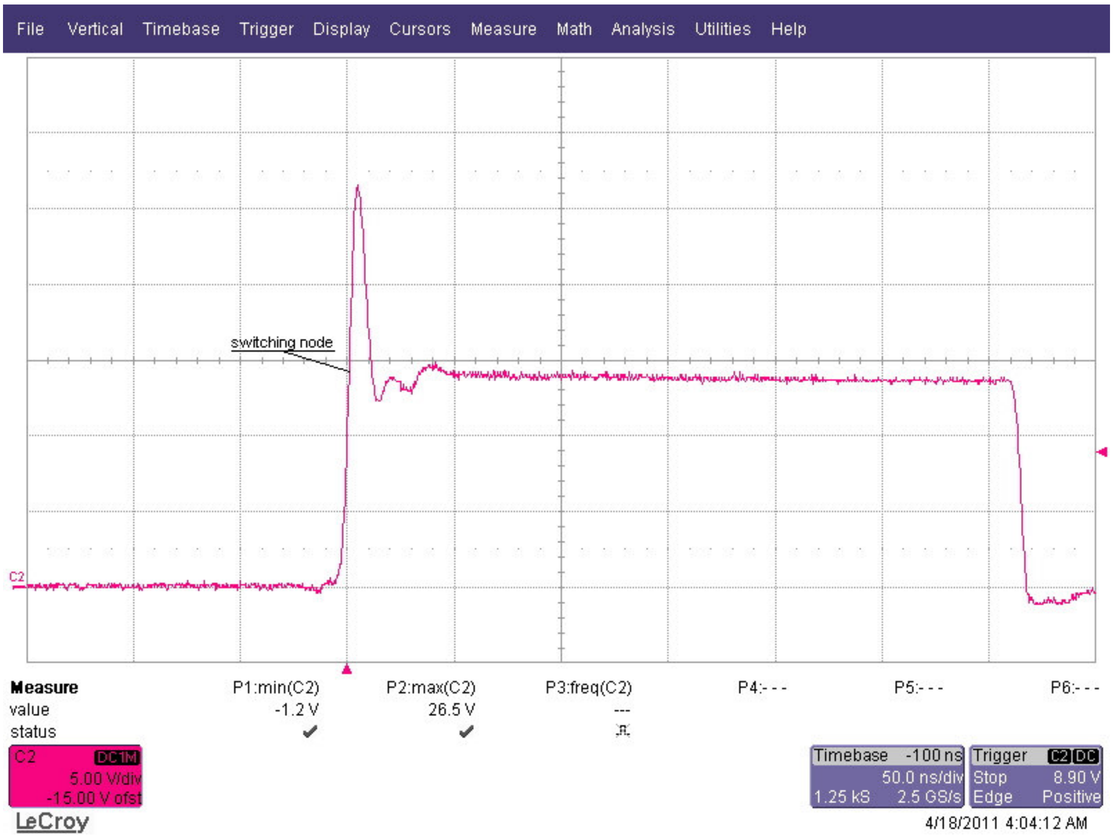
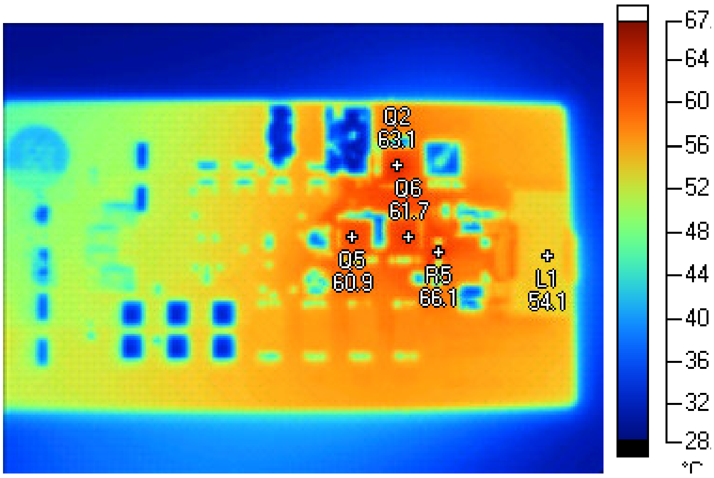


Figure 9

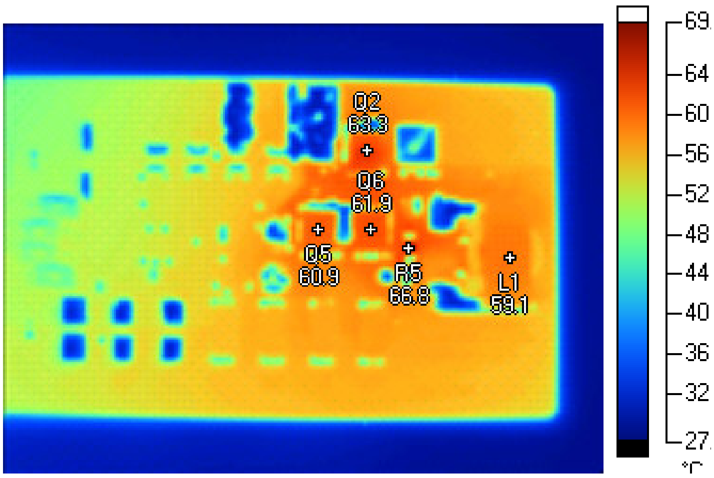
9 Thermal measurement

Figure 10 shows the circuit at an ambient temperature of 21 °C with an input voltage of 12.0V and a load of 20.0A.
The measurement was done with two different inductors.



SER2009-601M

Label	Temperature	Emissivity	Background
L1	54.1 °C	0.95	21.0 °C
R5	66.1 °C	0.95	21.0 °C
Q2	63.1 °C	0.95	21.0 °C
Q6	61.7 °C	0.95	21.0 °C
Q5	60.9 °C	0.95	21.0 °C



SER1408-501ME

Label	Temperature	Emissivity	Background
L1	59.1 °C	0.95	21.0 °C
R5	66.8 °C	0.95	21.0 °C
Q6	61.9 °C	0.95	21.0 °C
Q5	60.9 °C	0.95	21.0 °C
Q2	63.3 °C	0.95	21.0 °C

Figure 10

10 Additional measurements & analysis

10.1 Low side schottky diode

Often an additional schottky diode is placed in parallel to the low side MOSFET to reduce the overshoot (diode is conducting when high side FET was switched off and the low side FET is not yet conducting).
Figure 11 shows clearly that an additional diode has no influence. The drain-source voltage of the low side FET is exactly the same.
Due to adaptive gate drive the dead-time is already optimized by the controller.

C2: Schottky diode MBRS340A placed
M2: no diode placed

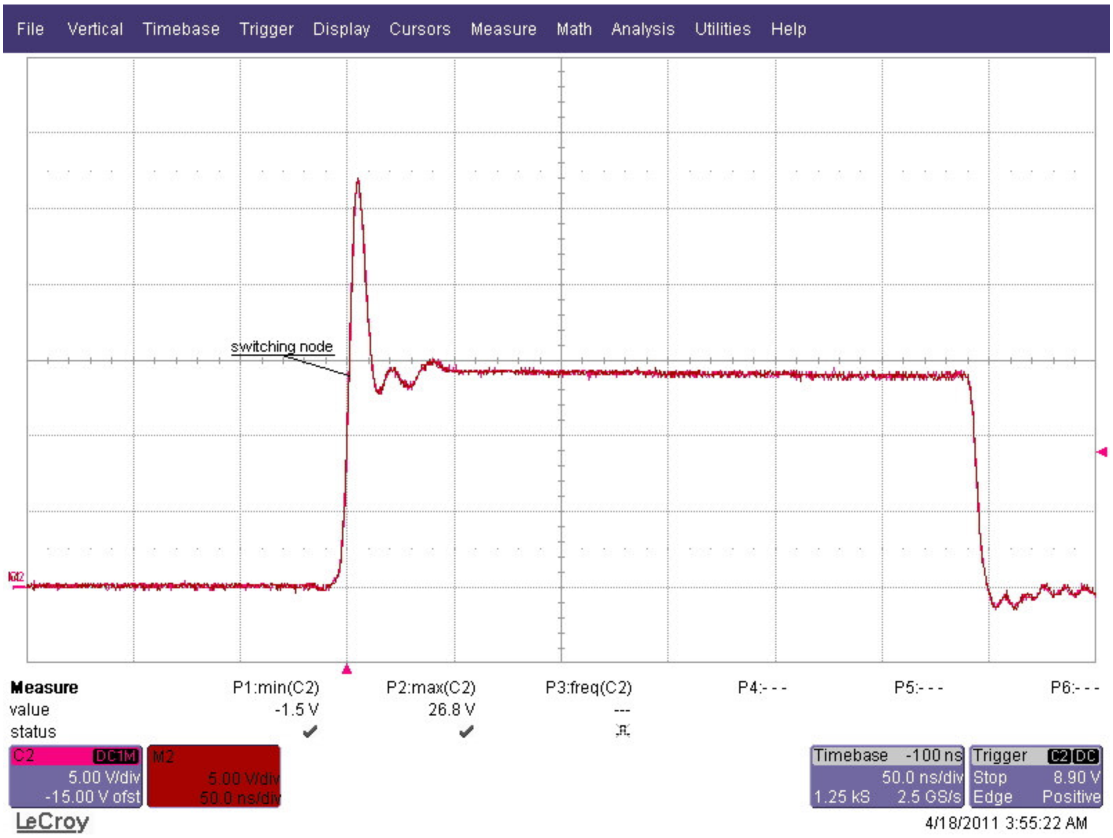


Figure 11

10.2 Voltage on switching node and on pin SW

The maximum voltage on pin SW is 27V. To reduce this voltage either a resistor can be placed between pin SW and the switching node or the overshoot on the switching node has to be reduced (snubber, gate resistors e.g.).
Already the inductance of the trace between the switching node and pin SW reduces the voltage on pin SW of the controller as Figure 12 shows.
The voltage can be reduced either by placing a resistor between pin SW and the switching node. In this configuration no resistor is necessary.

Peak voltage on switching node: 26.5V
Peak voltage on pin SW: 24.4V (no resistor between switching node and pin SW)

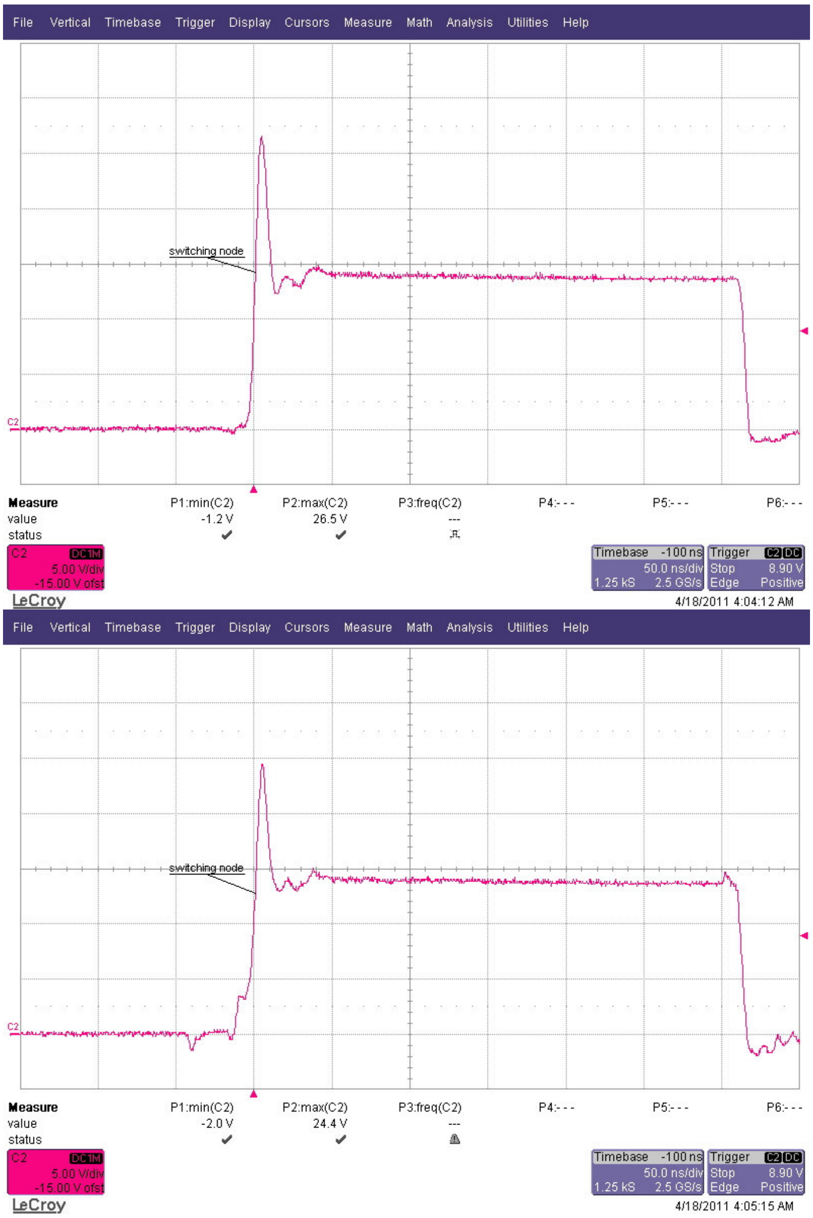
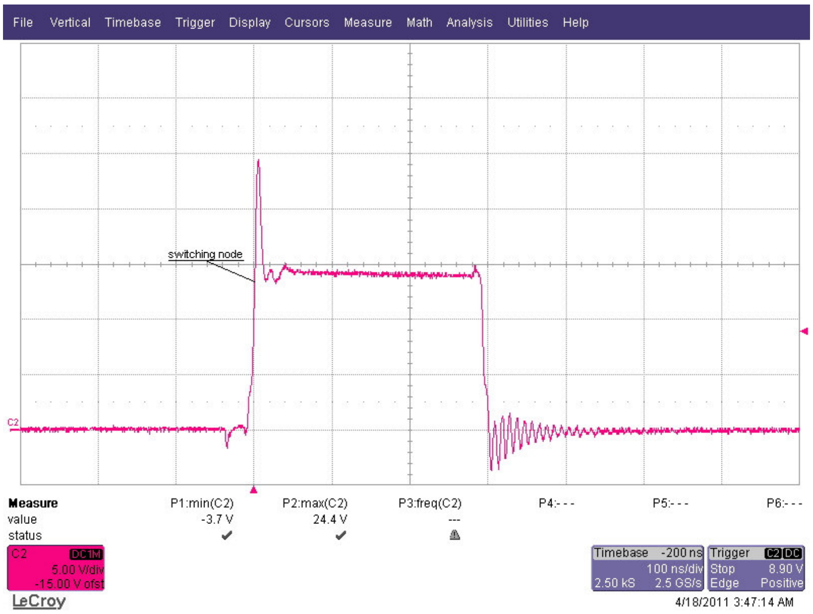


Figure 12

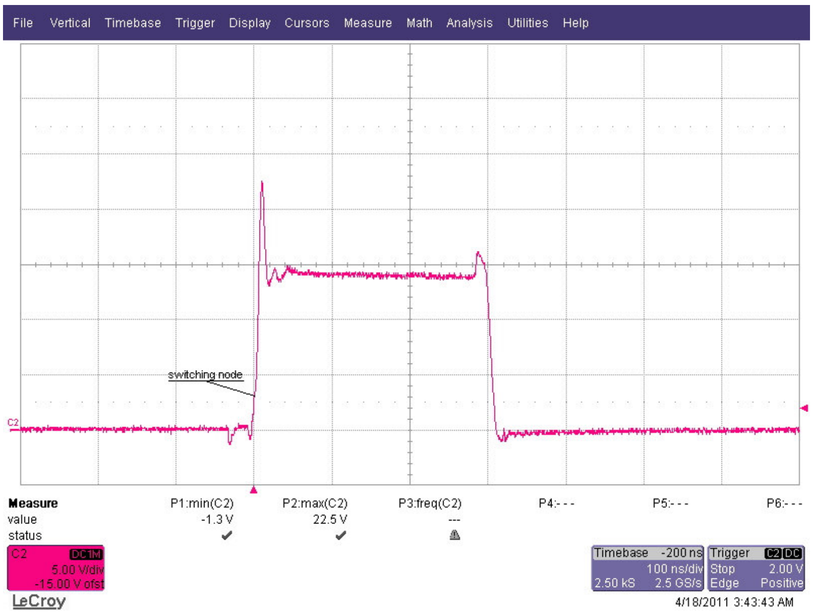
The pictures below show the influence of a resistor between the switching node and pin SW on the maximum voltage.

No resistor placed: 24.4V peak
3.3R placed: 22.5V peak

Care has to be taken if this resistor is placed inside or outside the bootstrap circuit of the high side FET! If it is located inside the bootstrap circuit it has also an influence on the switching behavior of the high side FET.



Pin SW connected directly to switching node



Pin SW connected to switching node via 3.3R

10.3 Gate resistors

To reduce the overshoot on the switching node resistors can be placed in the gate lines. This reduces the switching frequency and thus the overshoot.

The measurements show that too high gate resistors lead to problems. If they are too high, the adaptive gate drive doesn't work properly which leads to cross conduction.

8.0V input voltage, 1.2V @ 10.0A load

R1 - high side	R8 - low side	Vpeak - sw. node	Input current
0.0R	0.0R	17.2V	1.648A
1.0R	1.0R	15.5V	1.643A
2.2R	2.2R	15.2V	1.655A
3.3R	3.3R	15.3V	1.736A

A 1.0R resistor shows the best balance between peak voltage and input current.
If the resistors are too high, the input current is increasing (cross conduction) and the converter doesn't start up sometimes due to overcurrent.

10.4 Snubber circuit

A snubber placed in parallel to the low side FET reduces the overshoot. The influence is depending on the resistance and the capacitance.

The measurements were done at 8.0V input voltage and 1.2V output voltage with no load.

R5 - snubber	C29 - snubber	Vpeak - sw. node	Input current
open	open	14.5V	33mA
2.2R	3.3nF	13.9V	38mA
1.0R	3.3nF	13.6V	37mA
1.0R	10nF	12.4V	52mA
1.0R	4.7nF	13.0V	41mA

The resistor has to be pretty low to achieve a significant influence.
By varying the capacitance the overshoot is reduced. It has to be taken care to burn not too much energy in the resistor!

10.5 Conclusion

- An additional schottky diode parallel to the low side FET has no influence and is thus unnecessary.
- A resistor between the switching node and pin SW reduces effective the voltage on pin SW if the switching node voltage is close to the maximum of 27V.
- Gate resistors can be used to reduce the overshoot. But too high values lead to cross conduction. A good value is 1.0R for NexFETs but it depends highly on the gate charge.
- Also a snubber circuit reduces the overshoot. The resistor has to be pretty low, around 1.0R. The capacitors depends on the overshoot (1..10nF)

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