

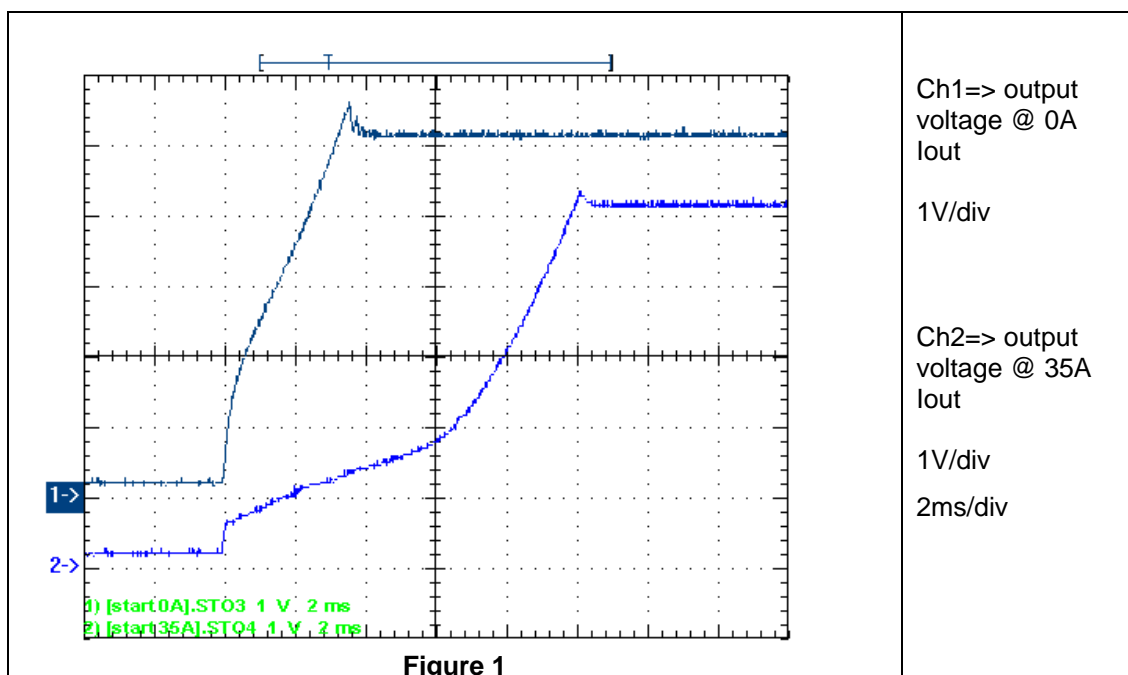
PMP5711RevC Test Results

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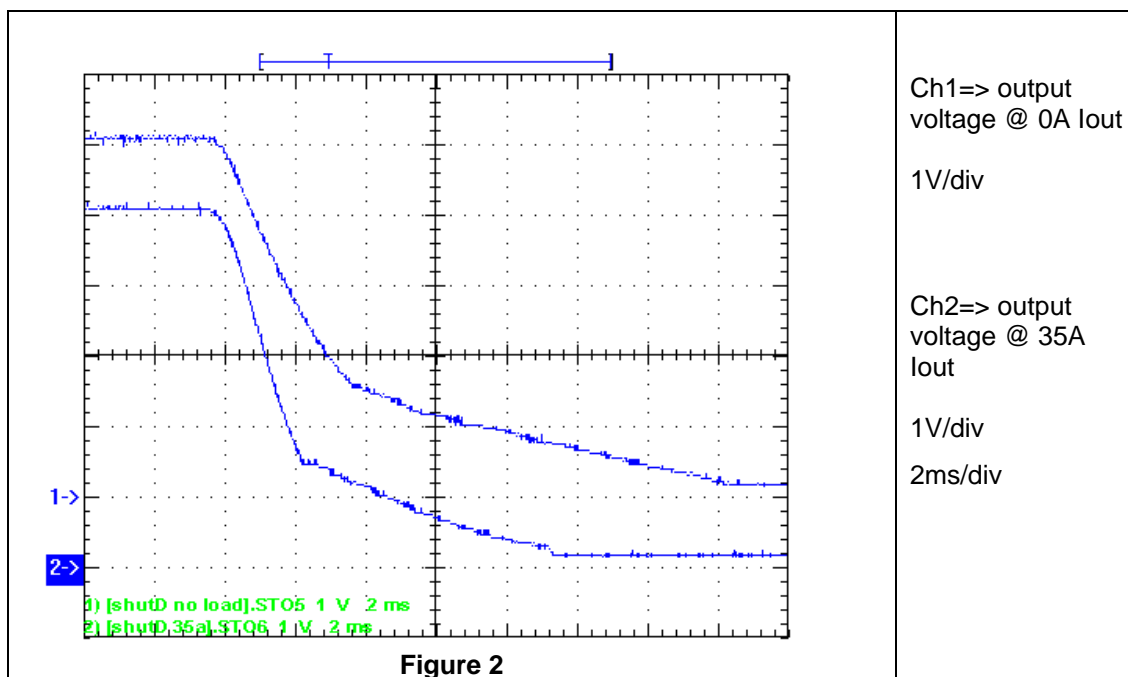
1 Startup

The startup waveform is shown in Figure 1. The input voltage was set to 48V, with 0A and 35A load current at the output. Startup at full load 35Amps needs 10ms.



2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage was set at 48V, with 0A, and 35A load on the output.



3 Efficiency

The efficiency is shown in Figure 3 below, evaluated at V_{min} 36V, V_{nom} 48V and V_{max} 72V; Both voltages are measured directly at input/output capacitors:

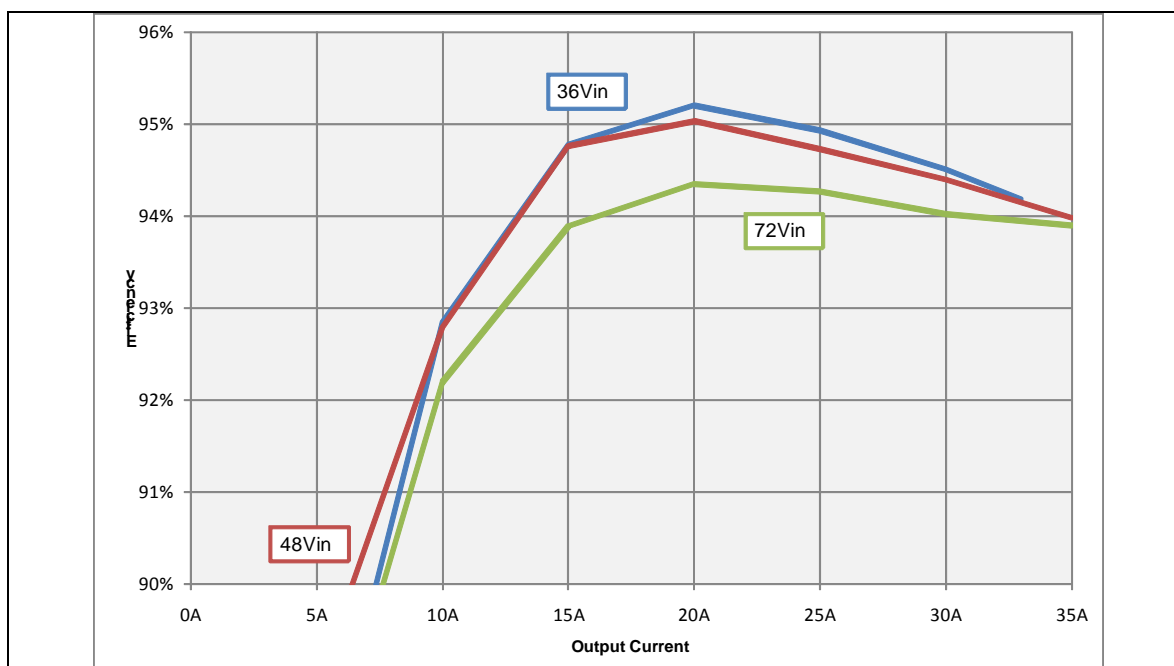


Figure 3

Table 1, V_{min} 36V:

| VOUT | IOUT | VIN | IIN | POUT | PIN | Eff |
|------|-------|-------|------|-------|-------|--------------|
| 5.00 | 5.04 | 36.25 | 0.80 | 25.2 | 28.8 | 87.5% |
| 5.01 | 10.01 | 36.24 | 1.49 | 50.1 | 54.0 | 92.8% |
| 5.01 | 15.02 | 36.22 | 2.19 | 75.2 | 79.4 | 94.8% |
| 5.01 | 20.03 | 36.21 | 2.91 | 100.4 | 105.4 | 95.2% |
| 5.01 | 25.00 | 36.19 | 3.65 | 125.3 | 131.9 | 94.9% |
| 5.01 | 30.01 | 36.18 | 4.40 | 150.4 | 159.2 | 94.5% |
| 5.01 | 32.99 | 36.17 | 4.86 | 165.4 | 175.6 | 94.2% |

Table 2, V_{nom} 48V:

| VOUT | IOUT | VIN | IIN | POUT | PIN | Eff |
|------|-------|-------|------|-------|-------|--------------|
| 5.00 | 5.04 | 48.48 | 0.59 | 25.2 | 28.4 | 88.9% |
| 5.01 | 10.01 | 48.47 | 1.11 | 50.1 | 54.0 | 92.8% |
| 5.01 | 15.02 | 48.46 | 1.64 | 75.2 | 79.4 | 94.8% |
| 5.01 | 20.03 | 48.45 | 2.18 | 100.4 | 105.6 | 95.0% |
| 5.01 | 25.00 | 48.44 | 2.73 | 125.3 | 132.2 | 94.7% |
| 5.01 | 30.01 | 48.43 | 3.29 | 150.4 | 159.4 | 94.4% |
| 5.02 | 35.02 | 48.42 | 3.86 | 175.7 | 186.9 | 94.0% |

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Table 3, Vmax 72V:

| VOUT | IOUT | VIN | IIN | POUT | PIN | Eff |
|------|-------|-------|------|-------|-------|--------------|
| 5.00 | 5.04 | 71.80 | 0.40 | 25.2 | 28.8 | 87.6% |
| 5.01 | 10.01 | 71.79 | 0.76 | 50.1 | 54.3 | 92.2% |
| 5.01 | 15.02 | 71.78 | 1.12 | 75.2 | 80.1 | 93.9% |
| 5.01 | 20.03 | 71.77 | 1.48 | 100.4 | 106.4 | 94.3% |
| 5.01 | 25.00 | 71.77 | 1.85 | 125.2 | 132.8 | 94.3% |
| 5.01 | 30.01 | 71.76 | 2.23 | 150.4 | 160.0 | 94.0% |
| 5.01 | 35.00 | 71.57 | 2.61 | 175.5 | 186.9 | 93.9% |

4 Load Regulation

The load regulation of the output is shown in the **Figure 4** below, precision is +14mV, so 0.28%.

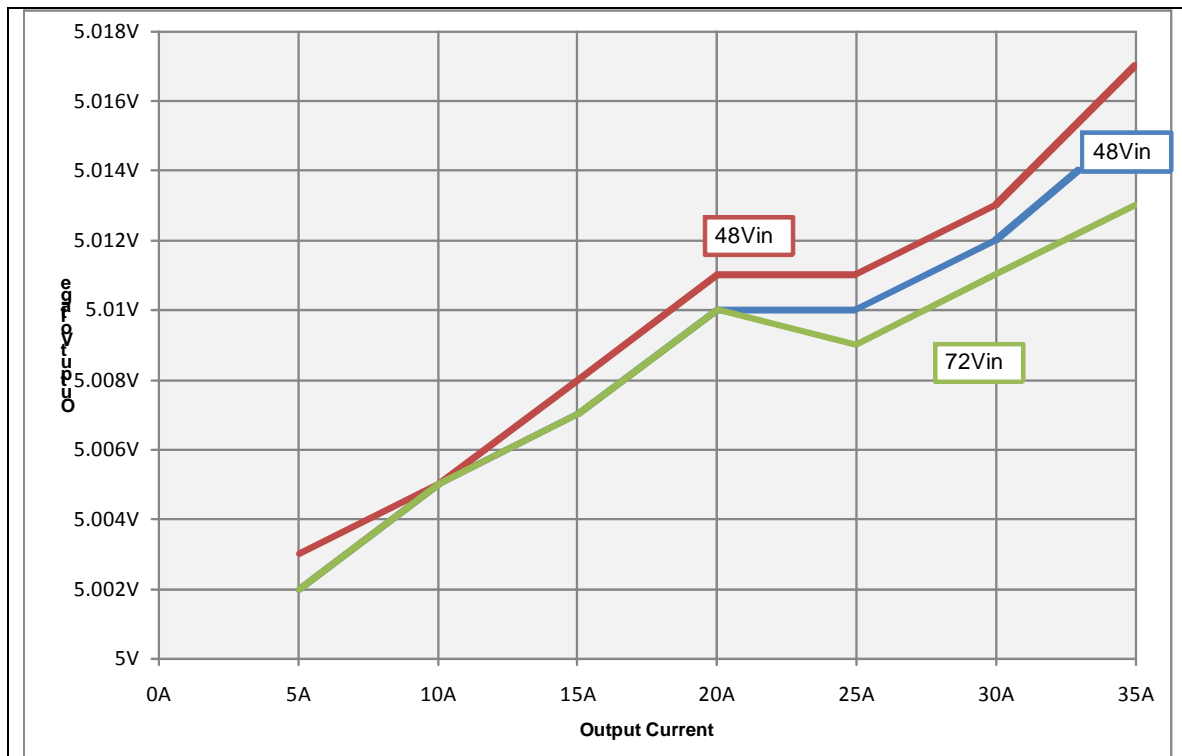


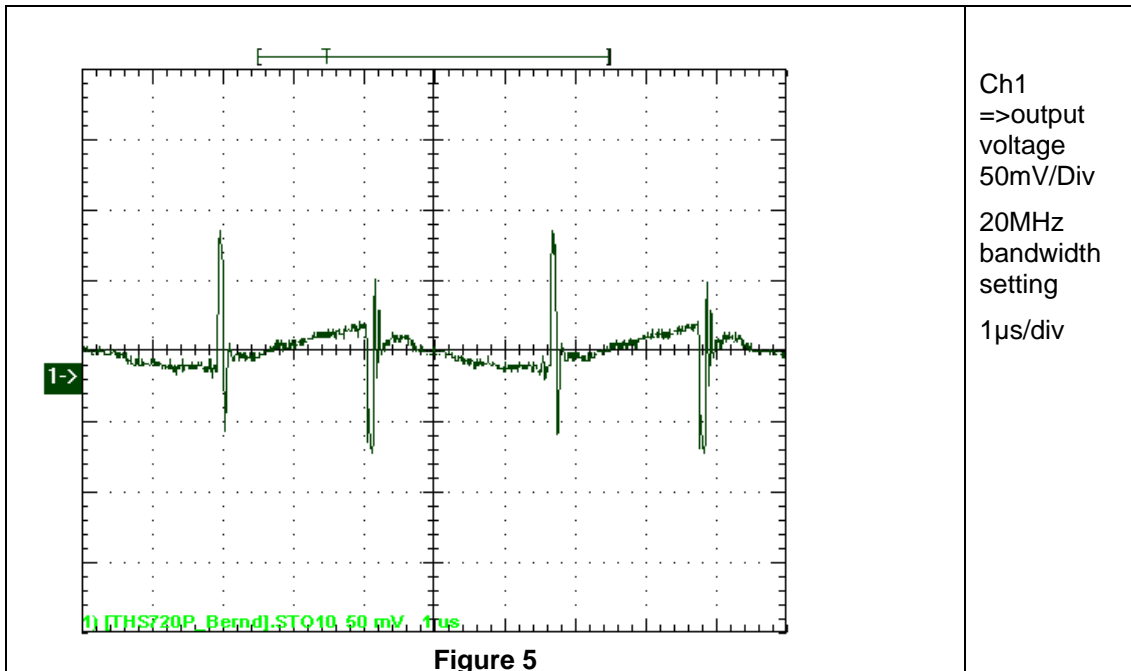
Figure 4

5 Line Regulation

No influence of the output voltage to the input voltage (36V to 72V). The current was set to 20A, voltage stayed constant at 5.011V by covering total input voltage range.

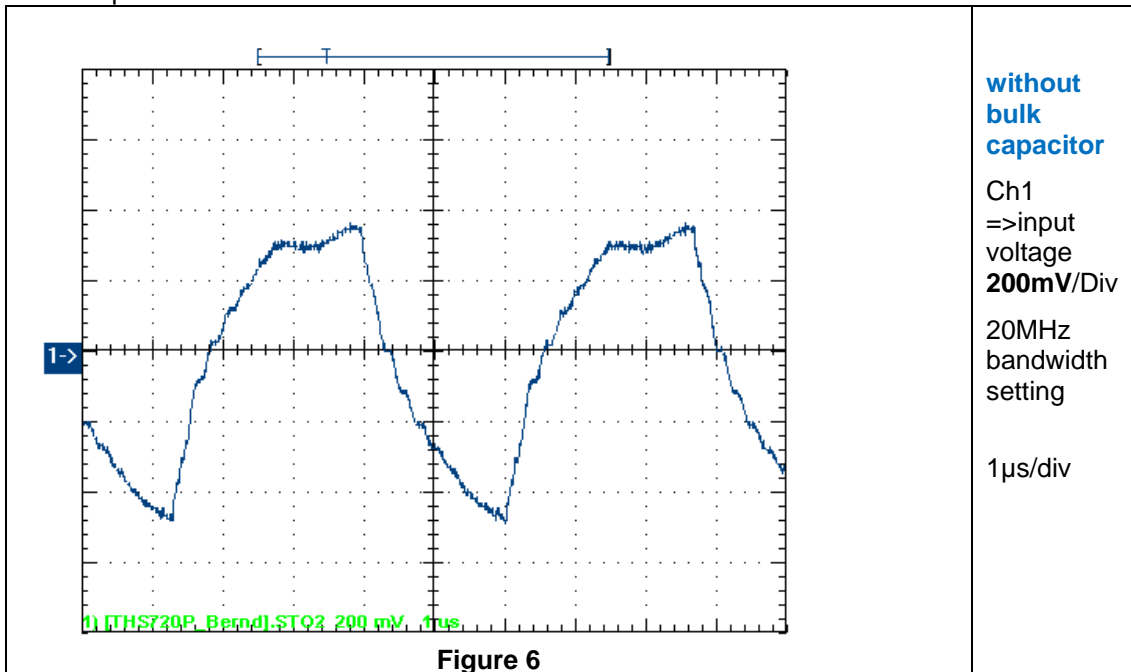
6 Output Ripple Voltage

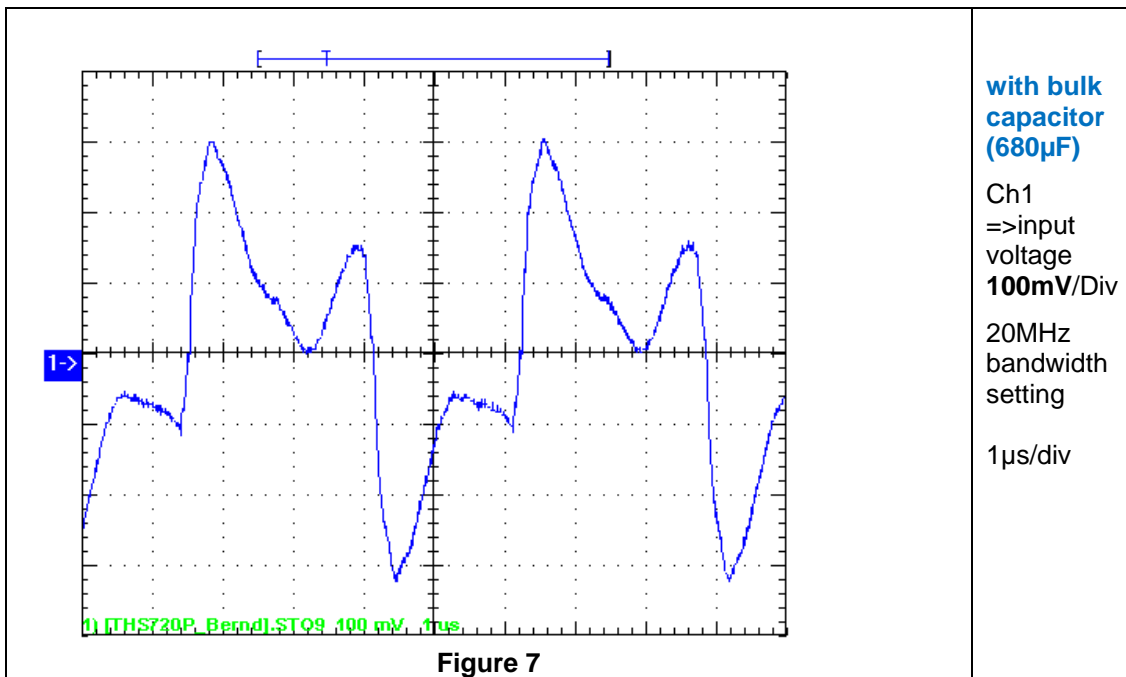
The output ripple voltage is shown in Figure 5. The image was taken with a 35 A load and 48V at the input. Voltage ripple du is 40mVpp, noise is 110mVp.



7 Input Ripple Voltage

The input ripple voltage is shown in Figure 6 and Figure 7. The input voltage was set to 48V with 20A output current.





8 Control Loop Frequency Response

Figure 8 shows the loop @ 30A with input voltages V_{min} 36V / V_{nom} 48V / V_{max} 72V:

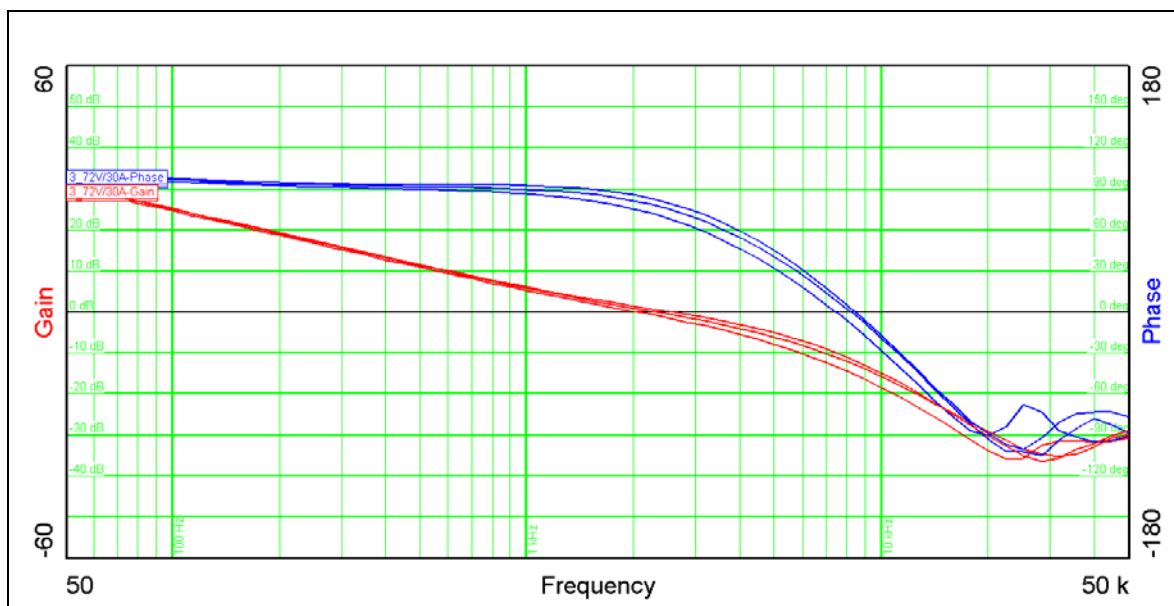


Figure 8

Table 4 summarizes the results from Figure 8

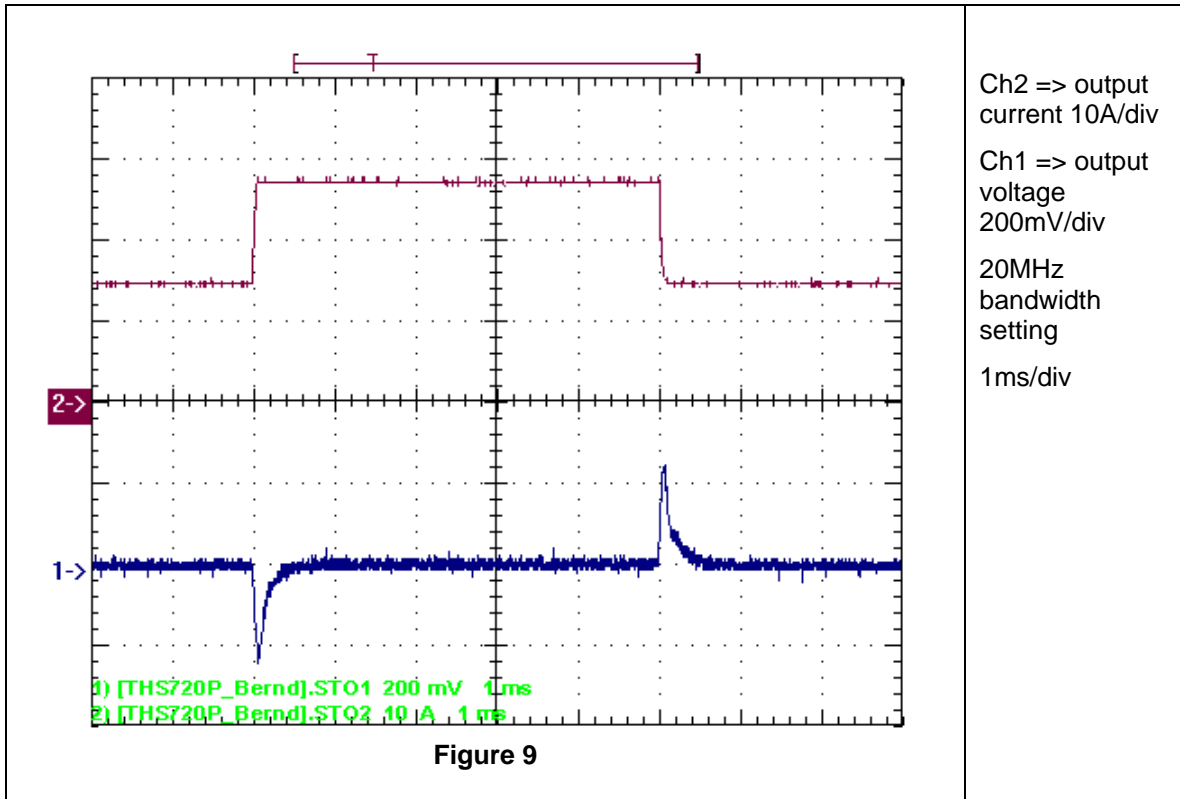
| | 36Vin | 48Vin | 72Vin |
|---------------------|-------|-------|-------|
| Bandwidth (kHz) | 2.04 | 2.31 | 2.55 |
| Phasemargin | 75° | 77.8° | 79.5° |
| slope (20dB/decade) | -0.87 | -0.80 | -0.74 |
| gain margin (dB) | -13.3 | 12.6 | -11.9 |
| slope (20dB/decade) | -1.79 | -1.8 | -1.9 |
| freq (kHz) | 7.45 | 8.23 | 8.45 |

Table 4

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9 Load Transients

The Figure 9 shows the response to load transients. The load is switching from 15A to 30A. with 100Hz frequency. Input voltage was set to 48V.



10 Waveforms

10.1 Primary FET Vds

With input voltage set to 48V results in the waveform shown in Figure 10; output current was set to 20A. *Keep in mind – NMOS conducts as gate is high, figures are not in phase:*

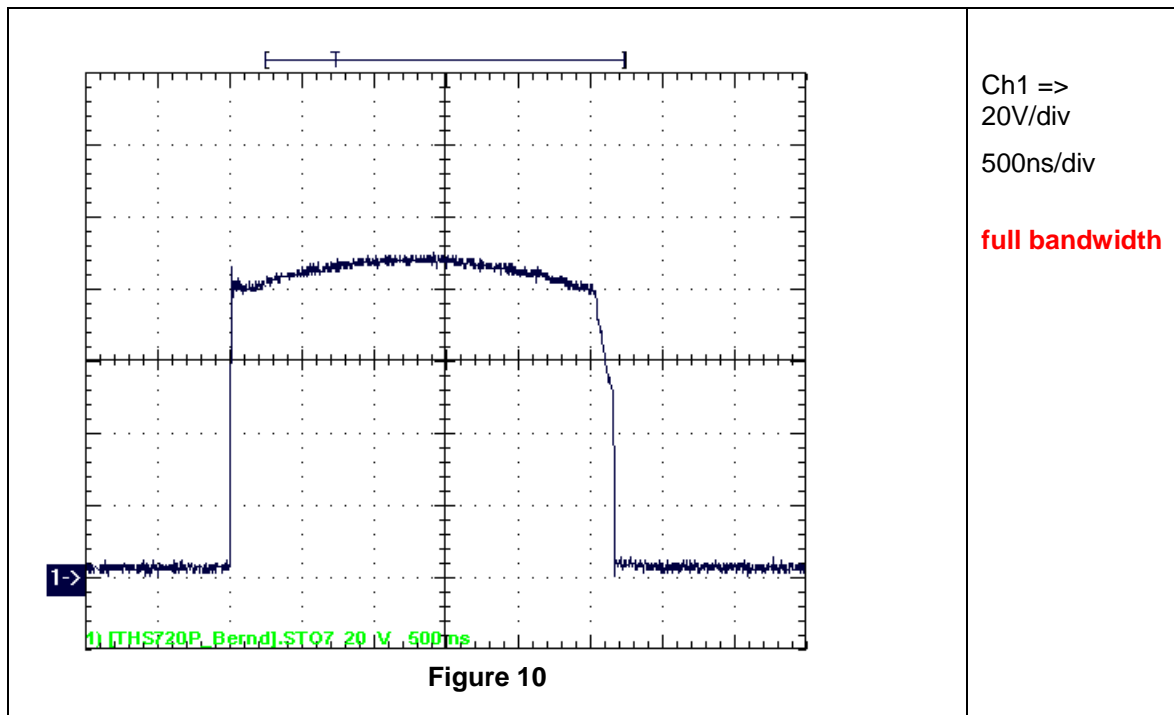
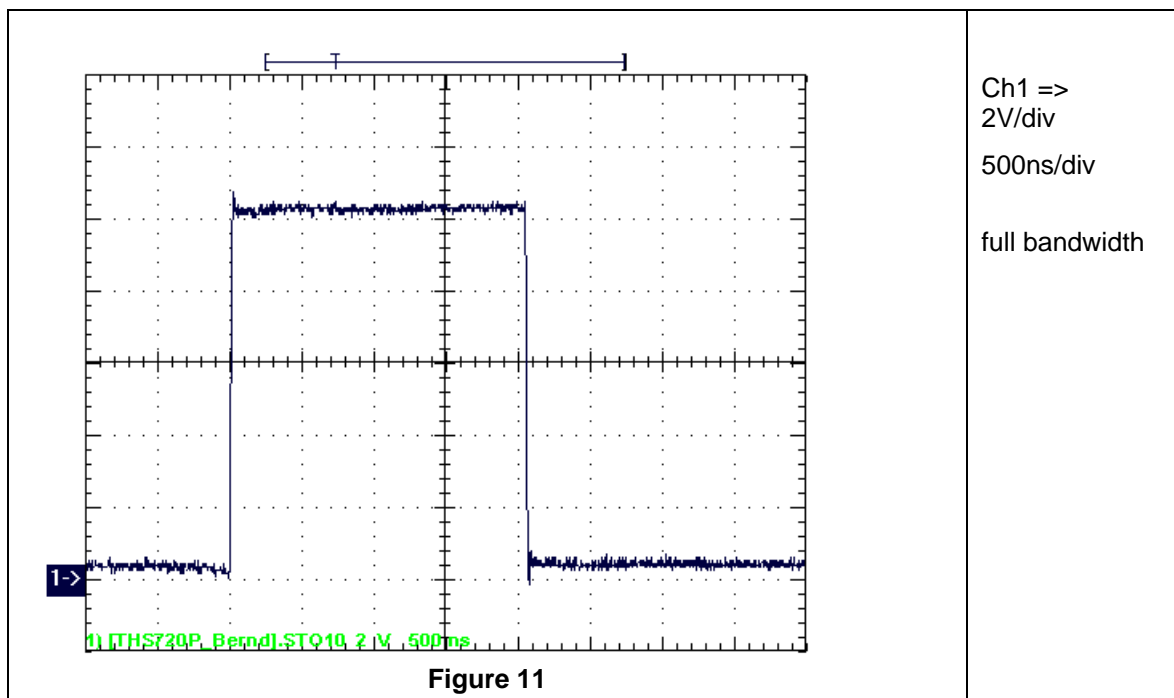


Figure 11 shows the Gate-Source voltage Vgs of the same FET



10.2 Active Clamp FET Vds

With input voltage set to 48V results in the waveform shown in Figure 12; output current was set to 20A.

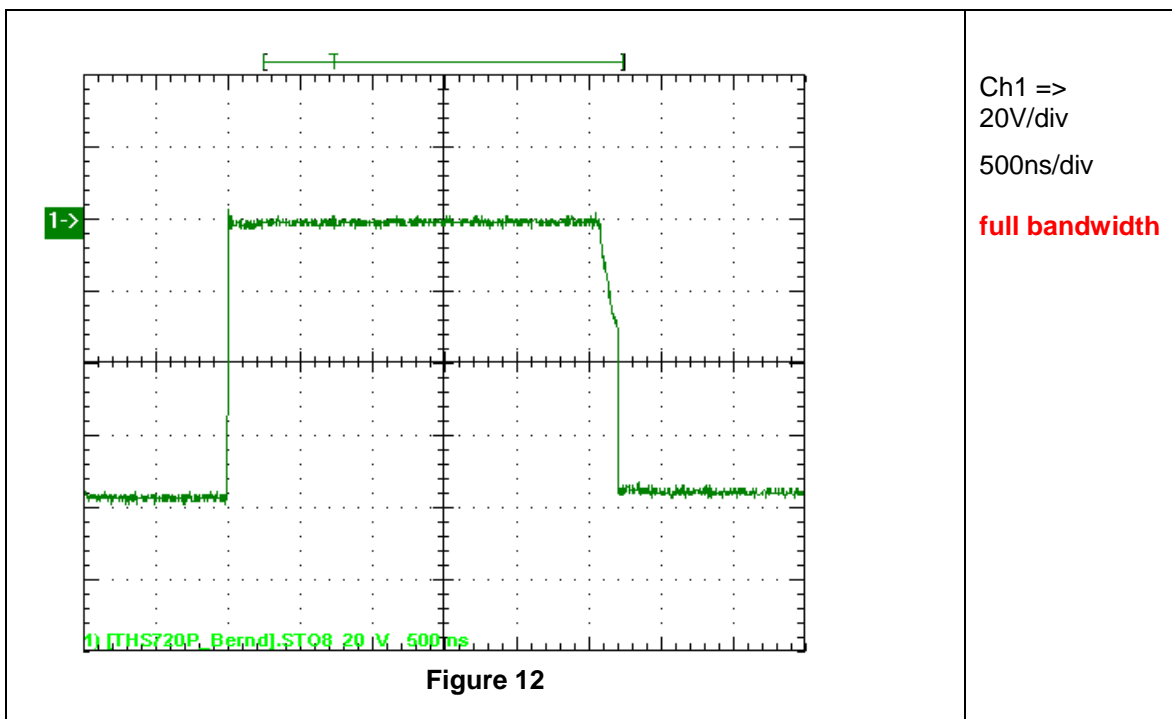
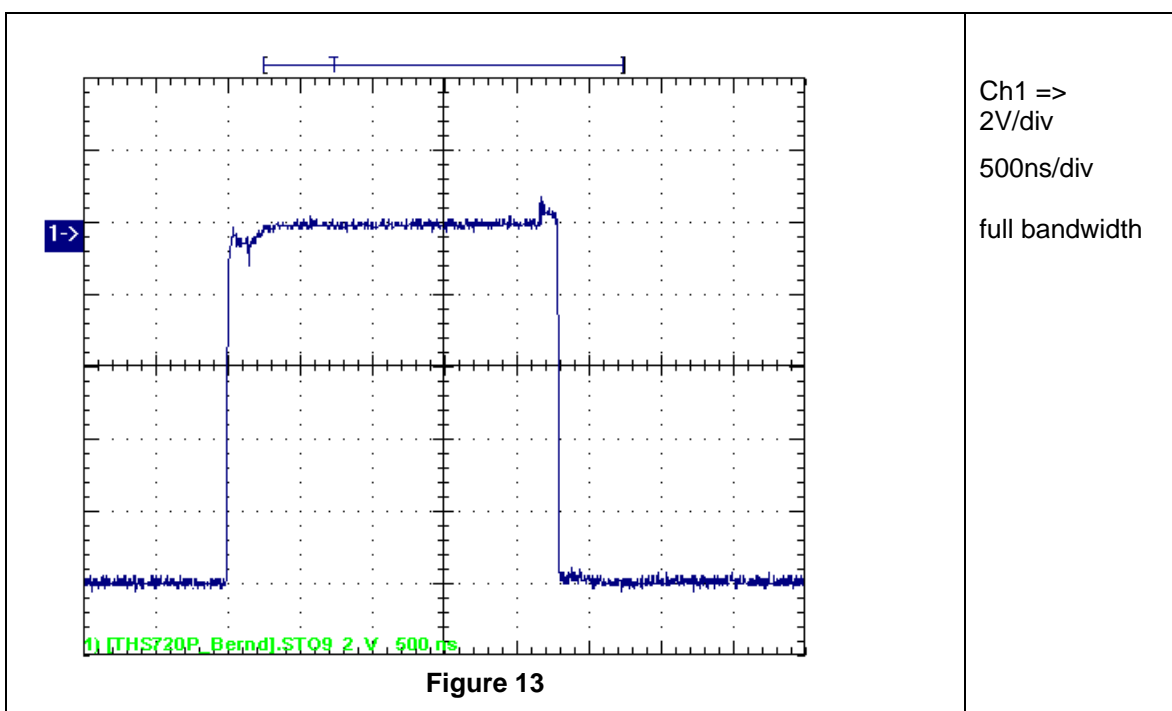


Figure 13 shows the Gate-Source voltage Vgs of the same FET



10.3 Freewheeling FET, secondary side

With input voltage set to 48V results in the waveform shown in Figure 14; output current was set to 20A.

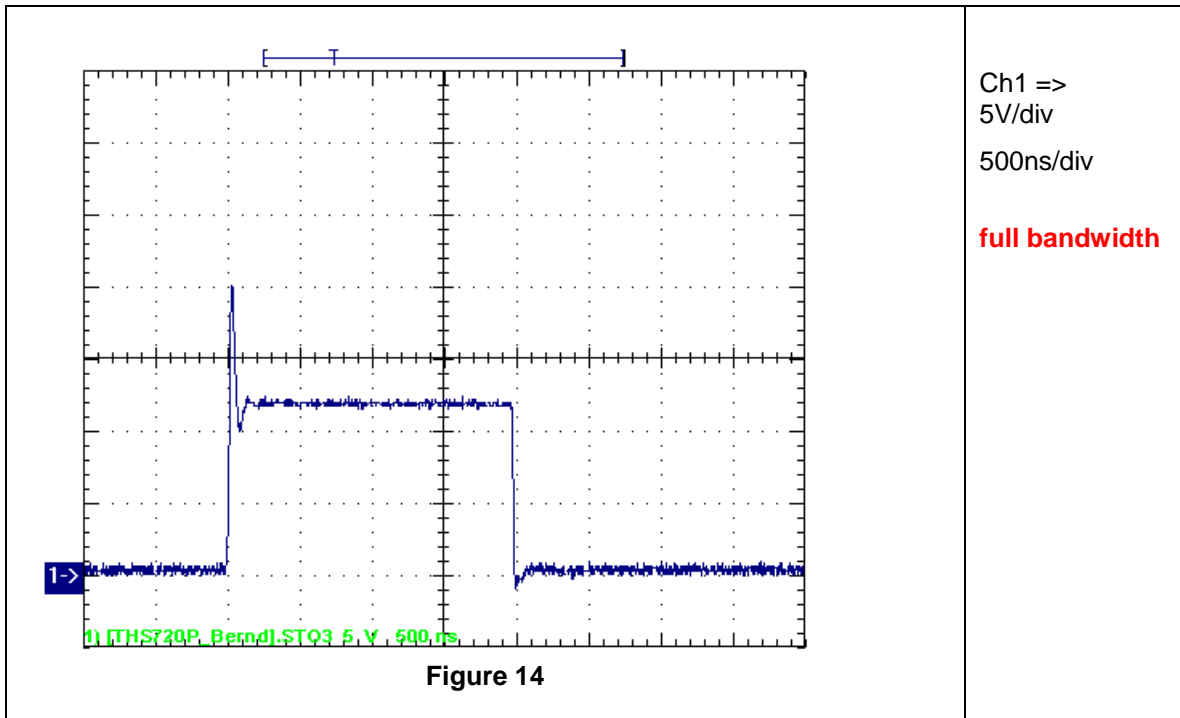
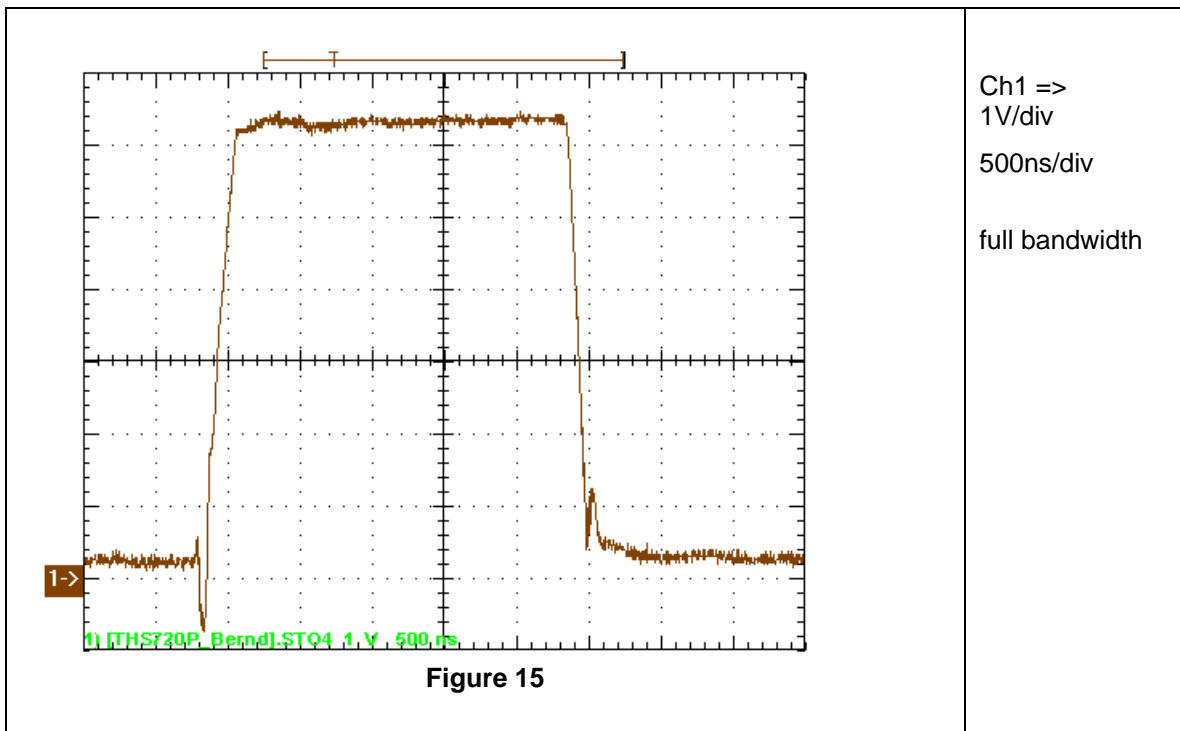


Figure 15 shows the Gate-Source voltage of the same FET



10.4 Synchronous Rectifier, secondary side

With input voltage set to 48V results in the waveform shown in Figure 16. Output current was set to 20A.

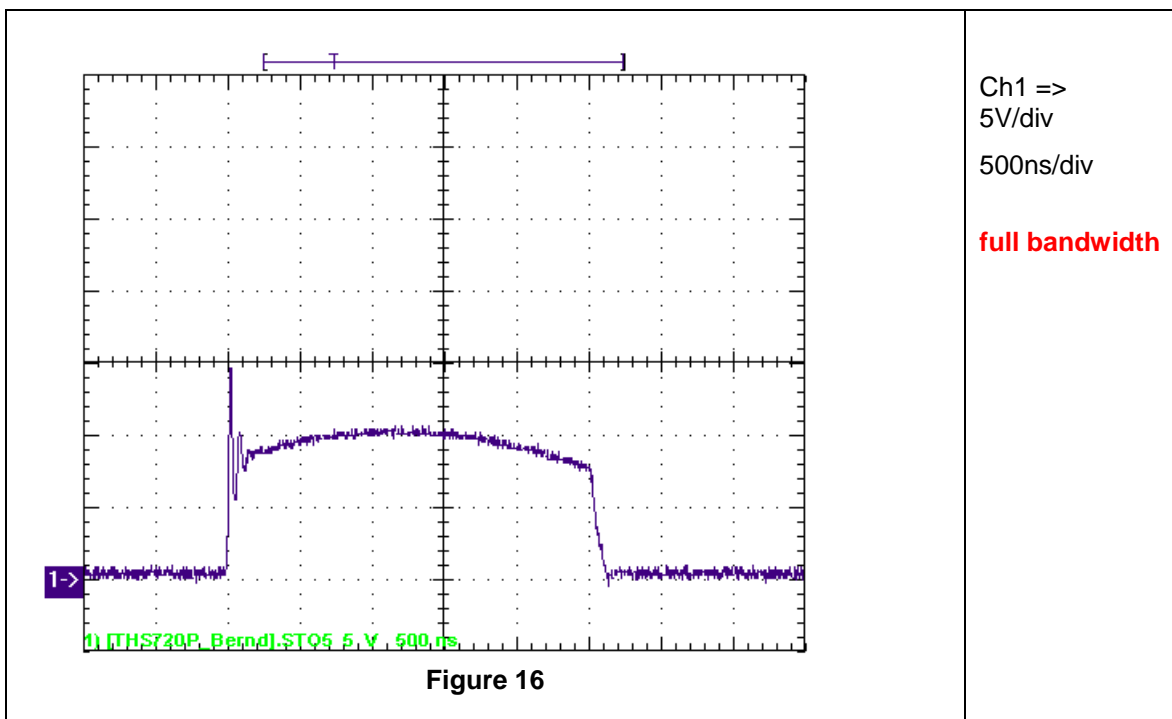
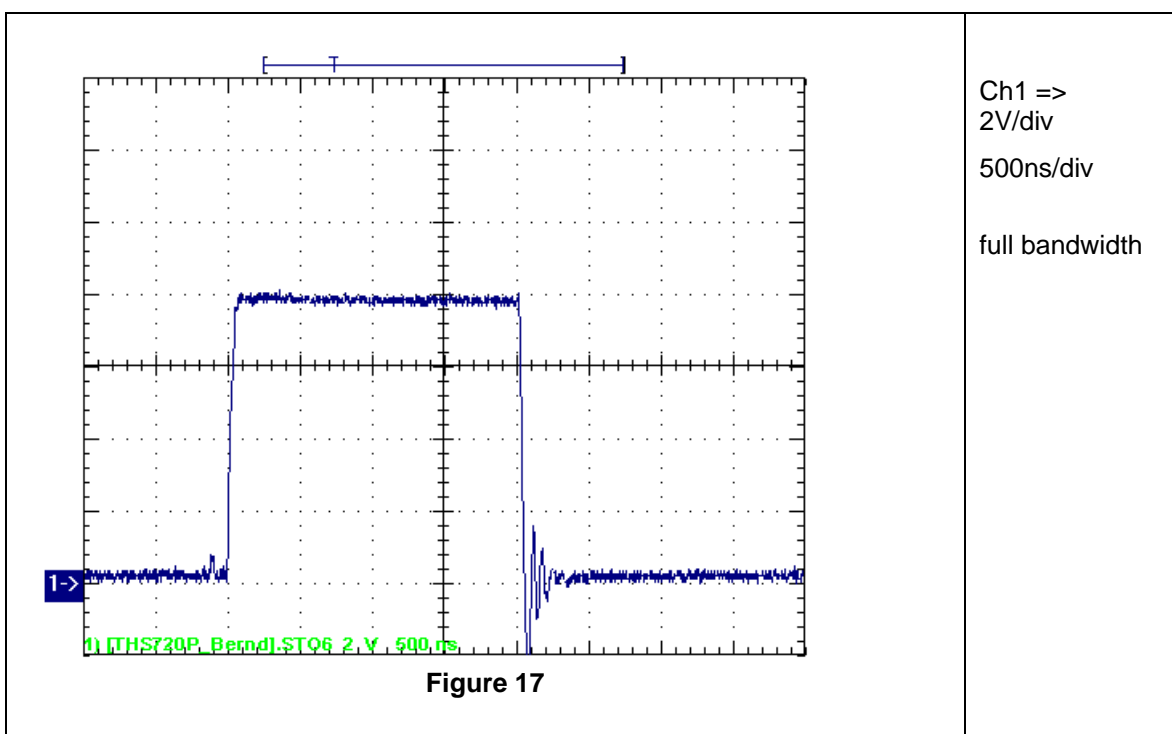


Figure 17 shows the Gate-Source voltage of the same FET



11 Thermal Image

11.1 25A load current, no air flow, convectional cooling:

Topside

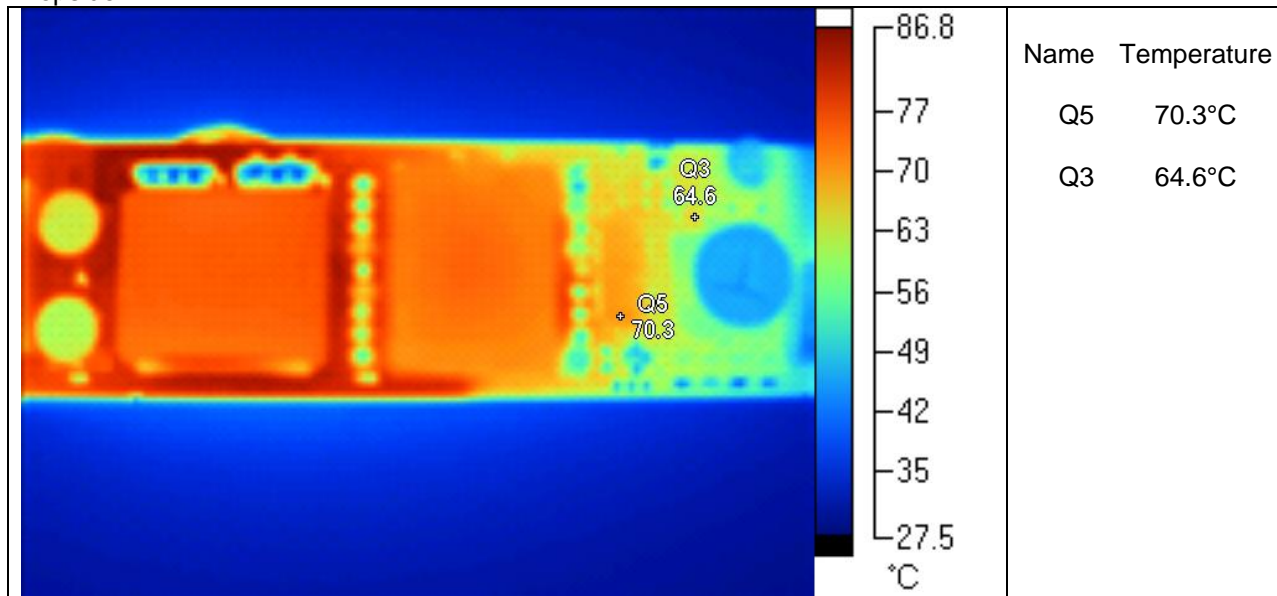


Figure 18

Bottomside

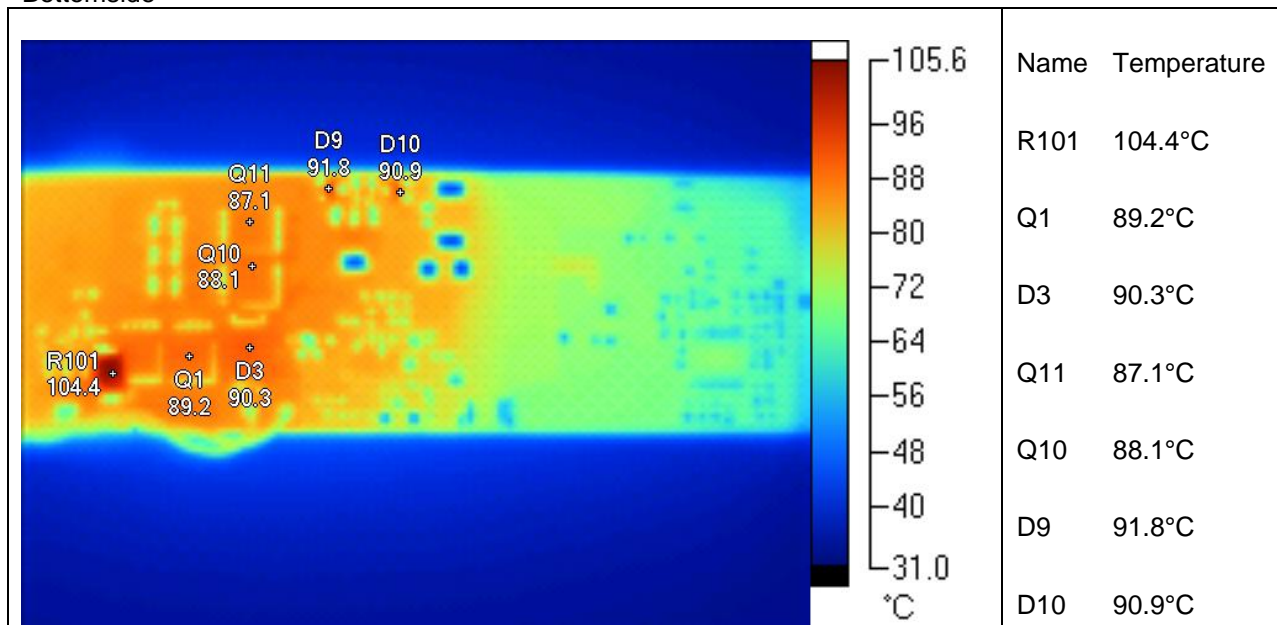


Figure 19

11.2 35A with forced air flow 2m/s / 400lfm:

Topside

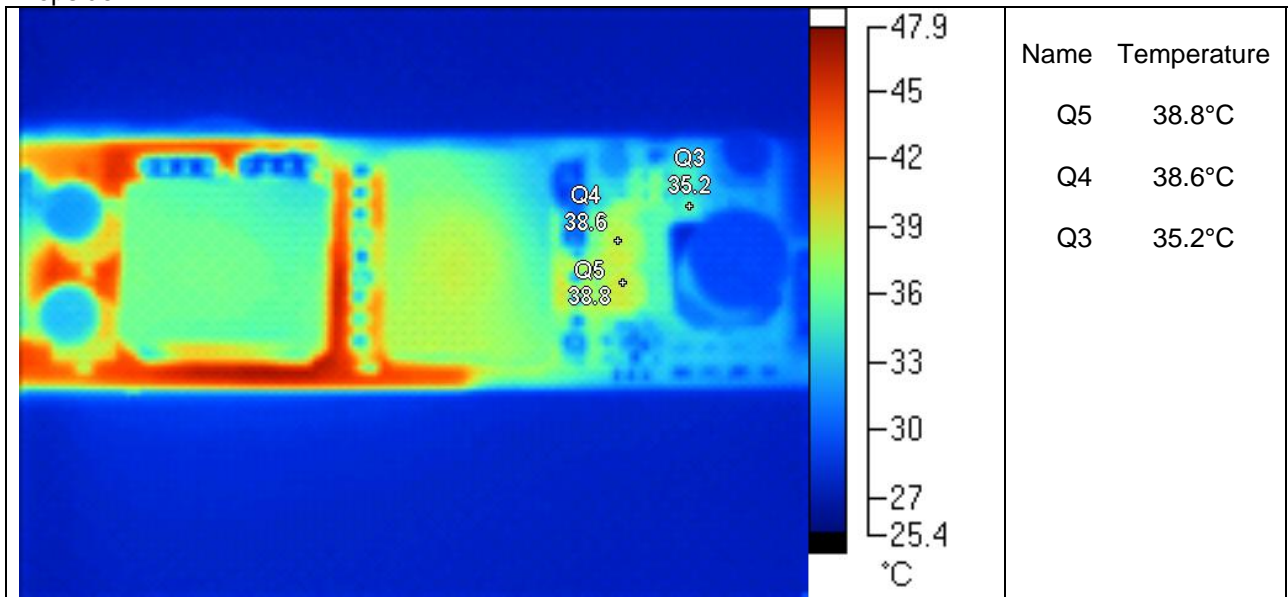


Figure 20

Bottomside

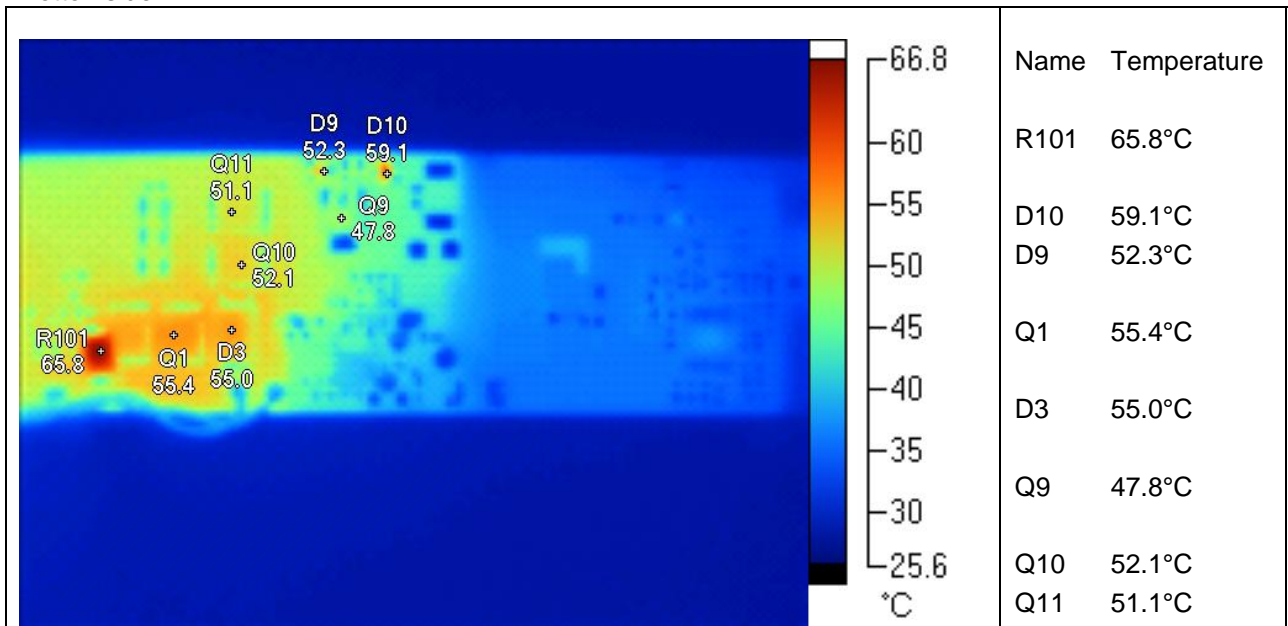


Figure 21

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12 Miscellaneous Measurements

- Bias Voltage 10.36 at nominal input 48V / 20Amps output
total variation across line and load is:
9.15V (36Vin/0Aout) to 11.56V (72Vin/35Aout)
- UV ON 36.1V
- UV OFF 34.5V
- OV ON 71.5V
- OV OFF 72.1V
- Fsw 211kHz
- Rise of full load at 36Vin is limited to 33A due to CS limitation.

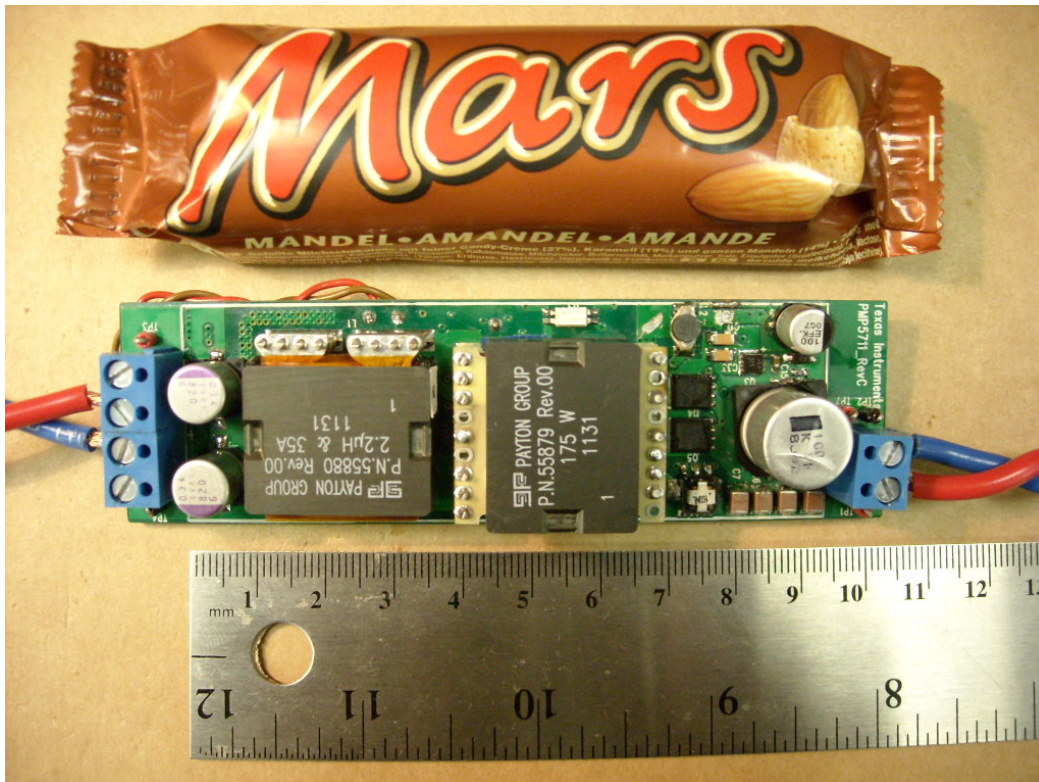
13 Summary & Pic

With an efficiency of >94% across 13Amps load to 35Amps full load and peak efficiency of 95% the results for a 5V forward converter are fine.

Due to space requirements the design is made as small as possible and is specified for forced cooling. Achieved size is L x W x H = 93mm x 31mm x 19mm.

If REMOTE SENSE isn't a must go for rugged TL431 as error amplifier. If dealing w/ TL103 select proper placement at secondary side and root shielding ground plane below this IC. So some caps could be removed and bandwidth could be doubled.

To reduce ringing on secondary side place RC snubber directly to Q1/Q2.



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For Feasibility Evaluation Only, in Laboratory/Development Environments. The reference design is not a complete product. It is intended solely for use for preliminary feasibility evaluation in laboratory / development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical / mechanical components, systems and subsystems. It should not be used as all or part of a production unit.

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