PMP7032RevB Test Results

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Measurements for 20Amps load were done with forced cooling;
for 20Amps continuous layout at secondary side needs redesign;
(copper area around SR has to be increased).

The design itself needs a better xfmr (see transformer spec at PMP7032RevA)

- *the xfmr does not meet isolation requirements*
- *primary inductance is to small, so magnetizing current too big*
- *coupling is poor, so leakage inductance is too big*

for 75 V input with this transformer an additional RC snubber network R201/C201 is needed to cover this voltage range; use of transformer w/ better coupling will provide better efficiency here; clamping circuit D1/C1/R1 will be sufficient.

1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 18V, with 20A load at the output.

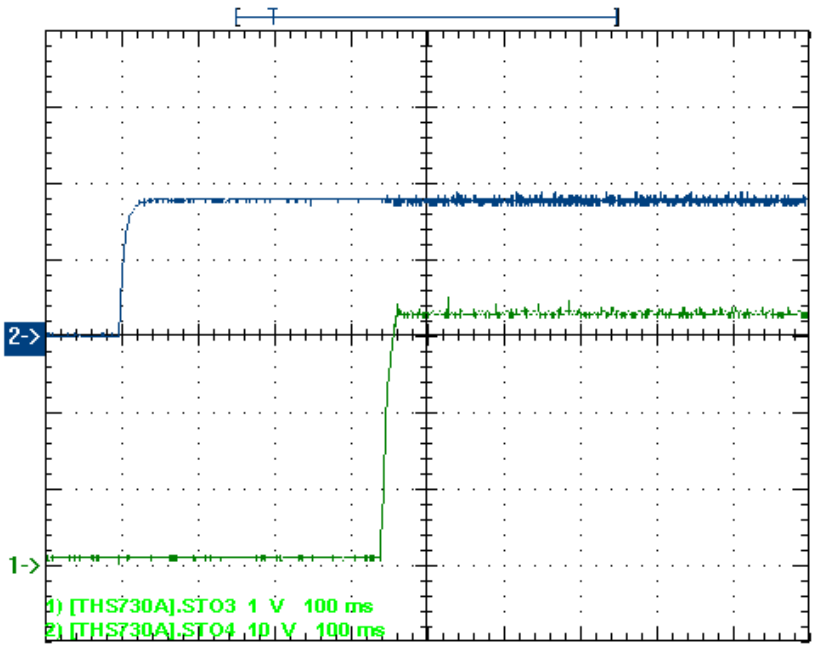


Figure 1

Ch2=> input voltage 10V/div

Ch1=> output voltage 1V/div

100ms/div

The startup waveform is shown in the Figure 2. The input voltage was set at 48V, with 20A load at the output

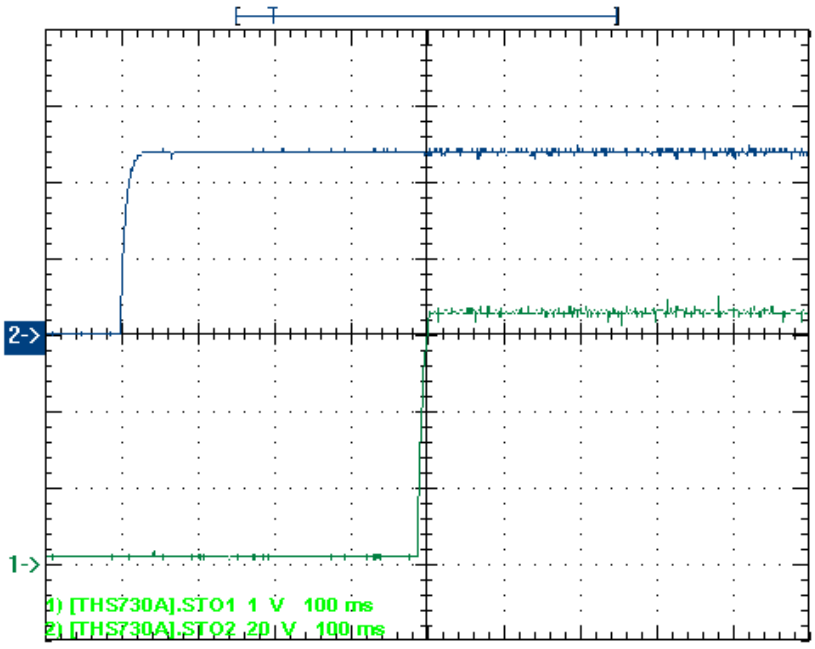


Figure 2

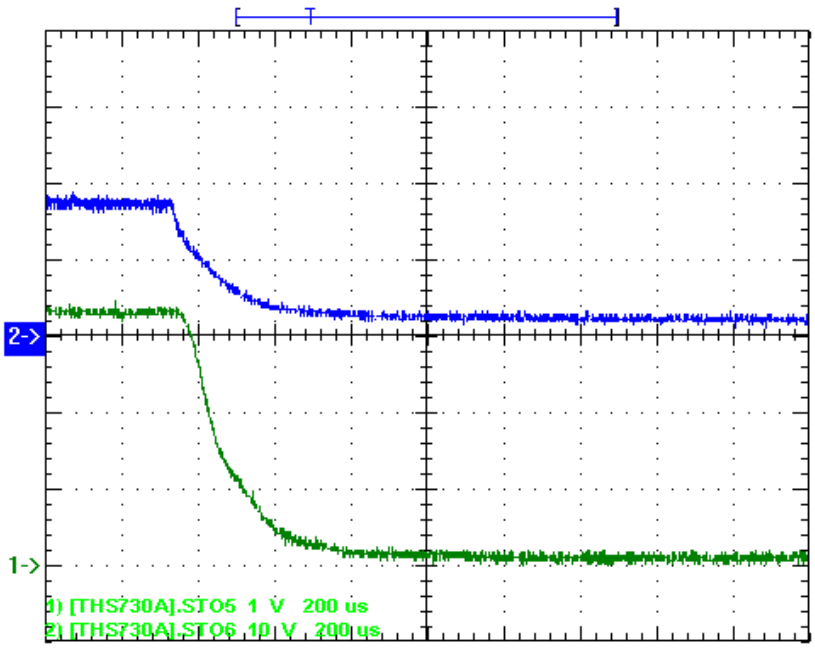
Ch2=> input voltage 20V/div

Ch1=> output voltage 1V/div

100ms/div

2 Shutdown

The shutdown waveform is shown in the Figure 3. The input voltage was set at 18V, with 20A, load on the output.



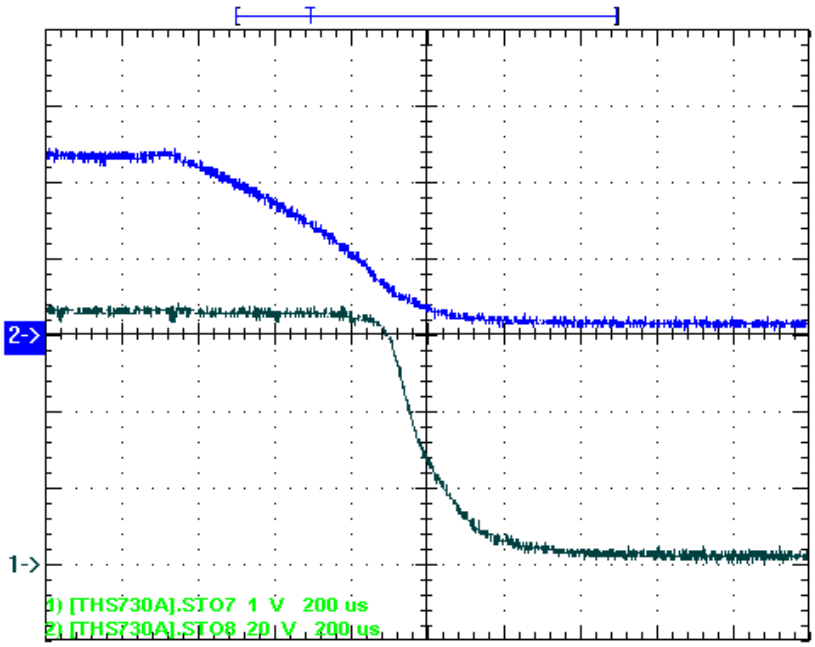
Ch2=> input voltage 10V/div

Ch1=> output voltage @ 1V/div

200µs/div

Figure 3

The shutdown waveform is shown in the Figure 4. The input voltage was set at 48V, with 20A, load on the output.



Ch2=> input voltage 20V/div

Ch1=> output voltage @ 1V/div

200µs/div

Figure 4

3 Efficiency

The efficiency is shown in the Figure 5 below.

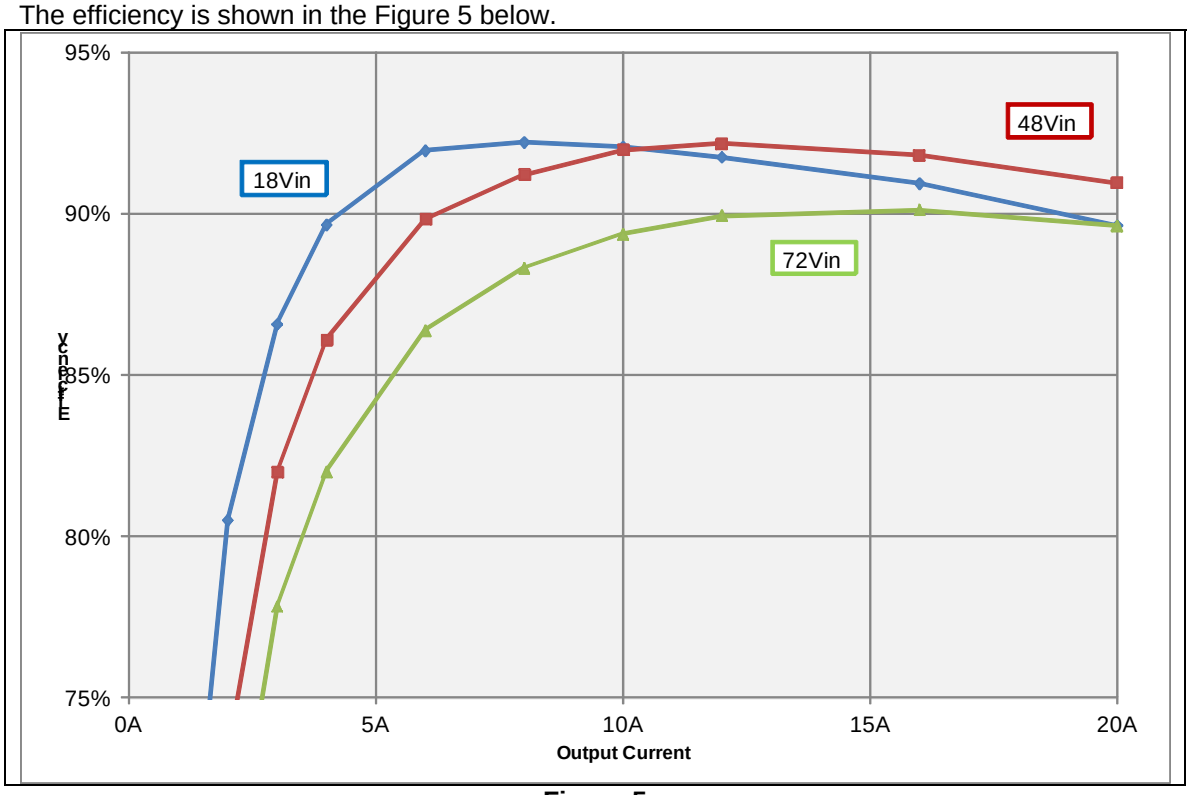


Figure 5

4 Load Regulation

The load regulation of the output is shown in the Figure 6 below.

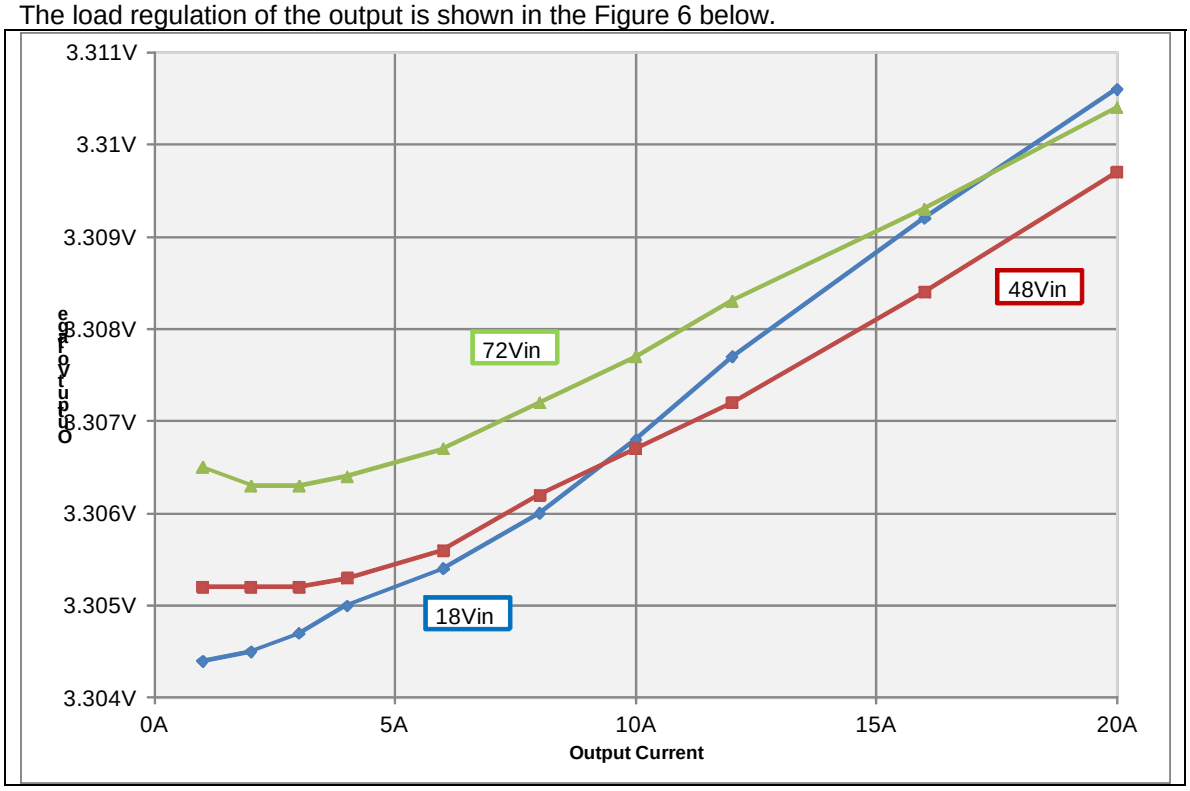


Figure 6

5 Line Regulation

The line regulation at 20A output current is shown in Figure 7

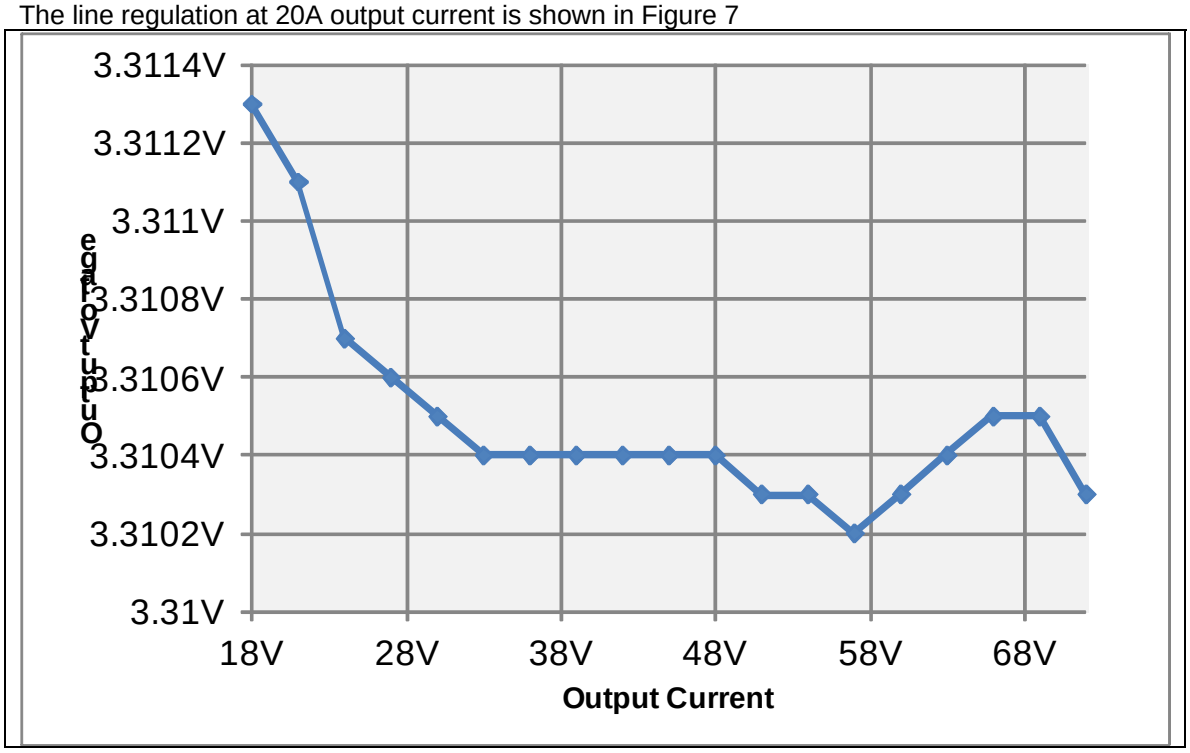


Figure 7

With the measurment above also the efficiencies were calculated. This is shown in Figure 8

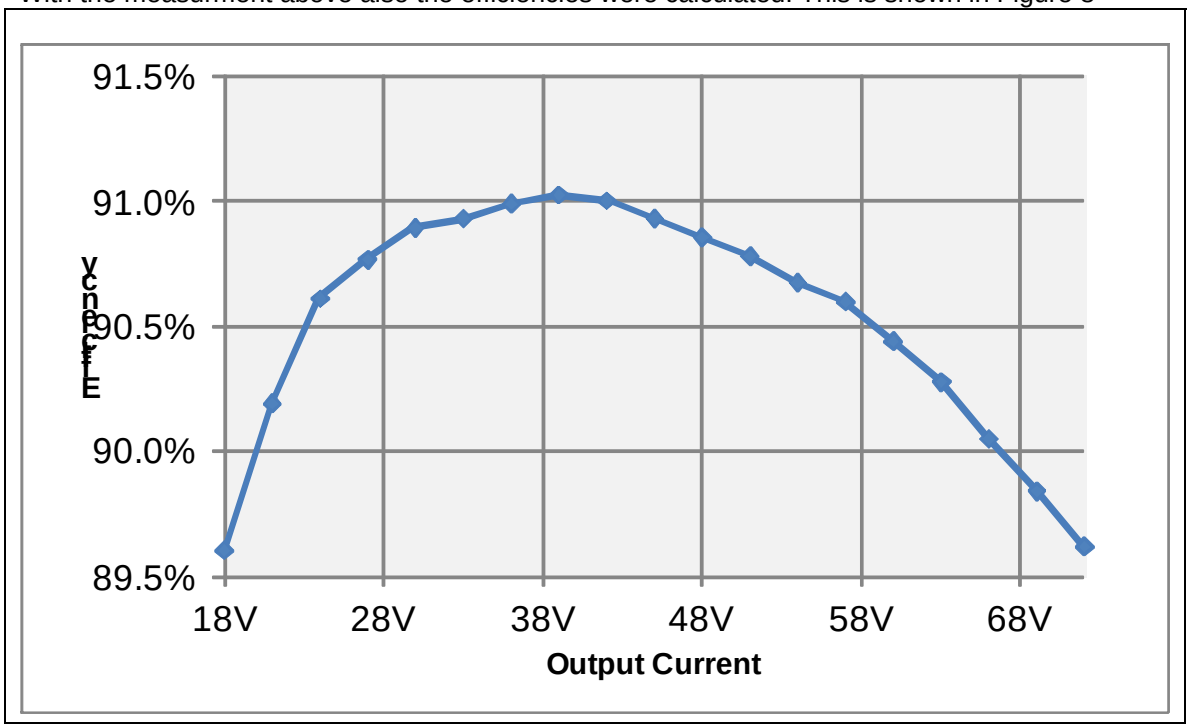


Figure 8

6 Output Ripple Voltage

The output ripple voltage is shown in Figure 9. The image was taken with a 20 A load.

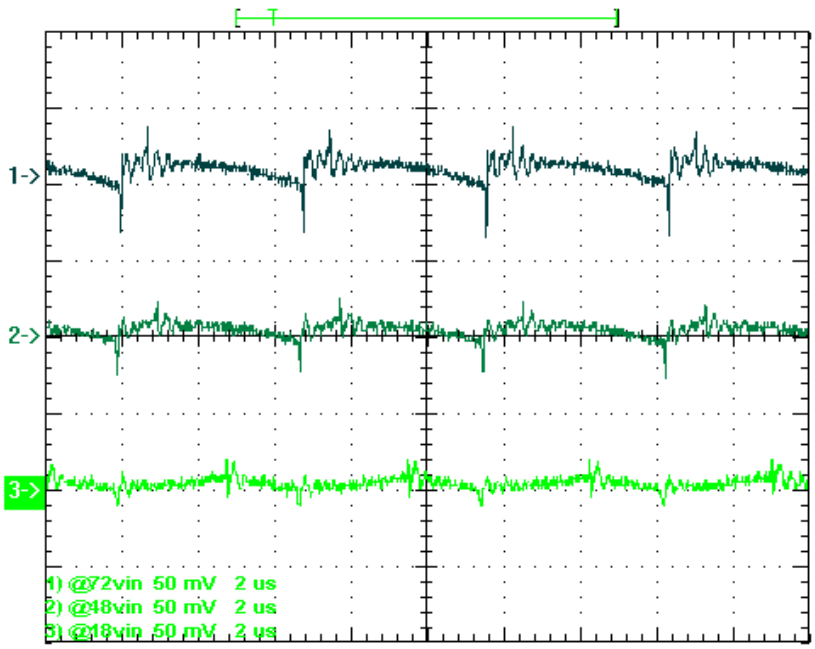


Figure 9

Ch1 =>output voltage @ 72Vin

Ch2 =>output voltage @ 48Vin

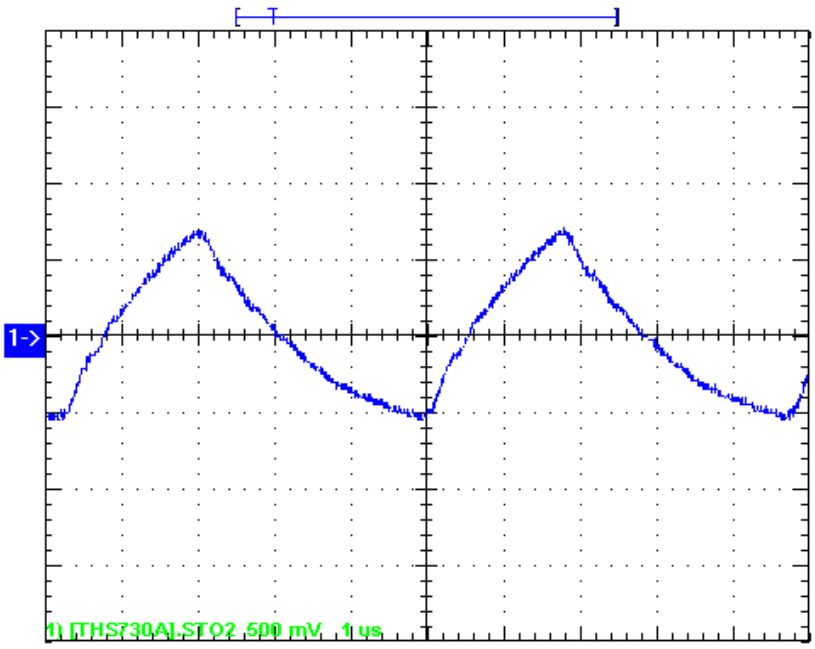
Ch1 =>output voltage @ 18Vin
50mV/Div

20MHz bandwidth setting

2µs/div

7 Input Ripple Voltage

The input ripple voltage is shown in Figure 10. The input voltage was set to 18V with 20A output current.



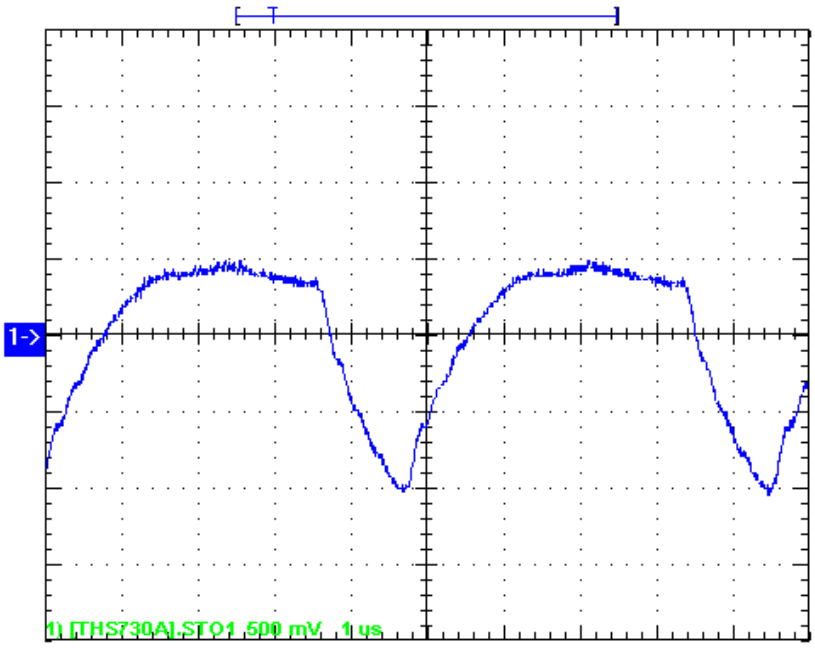
Ch1 =>input voltage 500mV/Div

20MHz bandwidth setting

1µs/div

Figure 10

The input ripple voltage is shown in Figure 11. The input voltage was set to 48V with 20A output current.



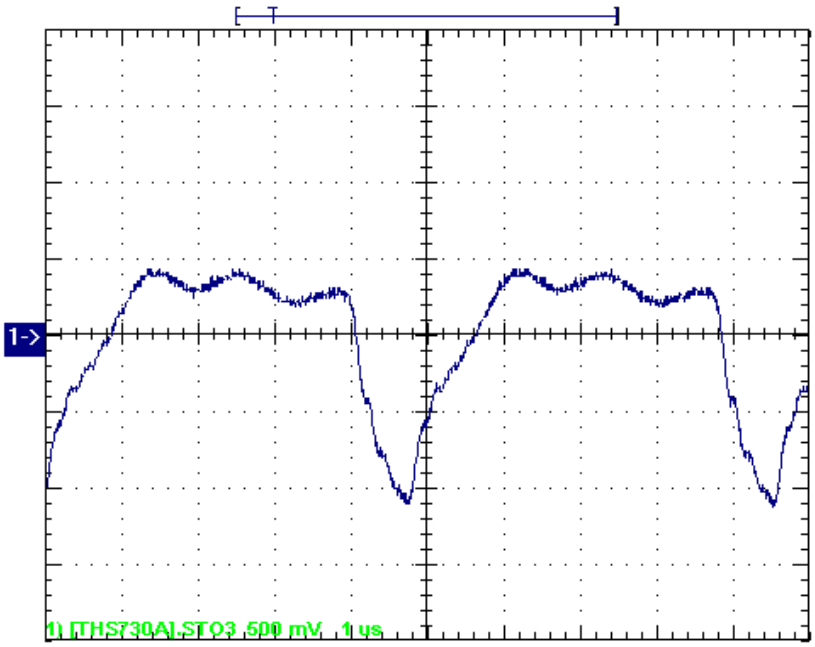
Ch1 =>input voltage 500mV/Div

20MHz bandwidth setting

1µs/div

Figure 11

The input ripple voltage is shown in Figure 12. The input voltage was set to 48V with 20A output current.



Ch1 =>input voltage 500mV/Div

20MHz bandwidth setting

1µs/div

Figure 12

8 Control Loop Frequency Response

Figure 13 shows the loop response @ 20A with 20V, 48V and 65V input voltage

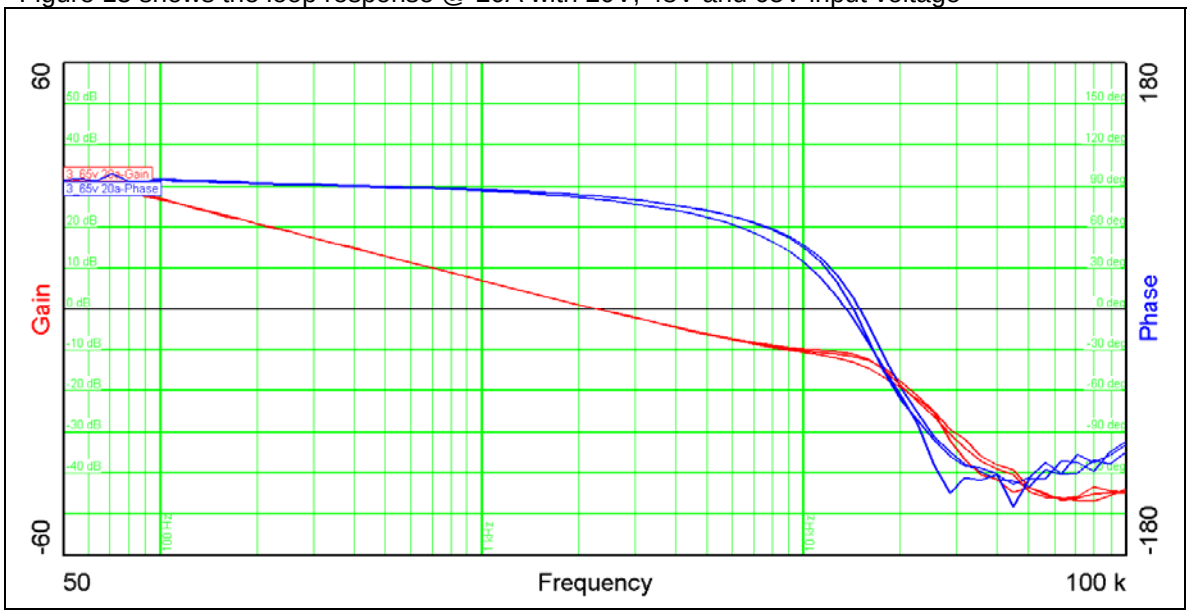


Figure 13

Table 1 summarizes the results from Figure 13

	20Vin	48Vin	65Vin
Bandwidth (kHz)	2.29	2.29	2.30
Phasemargin	80.4	82.6°	82.6
slope (20dB/decade)	-0.97	-0.955	-0.959
gain margin (dB)	-12.7	-12.0	-11
slope (20dB/decade)	-1	-1	-1.55
freq (kHz)	13.5	14.9	14.2

Table 1

9 Load Transients

Figure 14 shows the response to load transients. The load is switching from 7.5A to 20A.with 100Hz frequency. Input voltage was set to 18V.

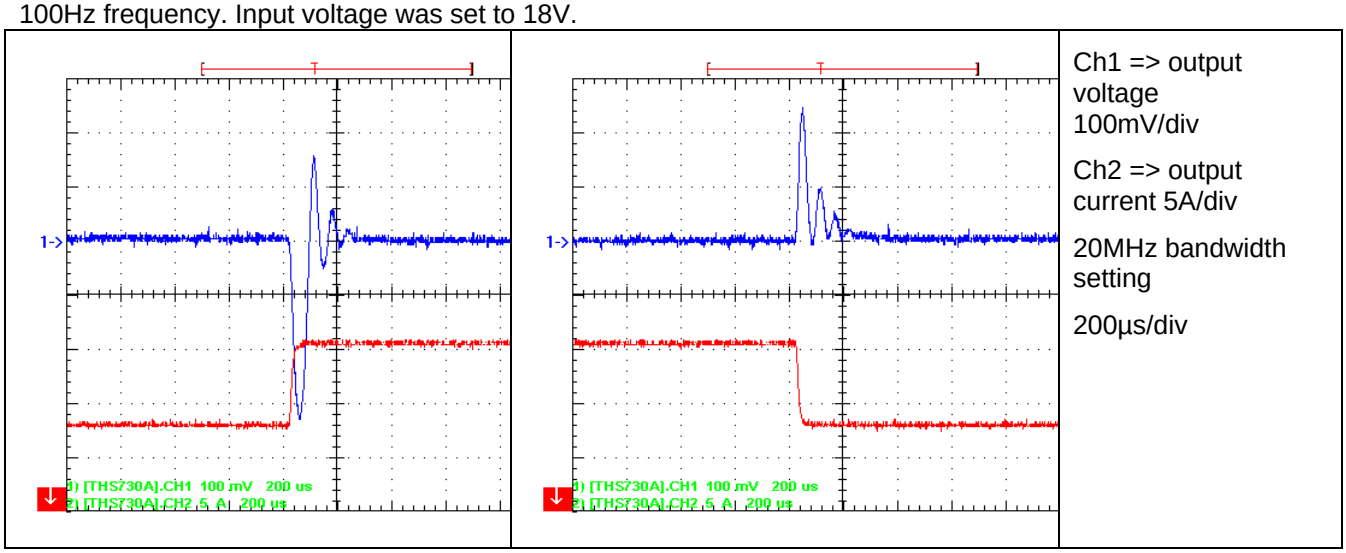


Figure 14

Figure 15 shows the response to load transients. The load is switching from 7.5A to 15A.with 100Hz frequency. Input voltage was set to 48V.

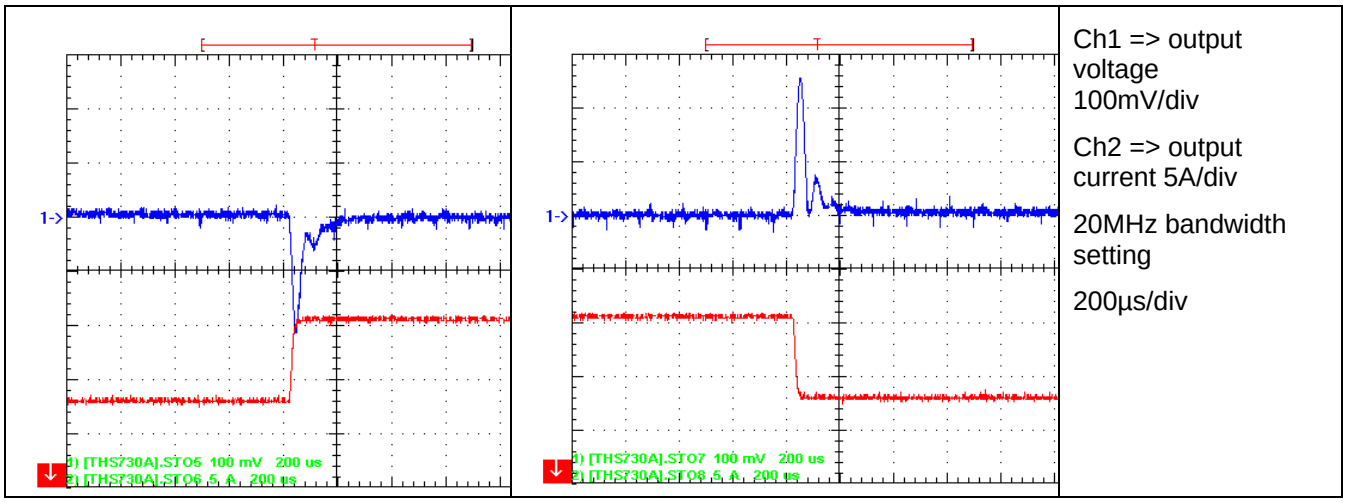


Figure 15

Figure 16 shows the response to load transients. The load is switching from 7.5A to 15A.with 100Hz frequency. Input voltage was set to 72V.

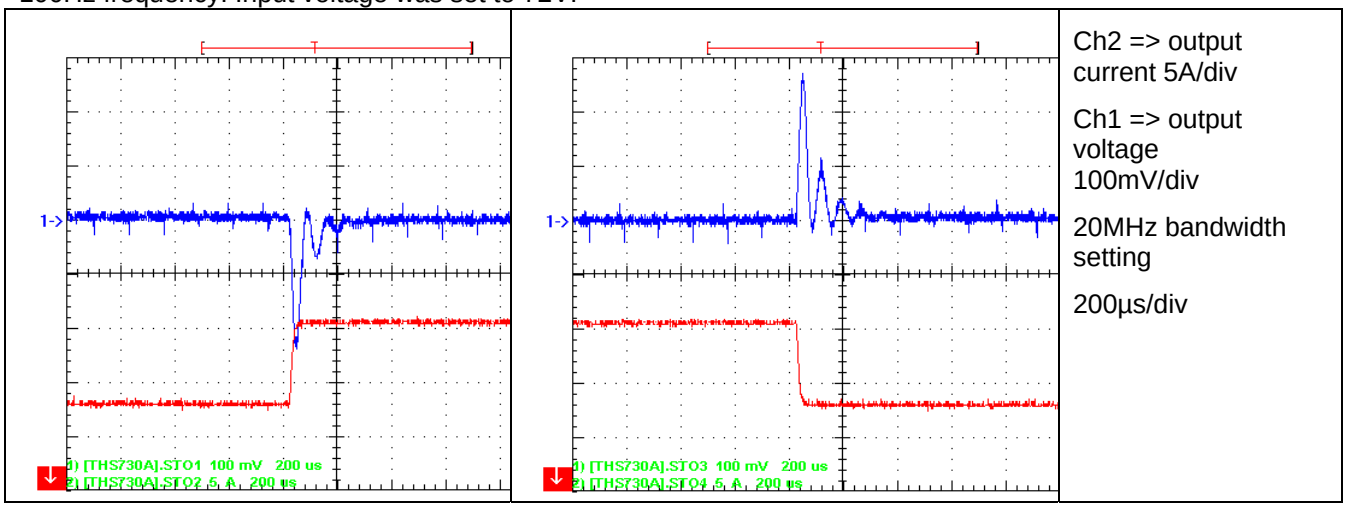


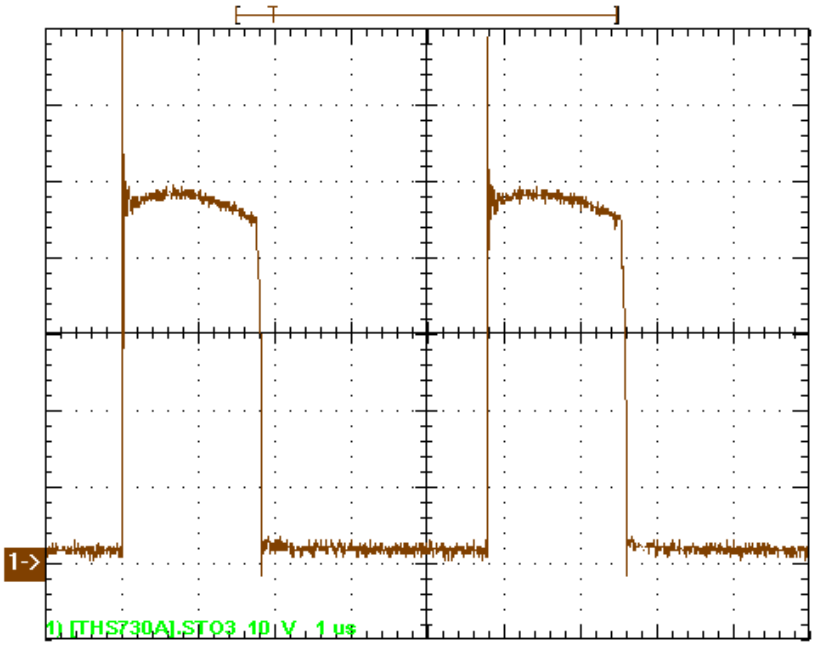
Figure 16

10 Waveforms

10.1 18V input voltage

10.1.1 Primary FET (Q5)

With input voltage set to 18V results in the waveform shown in Figure 17 Output current was set to 20A.

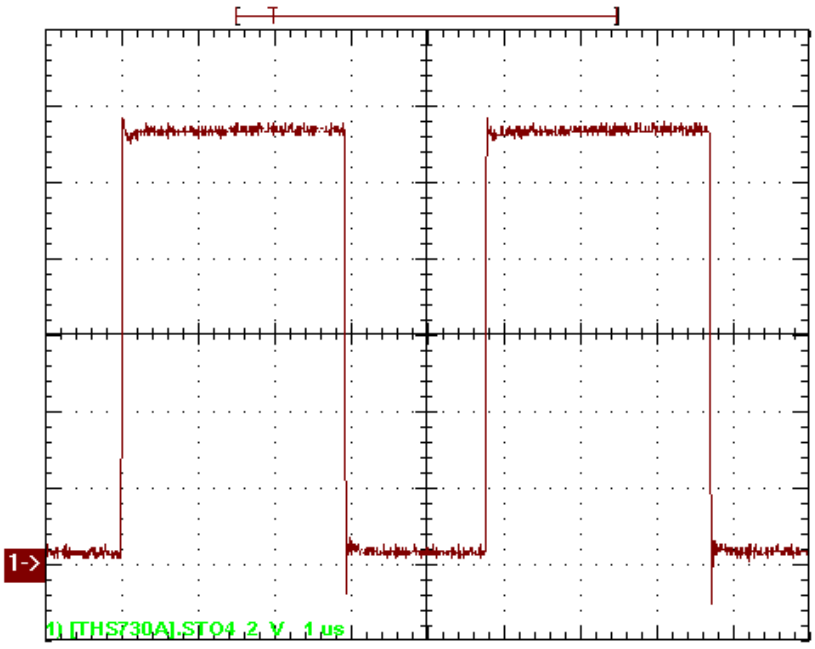


Ch1 =>
10V/div

1µs/div
full bandwidth

Figure 17

Figure 18 shows the Gate-Source voltage of the same FET



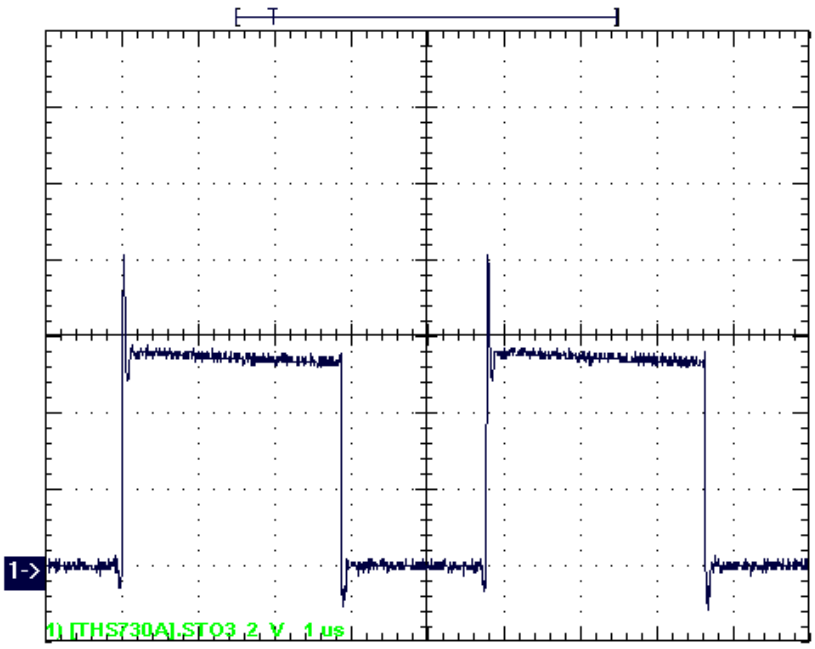
Ch1 =>
2V/div

1µs/div
full bandwidth

Figure 18

10.1.2 Freewheeling FET (Q2)

With input voltage set to 18V results in the waveform shown in Figure 19 Output current was set to 20A.

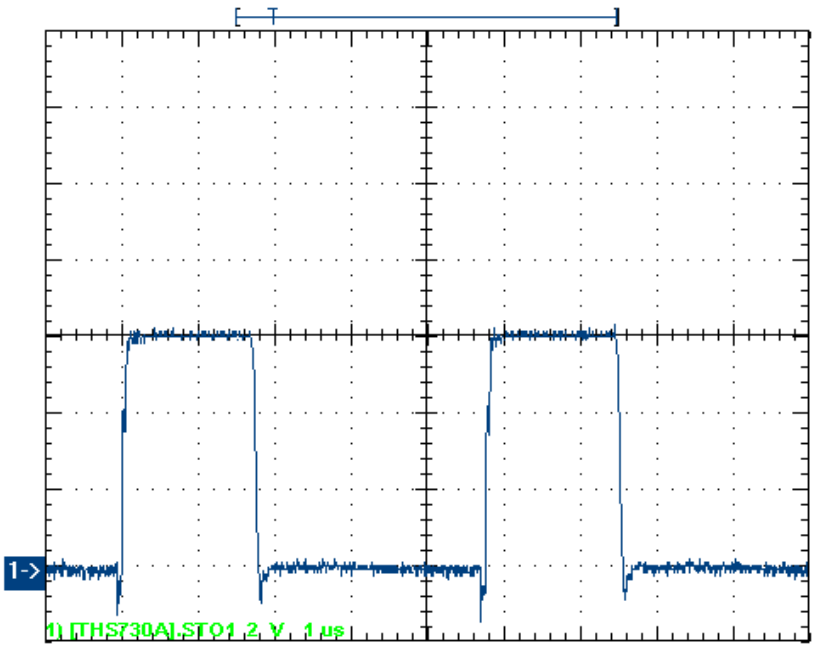


Ch1 =>
2V/div

1µs/div
full bandwidth

Figure 19

Figure 20 shows the Gate-Source voltage of the same FET



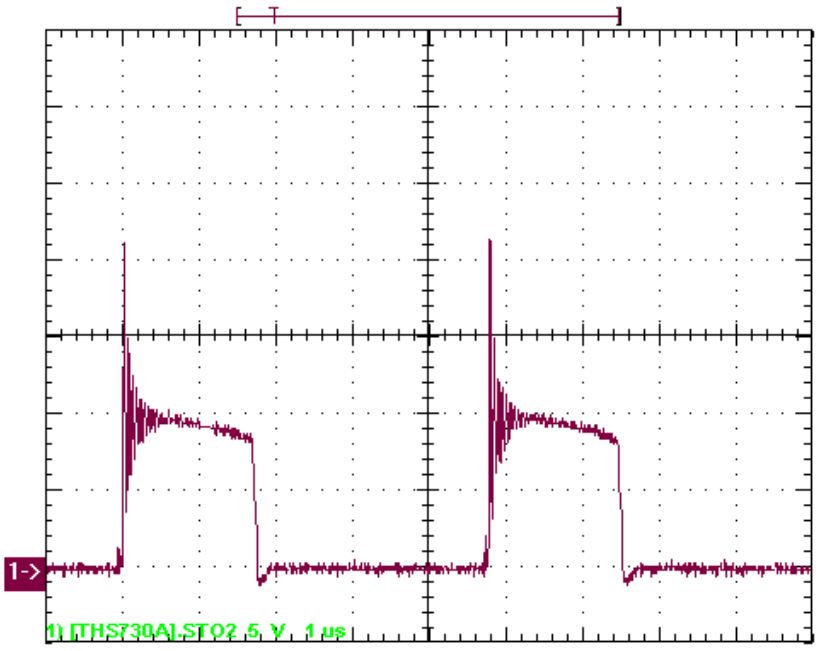
Ch1 =>
2V/div

1µs/div
full bandwidth

Figure 20

10.1.3 Synchronous Rectifier

With input voltage set to 18V results in the waveform shown in Figure 21 Output current was set to 20A.

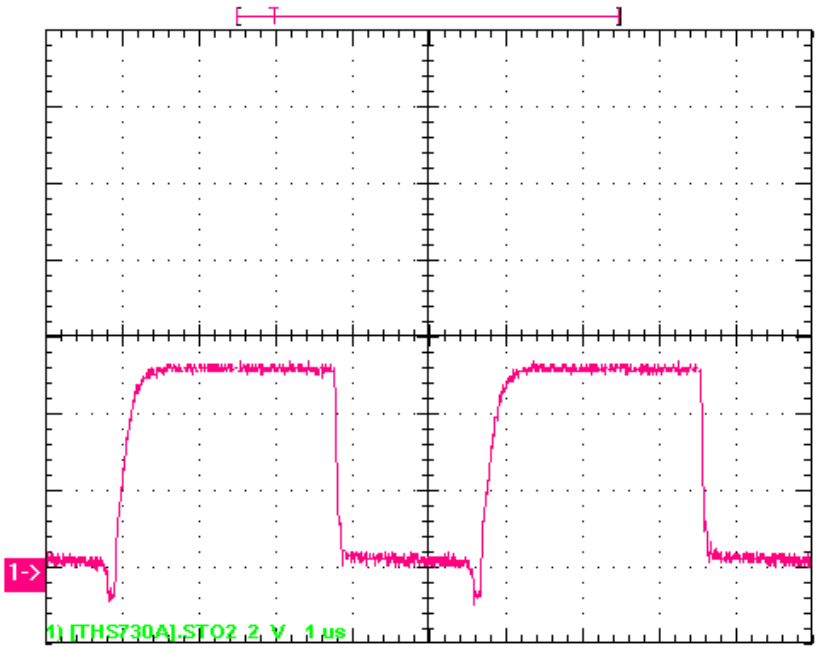


Ch1 =>
5V/div

1µs/div
full bandwidth

Figure 21

Figure 22 shows the Gate-Source voltage of the same FET



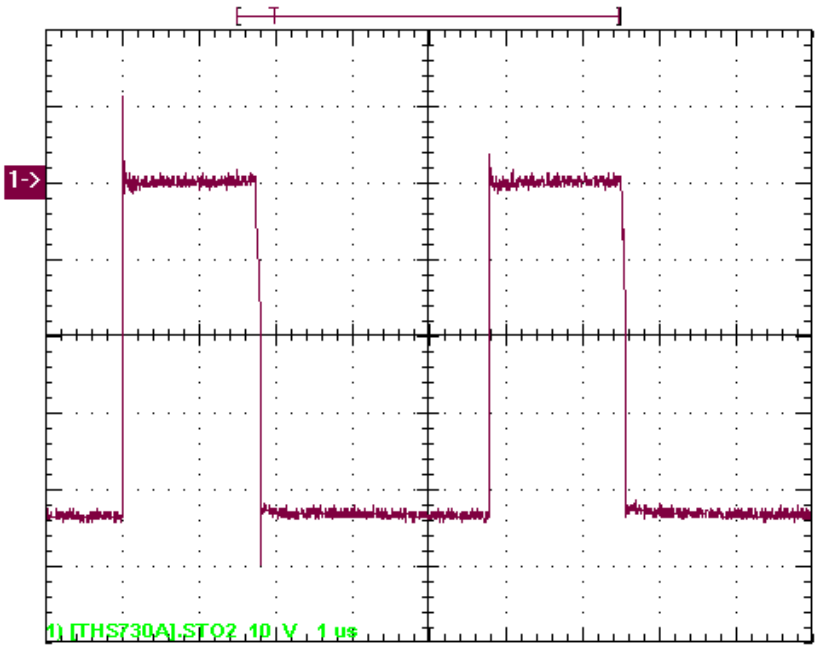
Ch1 =>
2V/div

1µs/div
full bandwidth

Figure 22

10.1.4 Active Clamp (Q4)

With input voltage set to 18V results in the waveform shown in Figure 23 Output current was set to 20A.

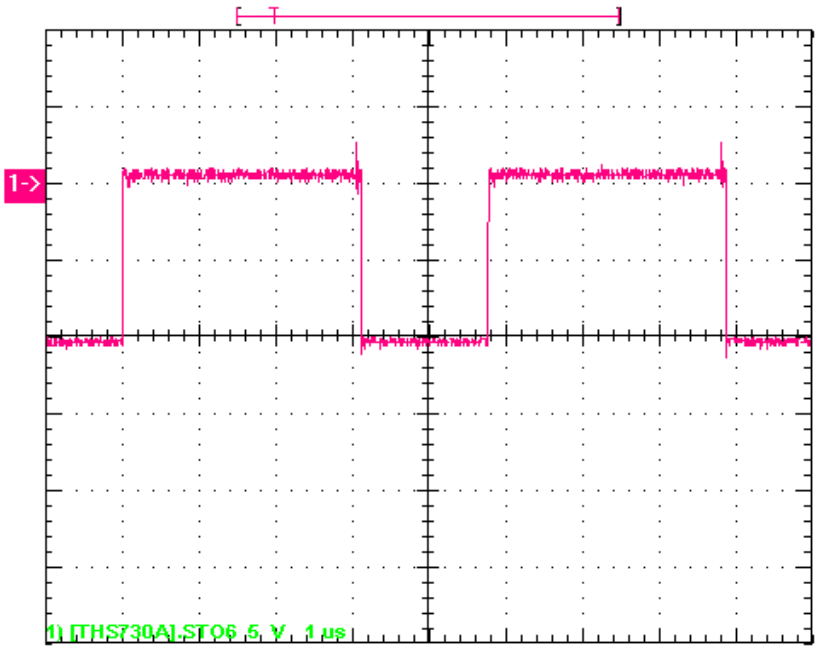


Ch1 =>
10V/div

1µs/div
full bandwidth

Figure 23

Figure 24 shows the Gate-Source voltage of the same FET



Ch1 =>
5V/div

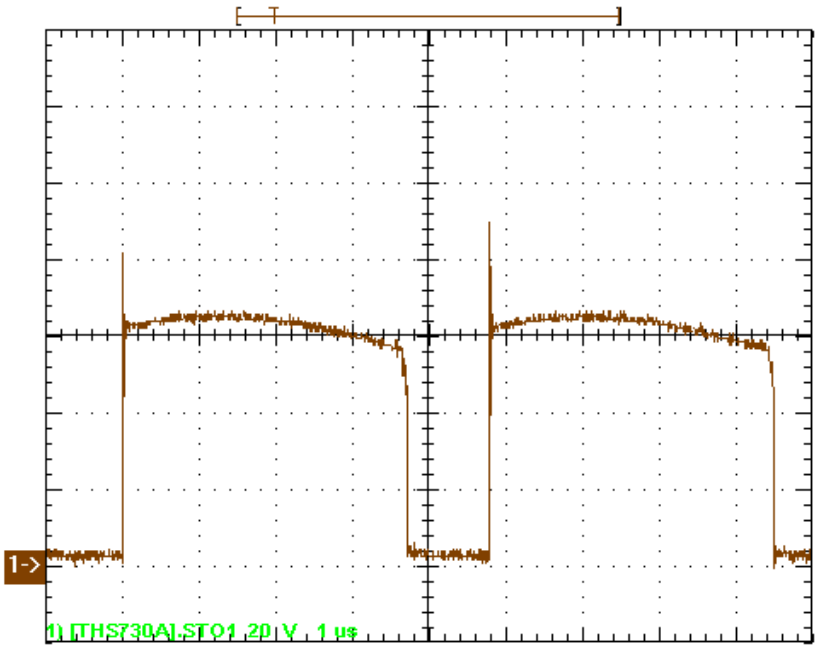
1µs/div
full bandwidth

Figure 24

10.2 48V input voltage

10.2.1 Primary FET (Q5)

With input voltage set to 48V results in the waveform shown in Figure 25 Output current was set to 20A.

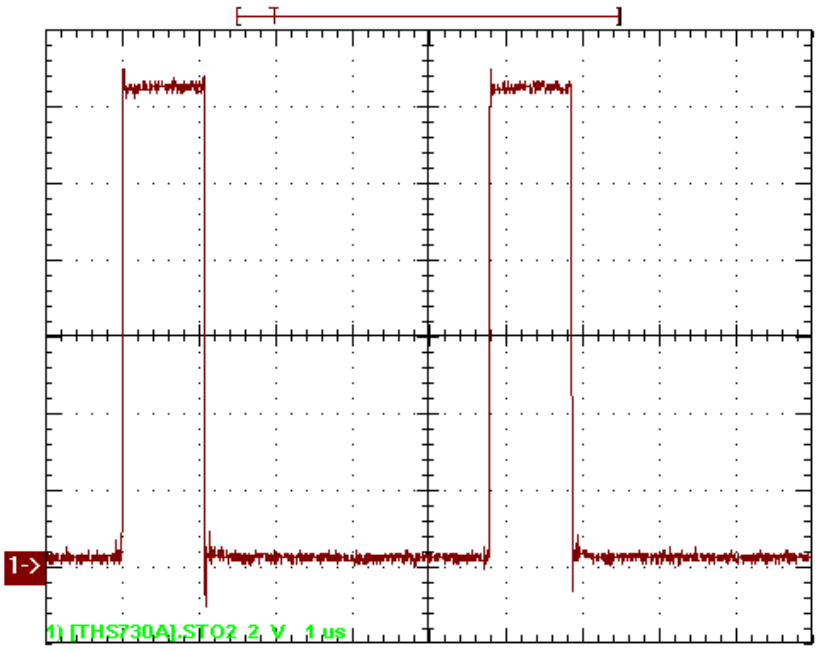


Ch1 =>
20V/div

1µs/div
full bandwidth

Figure 25

Figure 26 shows the Gate-Source voltage of the same FET



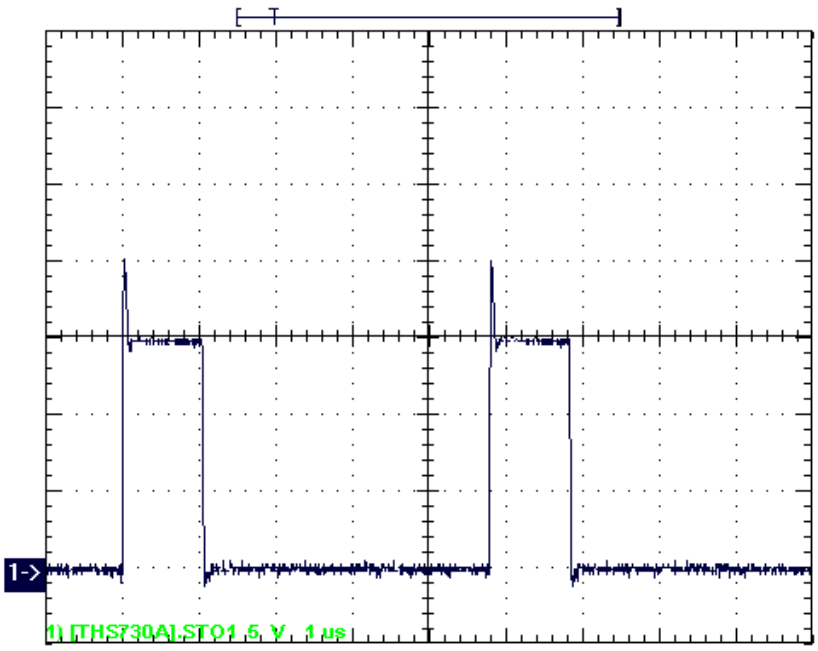
Ch1 =>
2V/div

1µs/div
full bandwidth

Figure 26

10.2.2 Freewheeling FET (Q2)

With input voltage set to 48V results in the waveform shown in Figure 27 Output current was set to 20A.

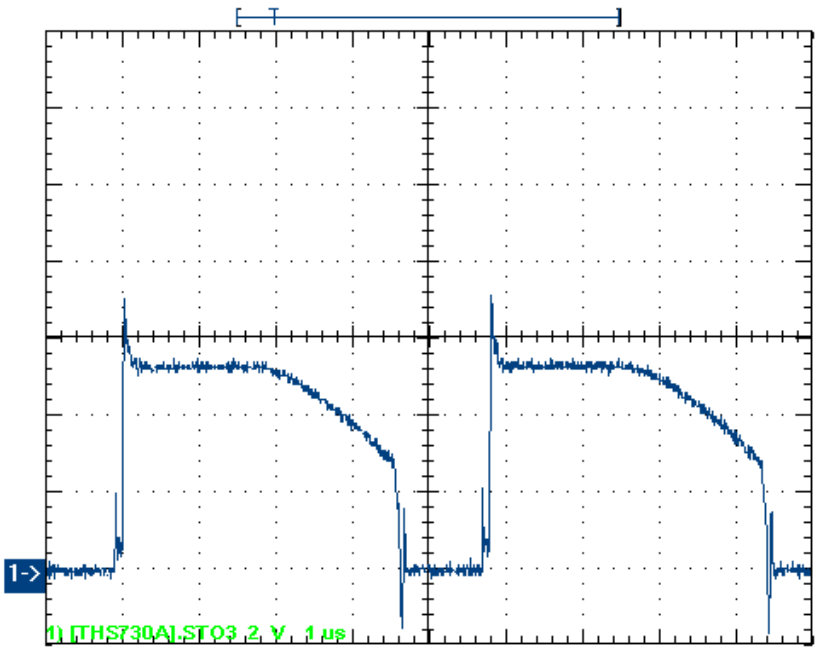


Ch1 =>
5V/div

1µs/div
full bandwidth

Figure 27

Figure 28 shows the Gate-Source voltage of the same FET



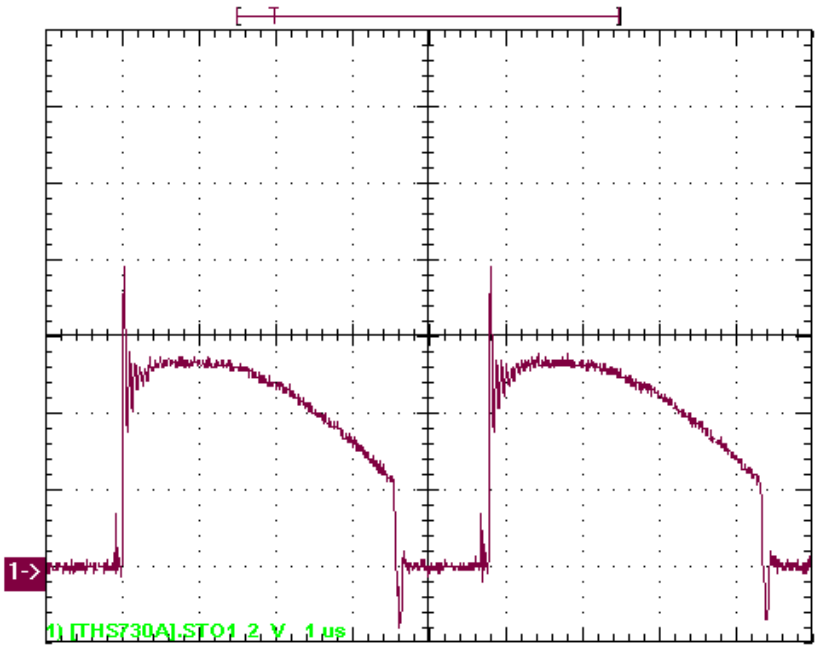
Ch1 =>
2V/div

1µs/div
full bandwidth

Figure 28

10.2.3 Synchronous Rectifier (Q6)

With input voltage set to 48V results in the waveform shown in Figure 29 Output current was set to 20A.

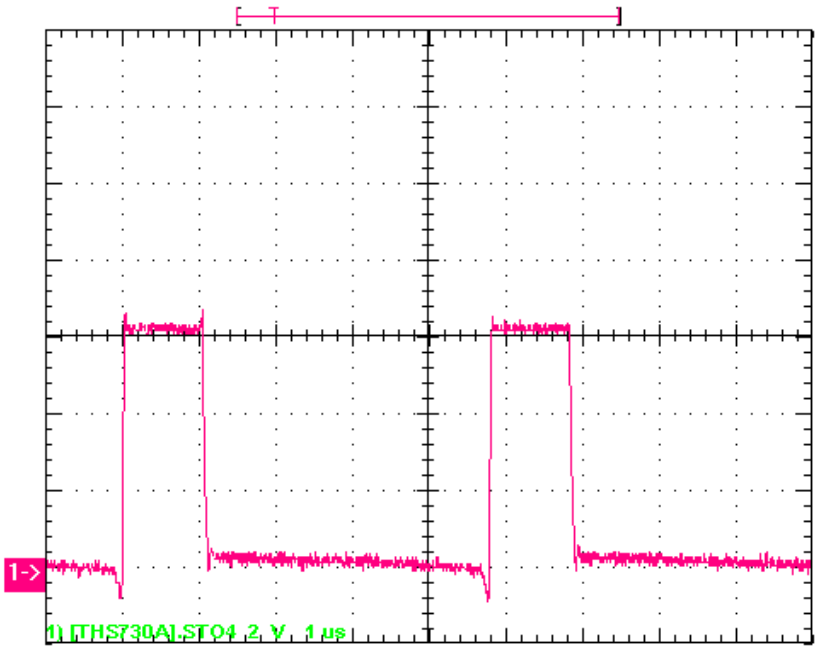


Ch1 =>
5V/div

1µs/div
full bandwidth

Figure 29

Figure 30 shows the Gate-Source voltage of the same FET



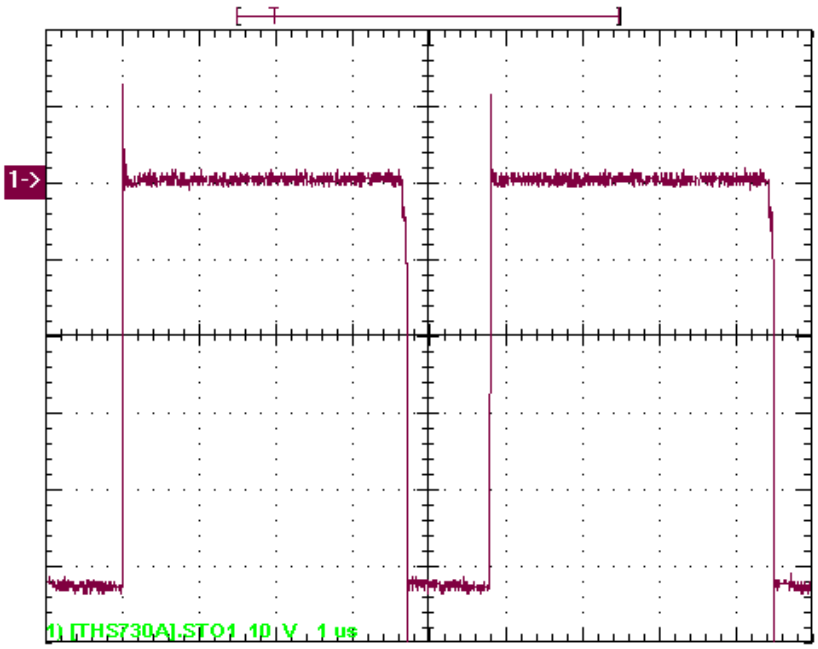
Ch1 =>
2V/div

1µs/div
full bandwidth

Figure 30

10.2.4 Active Clamp (Q4)

With input voltage set to 48V results in the waveform shown in Figure 31 Output current was set to 20A.

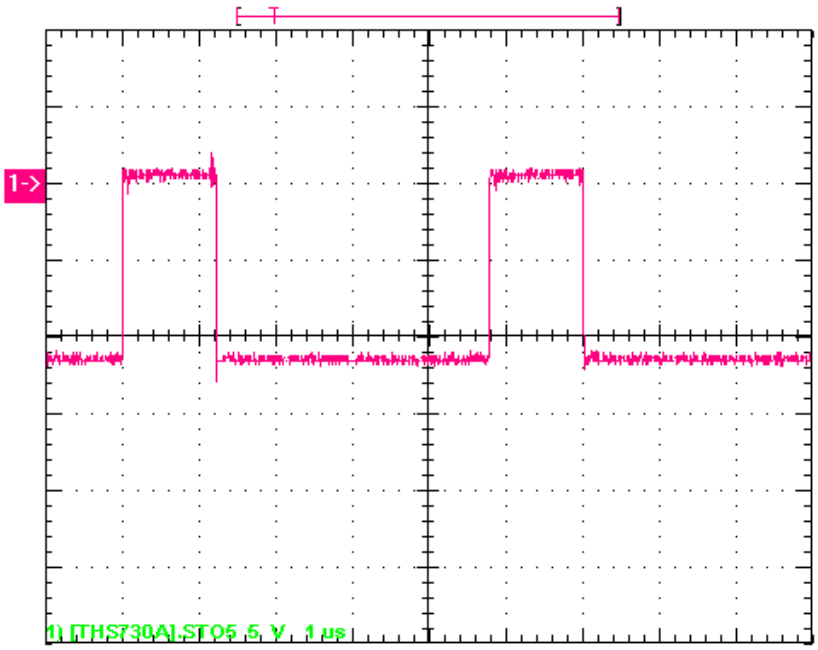


Ch1 =>
10V/div

1µs/div
full bandwidth

Figure 31

Figure 32 shows the Gate-Source voltage of the same FET



Ch1 =>
5V/div

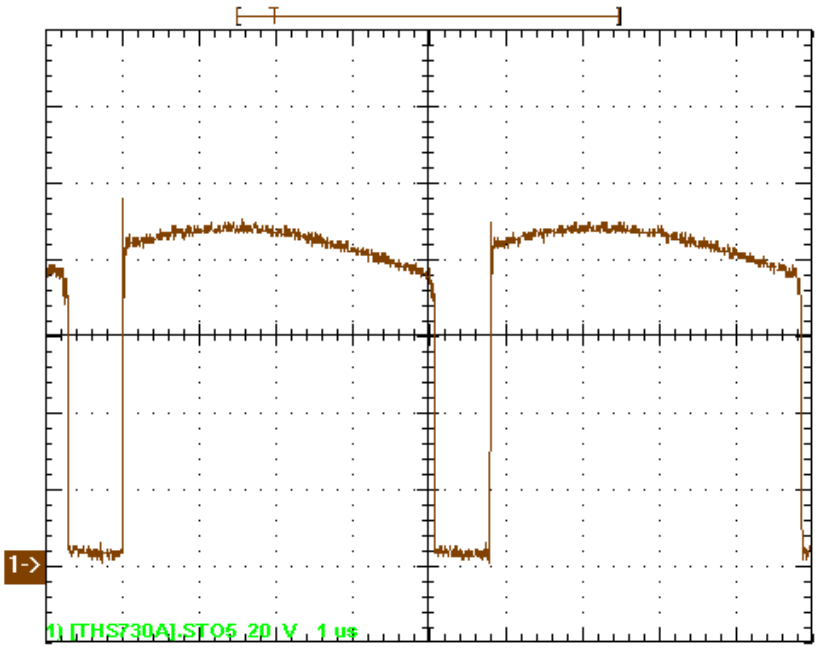
1µs/div
full bandwidth

Figure 32

10.3 72V input voltage

10.3.1 Primary FET (Q5)

With input voltage set to 72V results in the waveform shown in Figure 33 Output current was set to 20A.

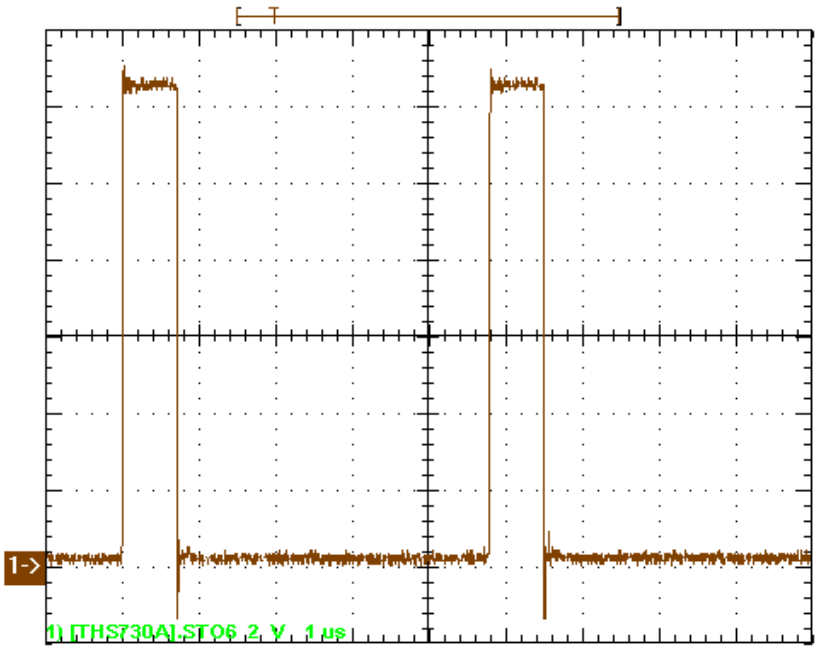


Ch1 =>
20V/div

1µs/div
full bandwidth

Figure 33

Figure 34 shows the Gate-Source voltage of the same FET



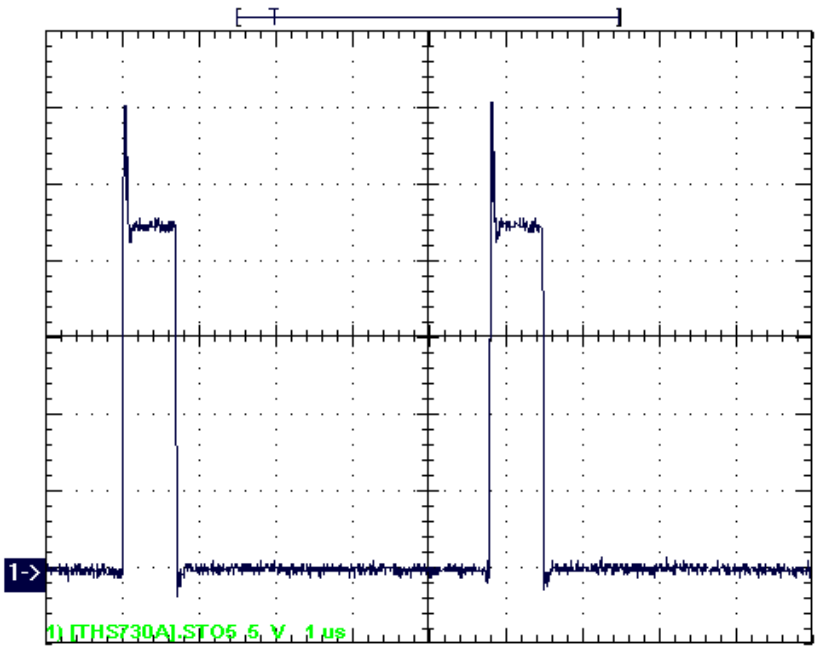
Ch1 =>
2V/div

1µs/div
full bandwidth

Figure 34

10.3.2 Freewheeling FET (Q2)

With input voltage set to 72V results in the waveform shown in Figure 35 Output current was set to 20A.

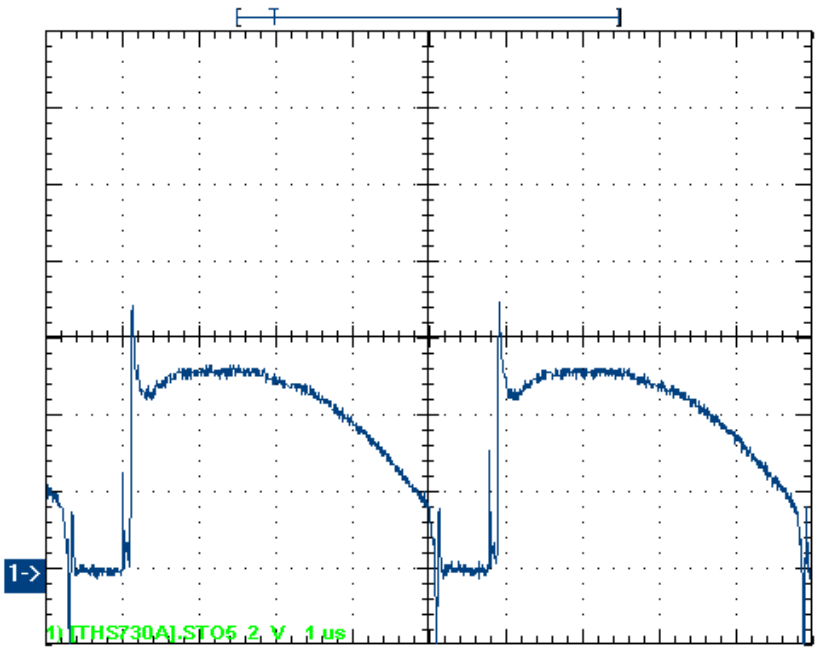


Ch1 =>
5V/div

1µs/div
full bandwidth

Figure 35

Figure 36 shows the Gate-Source voltage of the same FET



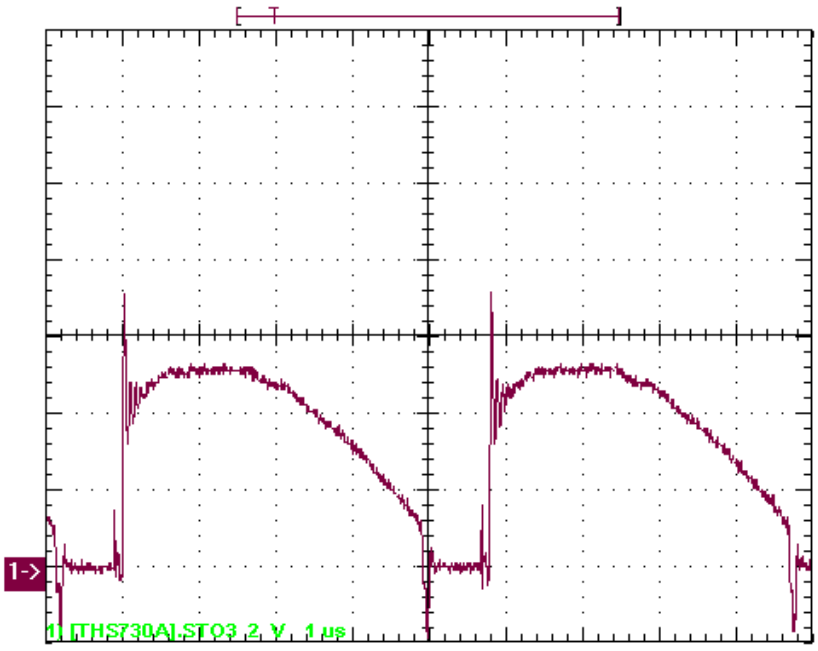
Ch1 =>
2V/div

1µs/div
full bandwidth

Figure 36

10.3.3 Synchronous Rectifier (Q6)

With input voltage set to 72V results in the waveform shown in Figure 37 Output current was set to 20A.

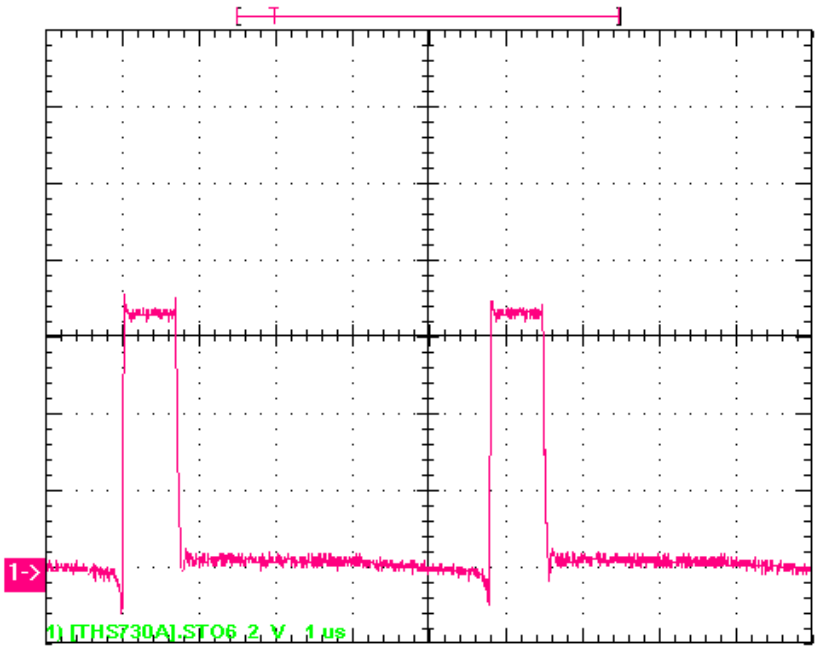


Ch1 => 2V/div

1µs/div full bandwidth

Figure 37

Figure 38 shows the Gate-Source voltage of the same FET



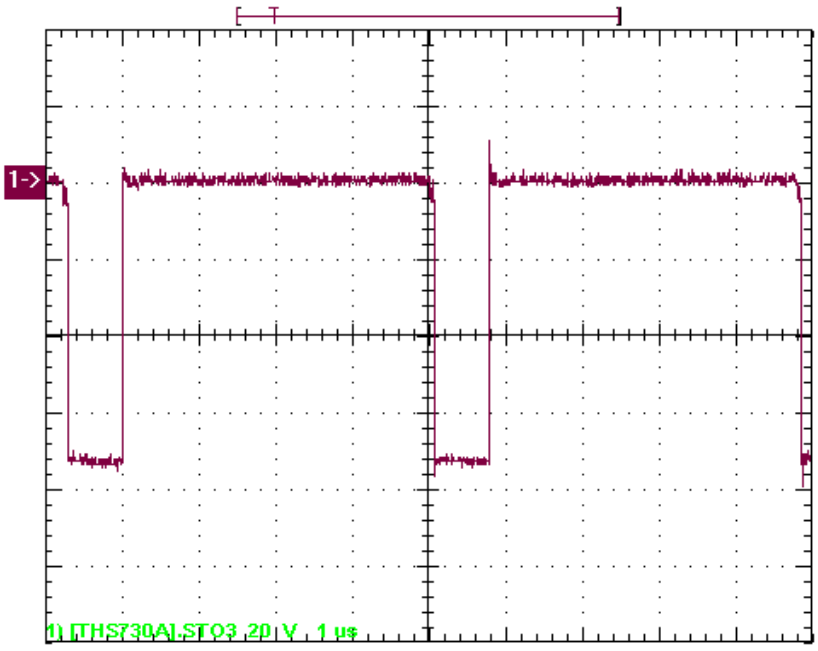
Ch1 => 2V/div

1µs/div full bandwidth

Figure 38

10.3.4 Active Clamp (Q4)

With input voltage set to 72V results in the waveform shown in Figure 39 Output current was set to 20A.

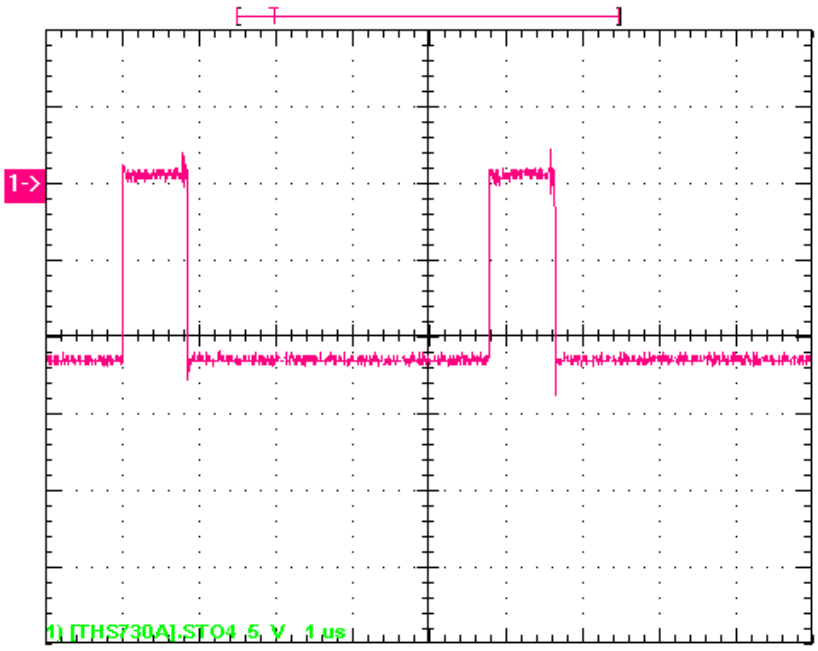


Ch1 =>
20V/div

1µs/div
full bandwidth

Figure 39

Figure 24 shows the Gate-Source voltage of the same FET



Ch1 =>
5V/div

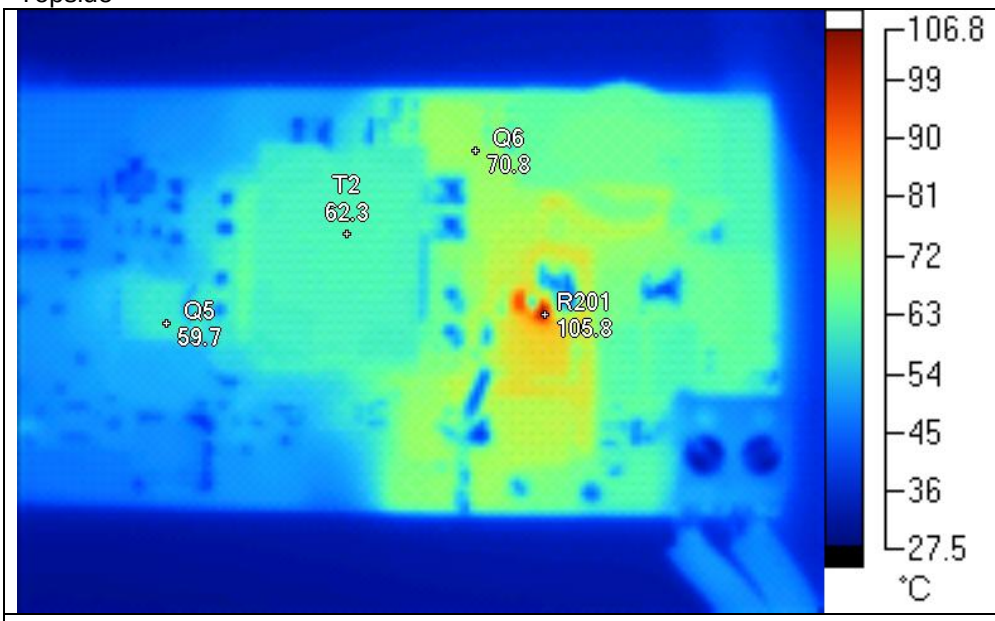
1µs/div
full bandwidth

Figure 40

11 Thermal Image

48V input and 15A output with no airflow, R201 of RC snubber covers overshoot

Topside



Name	Temperature
R201	105.8°C
Q5	59.7°C
Q6	70.8°C
T2	62.3°C

Figure 41

For Feasibility Evaluation Only, in Laboratory/Development Environments. The reference design is not a complete product. It is intended solely for use for preliminary feasibility evaluation in laboratory / development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical / mechanical components, systems and subsystems. It should not be used as all or part of a production unit.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the reference design for evaluation, testing and other purposes.
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