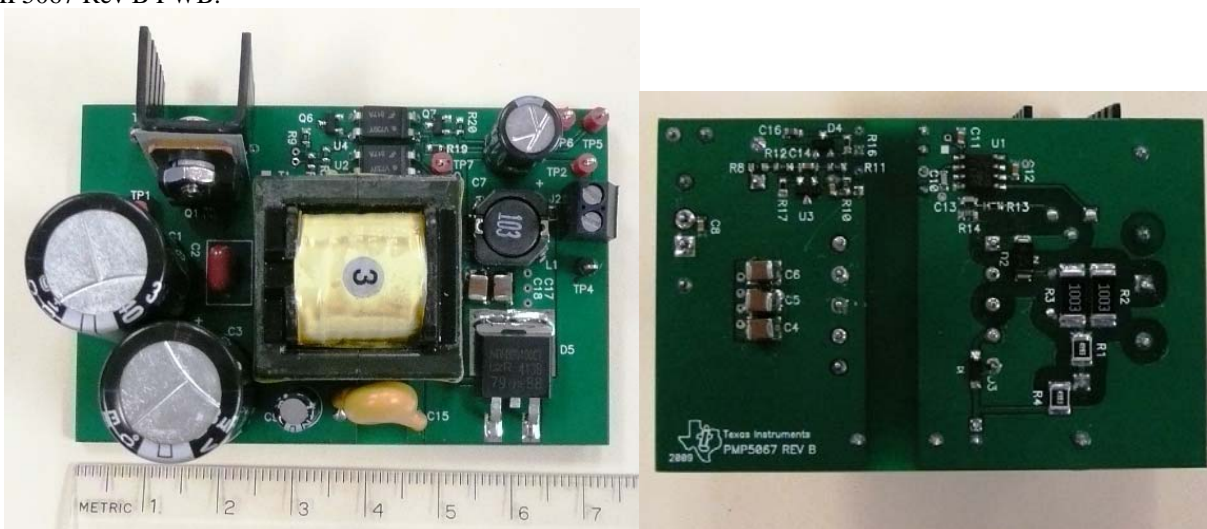


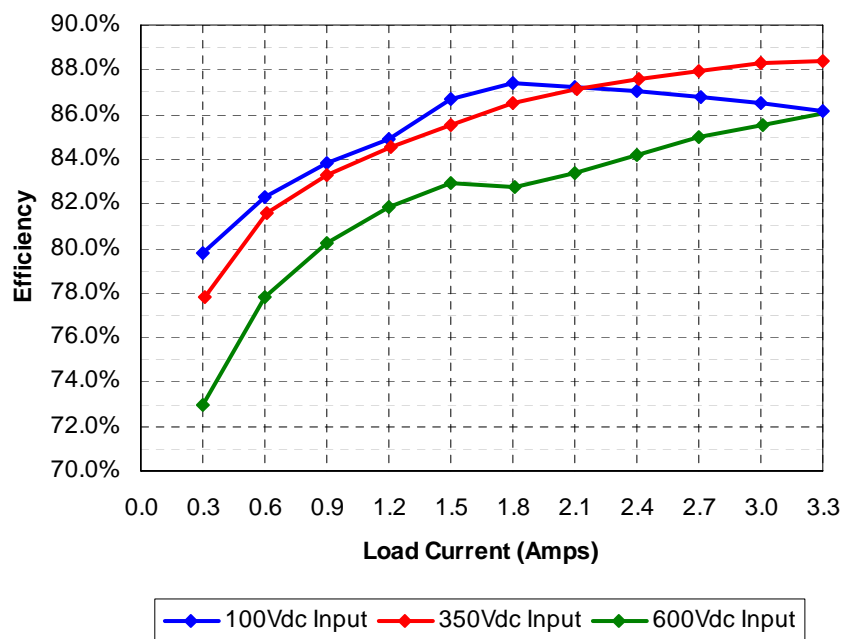
## 1 Photo

The photographs below show the top and bottom views of the PMP5067 Rev C demo board. The circuit is built on a PMP5067 Rev B PWB.



## 2 Efficiency

The efficiency data is shown in the tables and graph below.



**100Vdc**

Iout	Vout	Vin (Vdc)	Iin (mA)	Pin	Pout	Losses	Efficiency
0.300	12.01	99.9	45.2	4.52	3.60	0.91	79.8%
0.601	12.01	100.9	86.9	8.77	7.22	1.55	82.3%
0.899	12.01	100.8	127.8	12.88	10.80	2.09	83.8%
1.201	12.01	100.7	168.7	16.99	14.42	2.56	84.9%
1.502	12.00	100.6	206.6	20.78	18.02	2.76	86.7%
1.800	12.00	100.5	245.9	24.71	21.60	3.11	87.4%
2.100	12.00	100.5	287.4	28.88	25.20	3.68	87.2%
2.403	12.00	100.4	330.1	33.14	28.84	4.31	87.0%
2.710	12.00	100.3	373.7	37.48	32.52	4.96	86.8%
3.004	12.00	100.9	413	41.67	36.05	5.62	86.5%
3.304	12.00	100.9	456	46.01	39.65	6.36	86.2%

**350Vdc**

Iout	Vout	Vin (Vdc)	Iin (mA)	Pin	Pout	Losses	Efficiency
0.306	12.01	353.3	13.37	4.72	3.68	1.05	77.8%
0.607	12.01	353.3	25.30	8.94	7.29	1.65	81.6%
0.900	12.01	353.3	36.72	12.97	10.81	2.16	83.3%
1.206	12.01	353.3	48.5	17.14	14.48	2.65	84.5%
1.501	12.01	353.2	59.7	21.09	18.03	3.06	85.5%
1.798	12.00	353.2	70.6	24.94	21.58	3.36	86.5%
2.108	12.00	353.2	82.2	29.03	25.30	3.74	87.1%
2.405	12.00	353.2	93.3	32.95	28.86	4.09	87.6%
2.701	12.00	353.1	104.4	36.86	32.41	4.45	87.9%
3.004	12.00	353.1	115.6	40.82	36.05	4.77	88.3%
3.302	12.00	353.1	126.9	44.81	39.62	5.18	88.4%

**600Vdc**

Iout	Vout	Vin (Vdc)	Iin (mA)	Pin	Pout	Losses	Efficiency
0.304	12.01	600.2	8.34	5.01	3.65	1.35	72.9%
0.603	12.01	600.2	15.51	9.31	7.24	2.07	77.8%
0.896	12.01	600.2	22.36	13.42	10.76	2.66	80.2%
1.197	12.01	600.2	29.27	17.57	14.38	3.19	81.8%
1.496	12.01	600.2	36.10	21.67	17.97	3.70	82.9%
1.805	12.00	600.2	43.6	26.17	21.66	4.51	82.8%
2.102	12.00	600.2	50.4	30.25	25.22	5.03	83.4%
2.399	12.00	600.1	57.0	34.21	28.79	5.42	84.2%
2.698	12.00	600.1	63.5	38.11	32.38	5.73	85.0%
3.007	12.00	600.1	70.3	42.19	36.08	6.10	85.5%
3.308	12.00	600.1	76.9	46.15	39.70	6.45	86.0%

### 3 Standby Mode Power Consumption

The tables below show the input power and efficiency during light load operation.

**100Vdc**

Iout	Vout	Vin (Vdc)	Iin (mA)	Pin (mW)	Pout (mW)	Losses	Efficiency
0.000	12.04	101.3	1.74	176	0	176	0.0%
0.024	12.02	101.3	4.93	499	288	211	57.8%
0.049	12.02	101.3	8.55	866	589	277	68.0%

**350Vdc**

Iout	Vout	Vin (Vdc)	Iin (mA)	Pin (mW)	Pout (mW)	Losses	Efficiency
0.000	12.03	352.4	0.82	289	0	289	0.0%
0.025	12.01	352.4	1.79	631	300	331	47.6%
0.049	12.01	352.4	2.75	969	588	381	60.7%

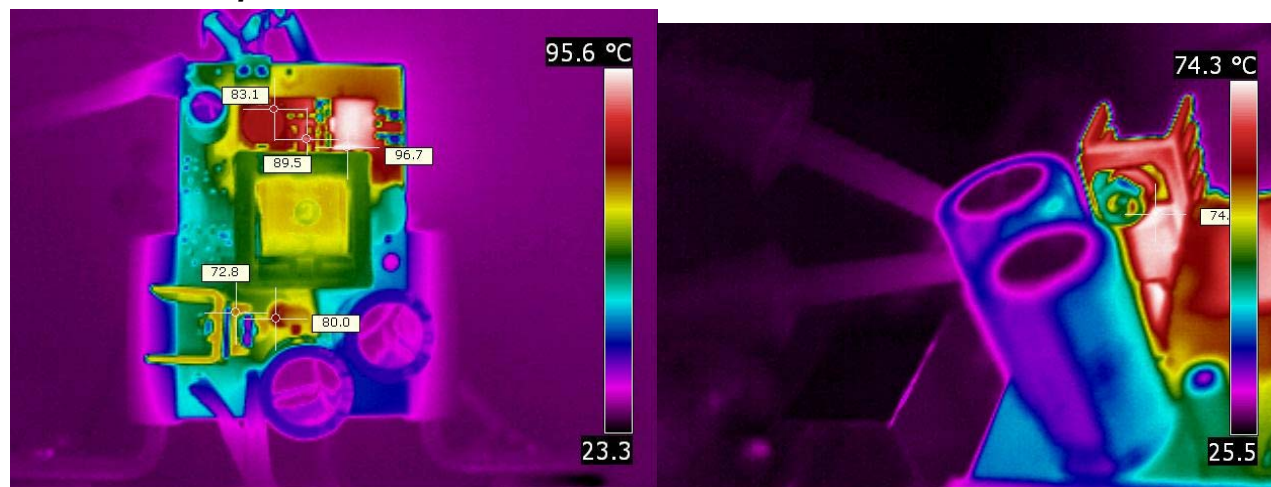
**600Vdc**

Iout	Vout	Vin (Vdc)	Iin (mA)	Pin (mW)	Pout (mW)	Losses	Efficiency
0.000	12.02	600.2	0.89	534	0	534	0.0%
0.025	12.01	600.2	1.47	882	300	582	34.0%
0.049	12.01	600.3	2.10	1261	588	672	46.7%

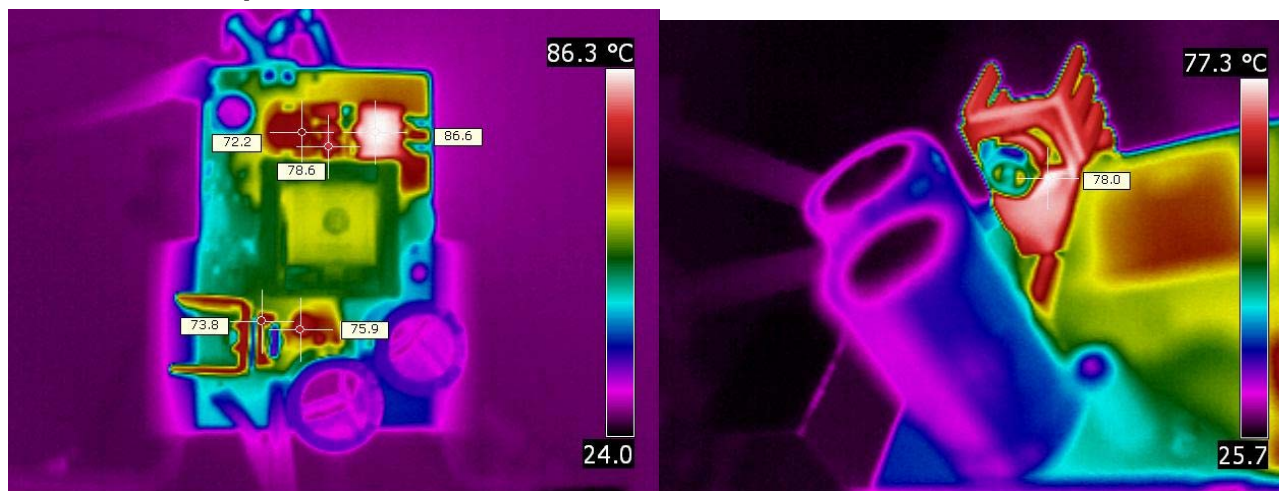
## 4 Thermal Images

The thermal images below show a top view (left) of the board and close up view (right) of the main FET (Q1). The ambient temperature was 26°C with no forced air flow. The output was loaded with 3.3A.

### 4.1 100VDC Input

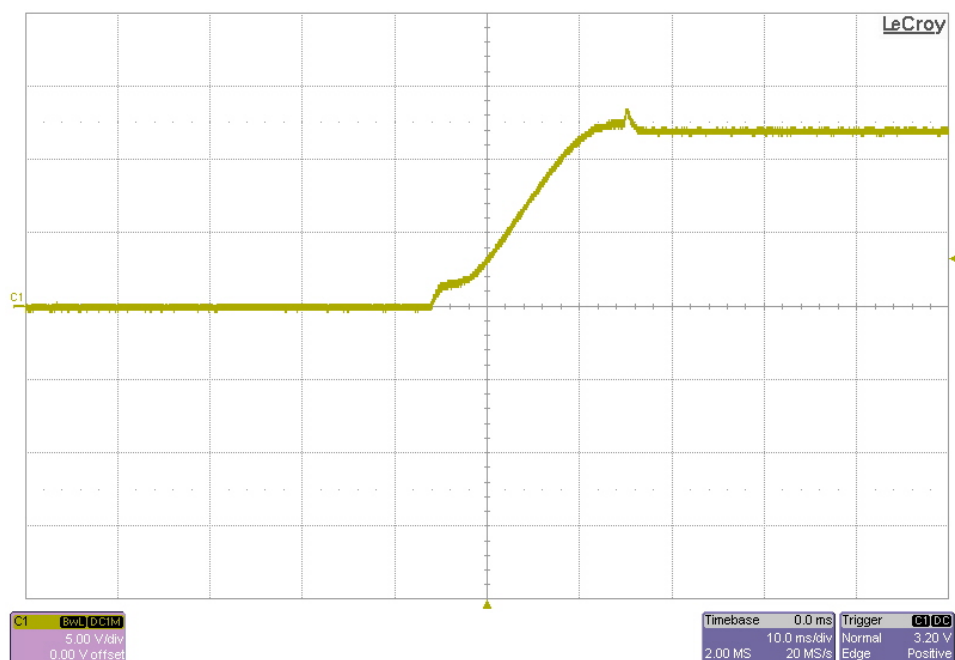
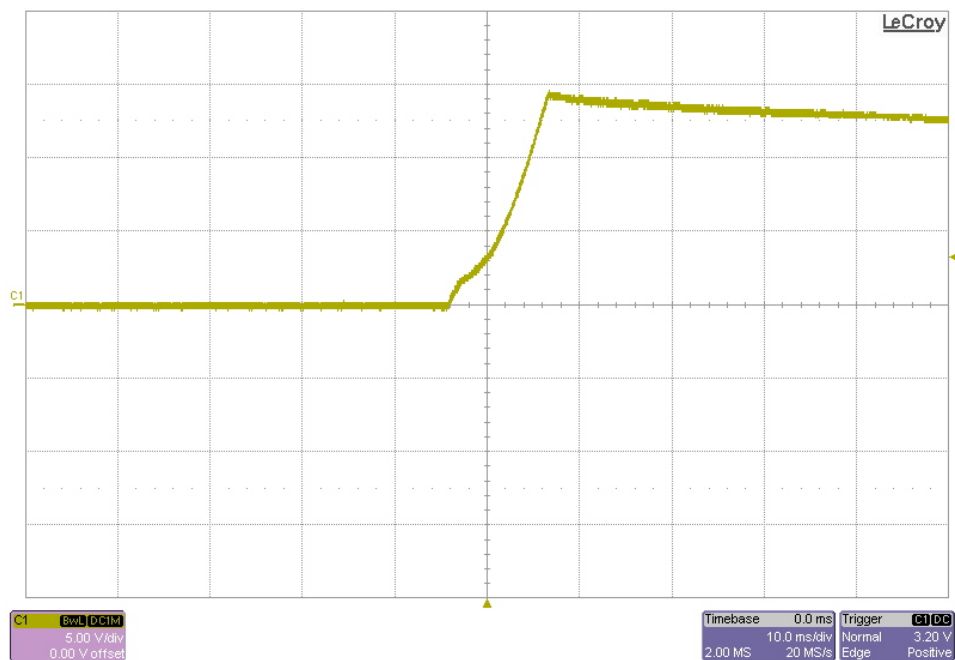


### 4.2 600VDC Input



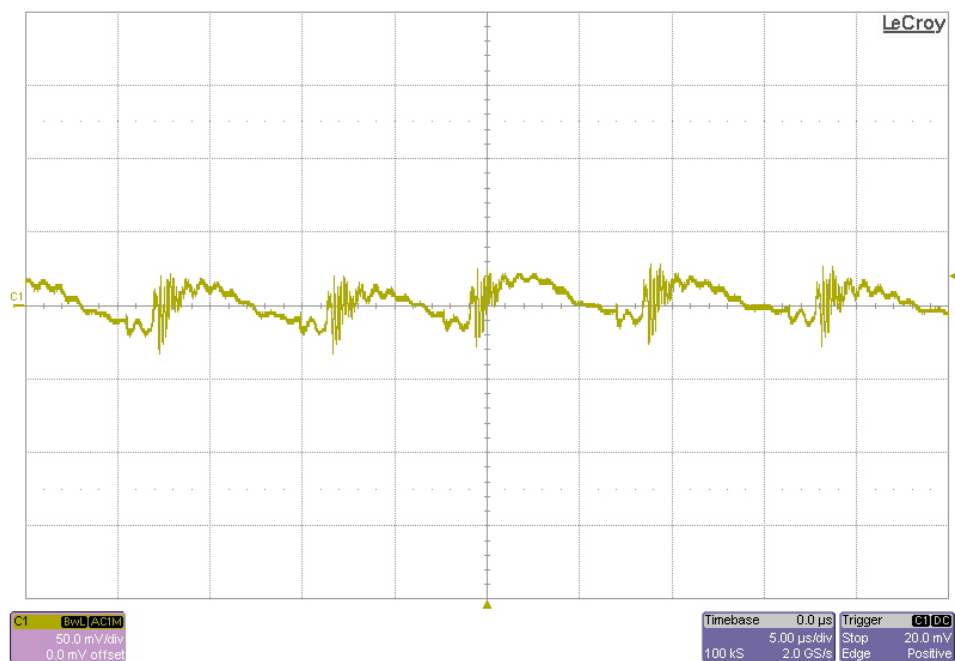
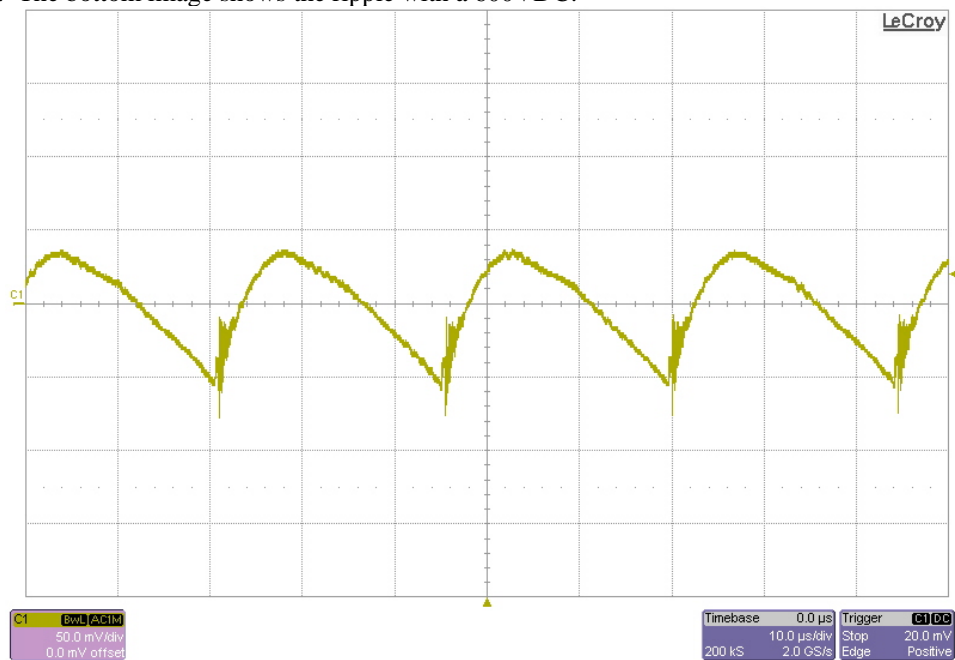
## 5 Startup

The output voltage at startup is shown in the images below. The input was 350VDC. For the top image, the output was unloaded. For the bottom image, the output was loaded with 3.3A.

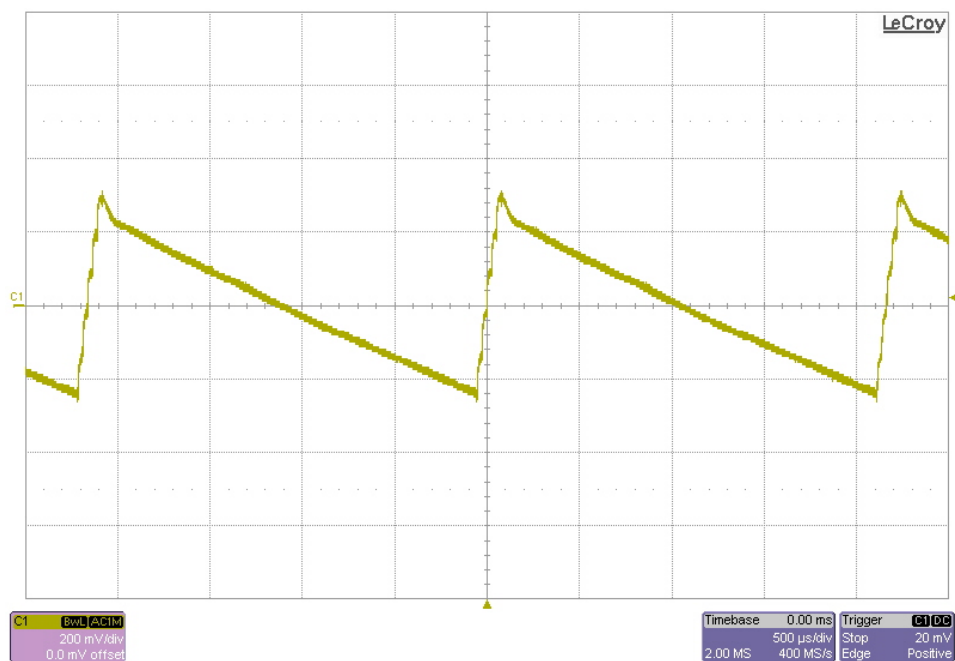
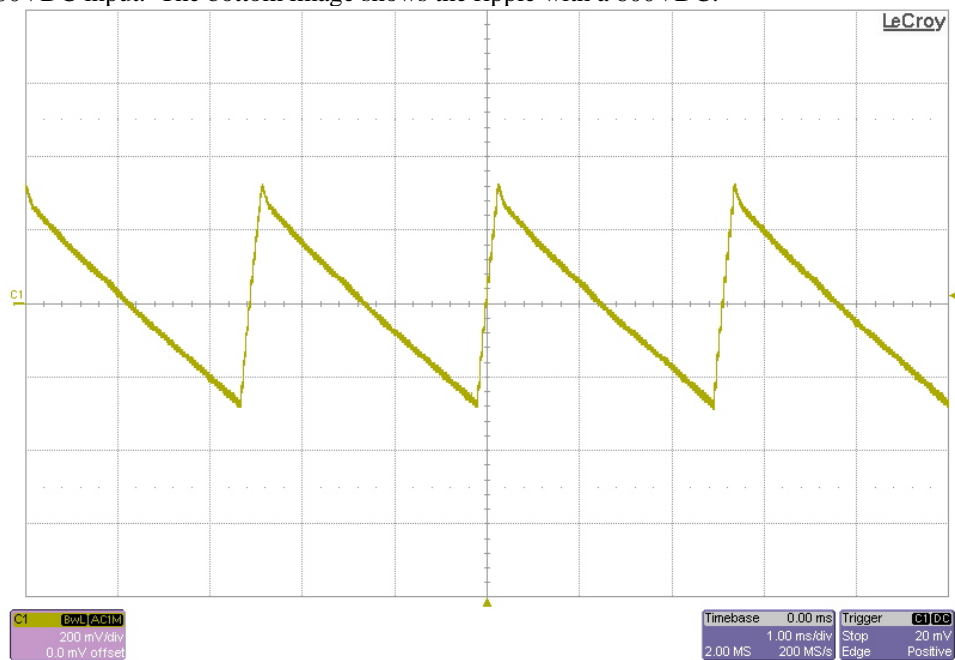


## 6 Output Ripple Voltage – Full Load

The output ripple voltage during full load operation is shown in the plots below. The top image shows the ripple with a 100VDC input. The bottom image shows the ripple with a 600VDC.



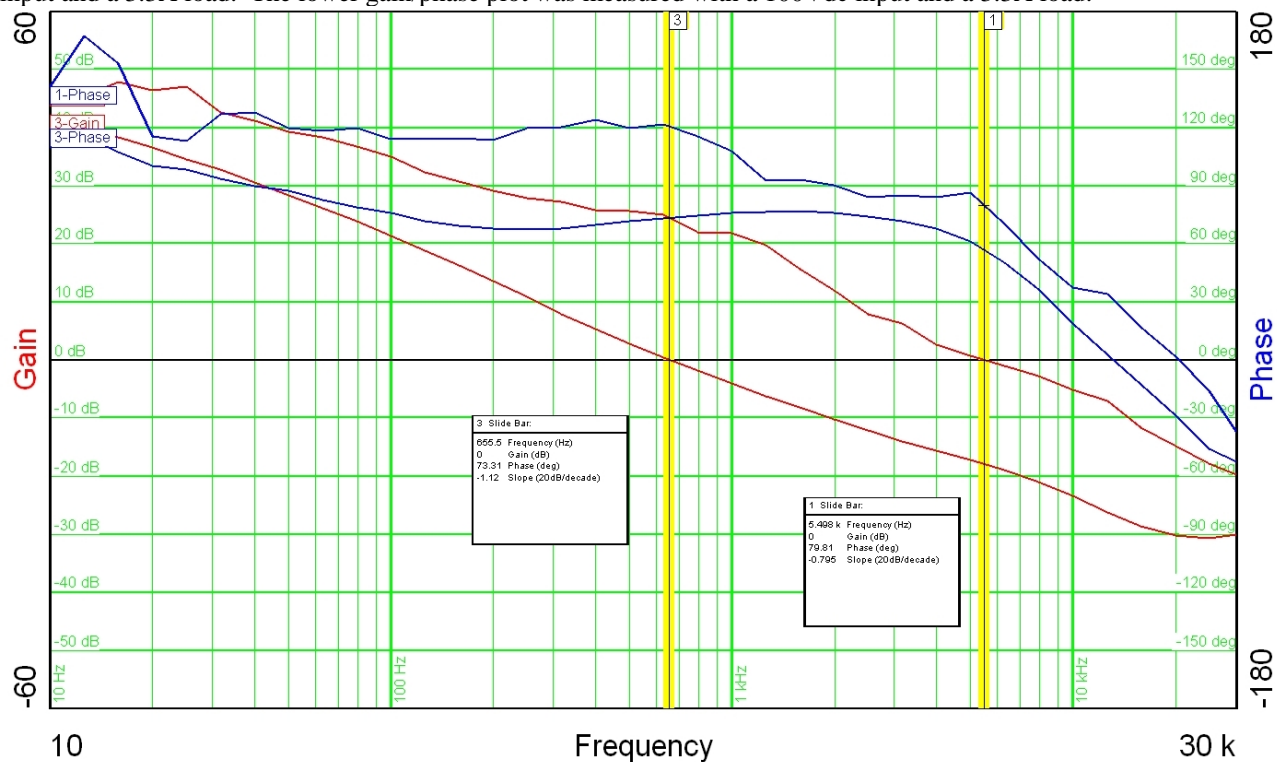
The output ripple voltage during light load operation (100mA) is shown in the plots below. The top image shows the ripple with a 100VDC input. The bottom image shows the ripple with a 600VDC.





## 8 Loop Response

The image below shows the loop response of the converter. The upper gain/phase plot was measured with a 600Vdc input and a 3.3A load. The lower gain/phase plot was measured with a 100Vdc input and a 3.3A load.

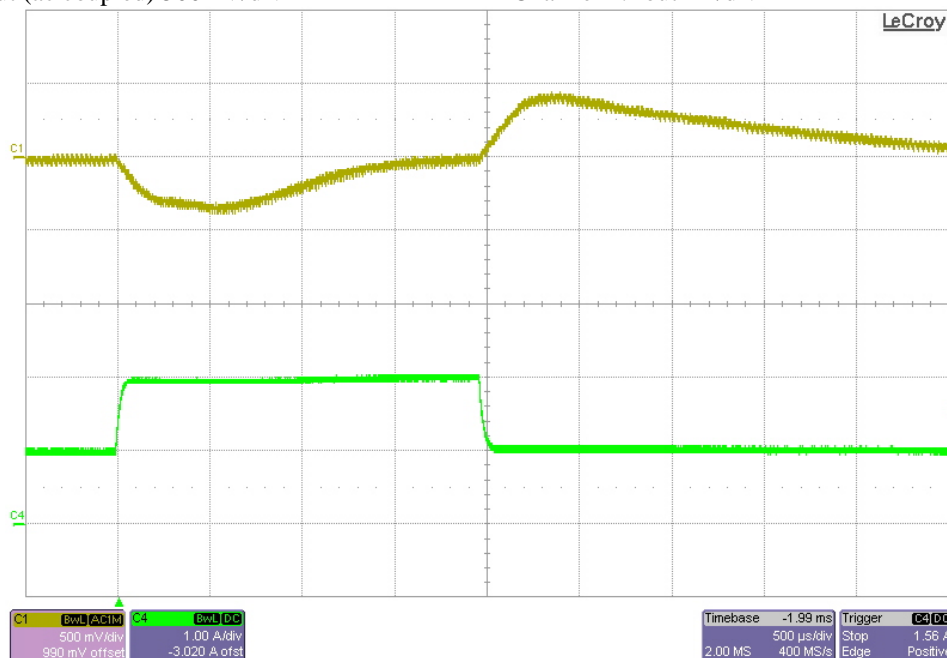


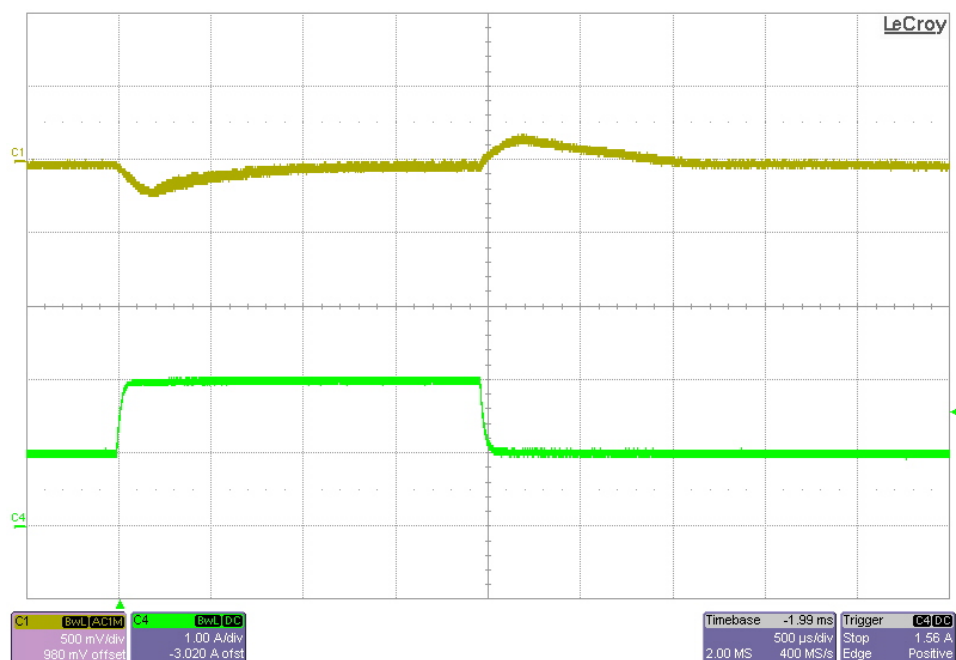
## 9 Load Transients

The images below show the response to a 1A to 2A load transient. For the top image, the input voltage was set to 100VDC. For the bottom image, the input was set to 600VDC.

Channel 1: Vout (ac coupled) 500mV/div

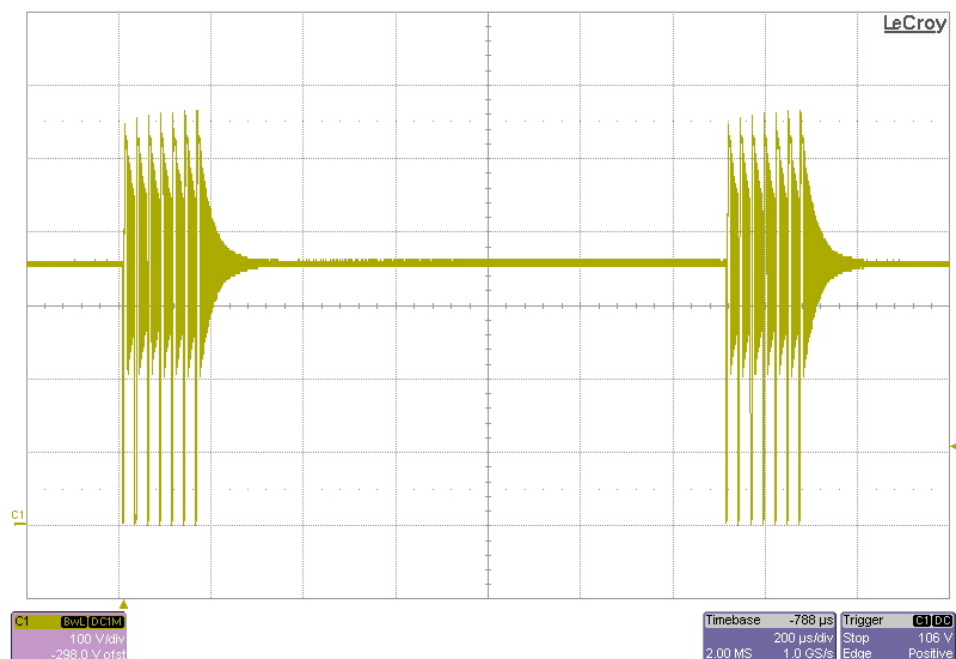
Channel 4: Iout 1A/div



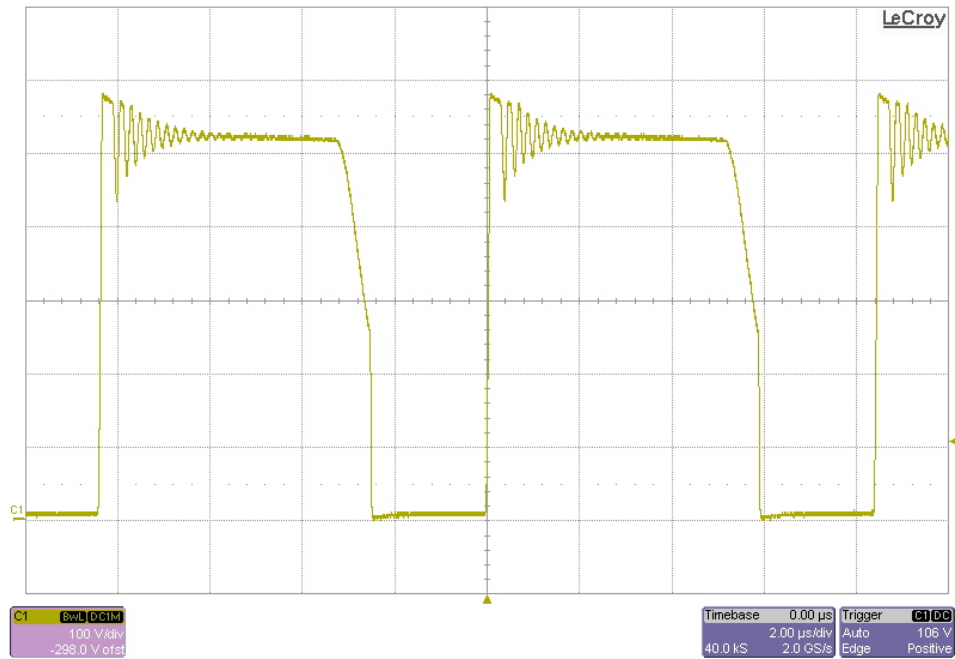


## 10 Switching Waveforms

The images below show the drain-to-source voltage waveform on the primary MOSFET (Q1). The top image demonstrates burst mode operation, where the load was 200mA and the input was set to 350VDC. In the bottom image, the load was 3.3A and the input was 350VDC.







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