PMP7051RevC Test Results

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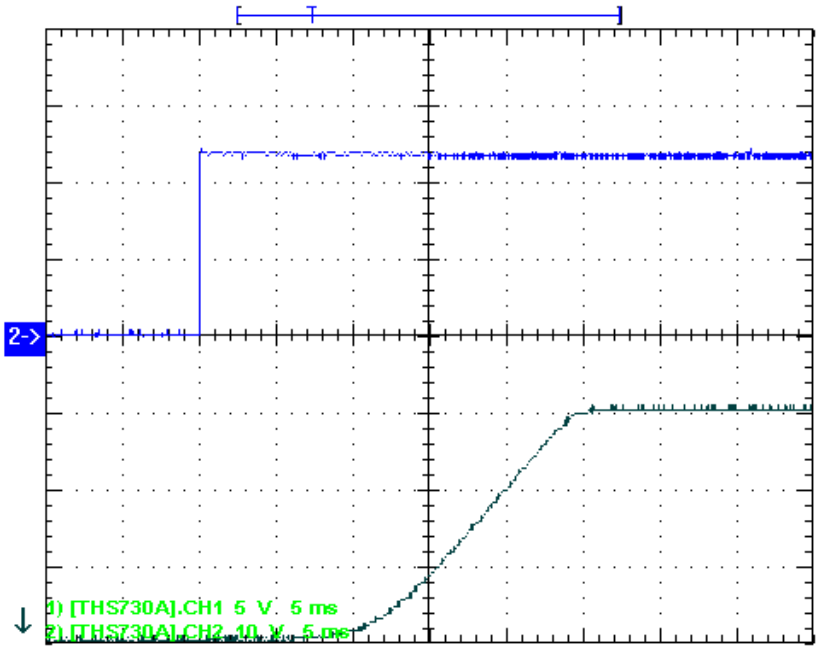
topology: buck

device: TPS40055

1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set to 24V, with 10A load at the output.



Ch2=> input voltage 10V/div

Ch1=> output voltage 5V/div

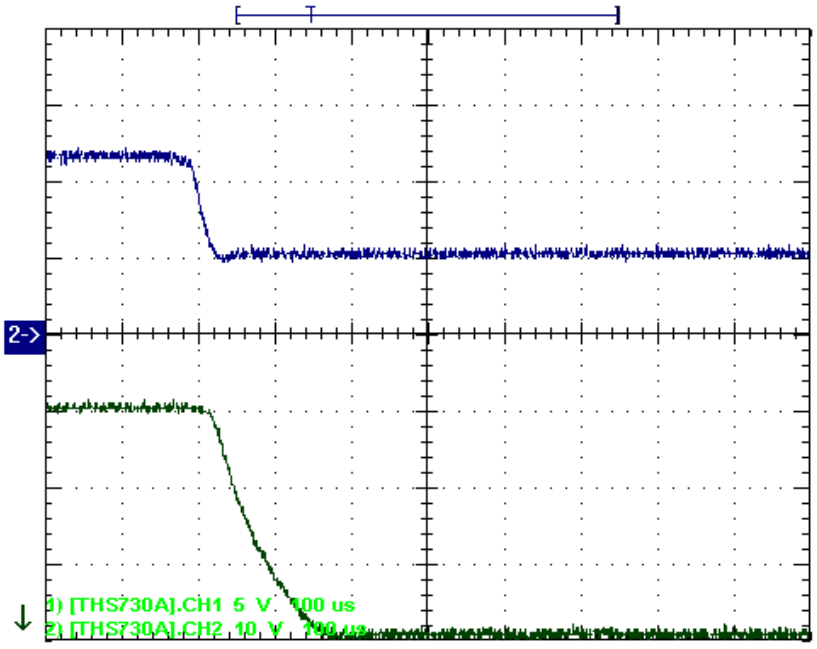
5ms/div

20MHz bandwidth

Figure 1

2 Shutdown

The shutdown waveform is shown in the Figure 2 to 24V input voltage. With 10A load applied at the output.



Ch2=> input voltage 10V/div

Ch1=> output voltage 5V/div

100µs/div

20MHz bandwidth

Figure 2

3 Efficiency

The efficiency is shown in the Figure 3 below. The input voltage was adjusted to 24V

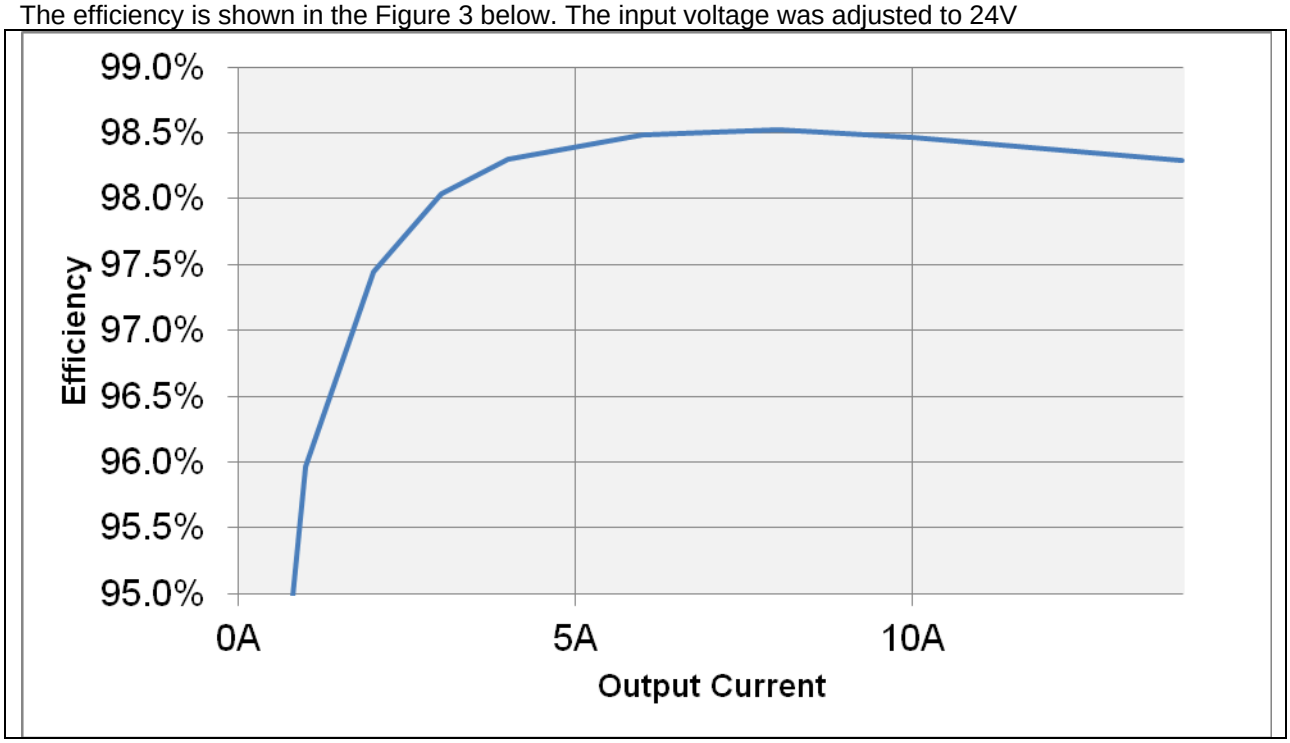


Figure 3

4 Load regulation

The load regulation for 24V input voltage is shown in Figure 4.

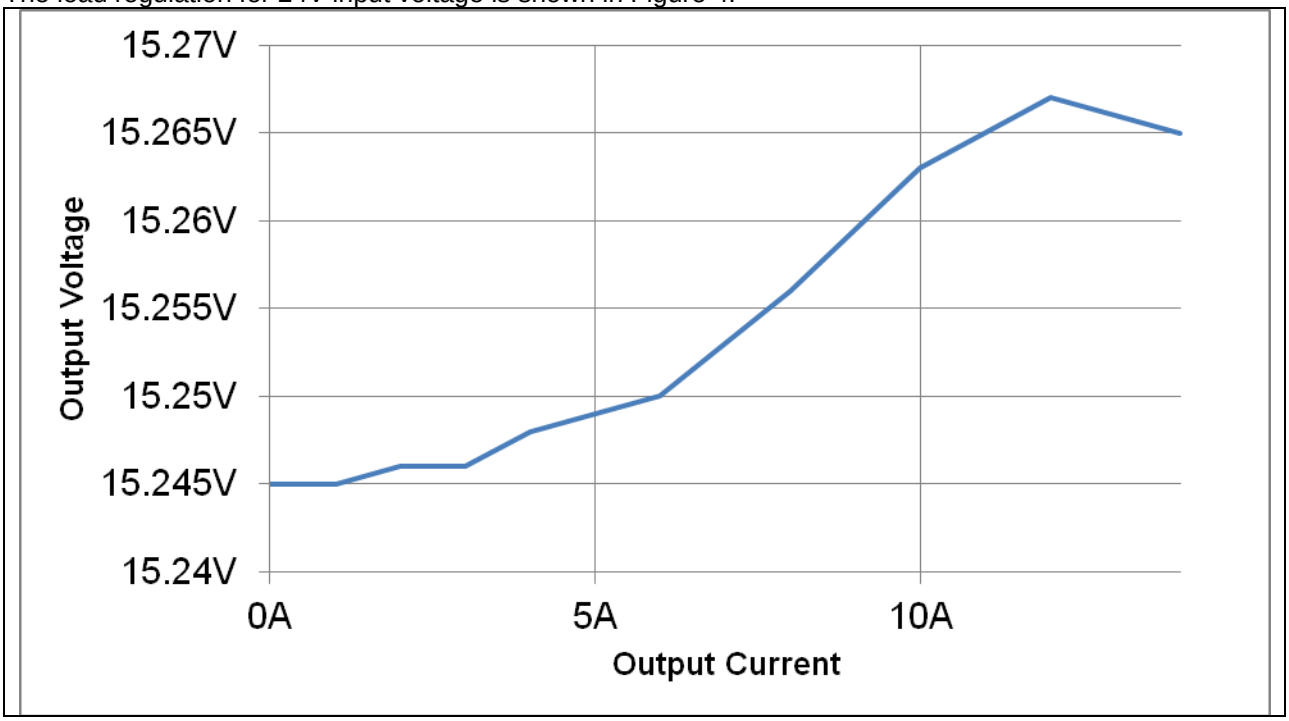


Figure 4

5 Control Loop Frequency Response

Figure 5 shows the loop response. 1A-load applied. The input voltage was set to 24V.

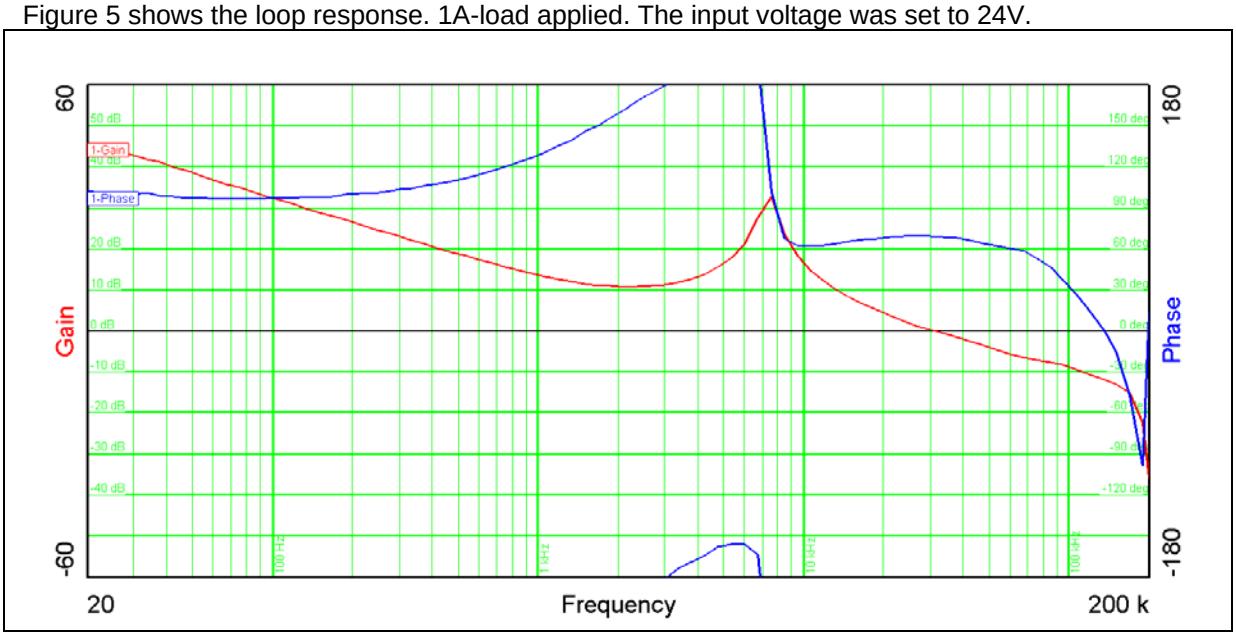


Figure 5

Table 1 summarizes the results from Figure 5

Vin	24V
Bandwidth (kHz)	31.2
Phase margin	69°
slope (20dB/decade)	-1.02
gain margin (dB)	-12
slope (20dB/decade)	-0.88
freq (kHz)	135.8

Table 1

6 Switch Node Waveform (Low Side FET)

With 10A load results in the waveforms shown in Figure 6 and Figure 7. 24V were applied to the input.

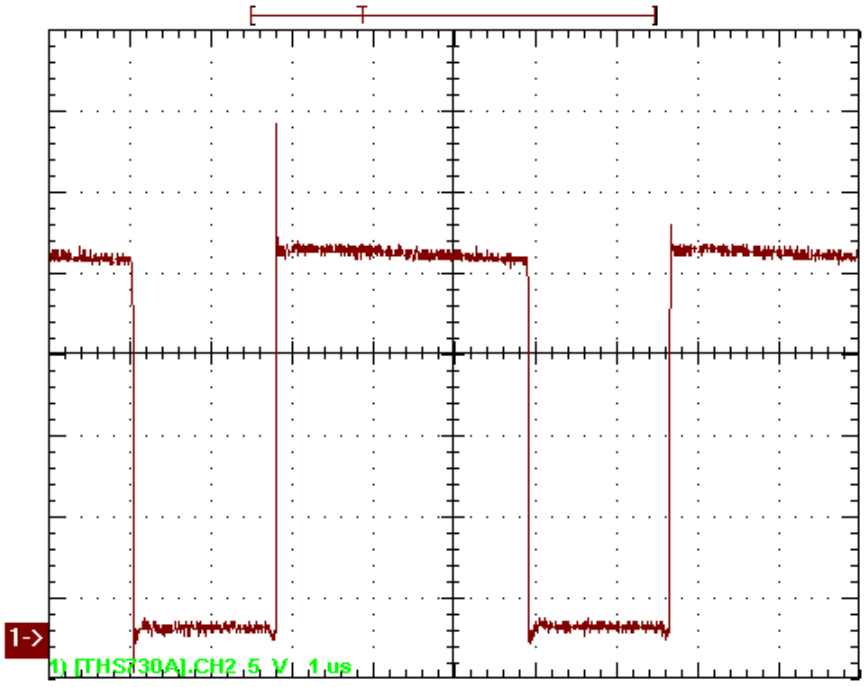
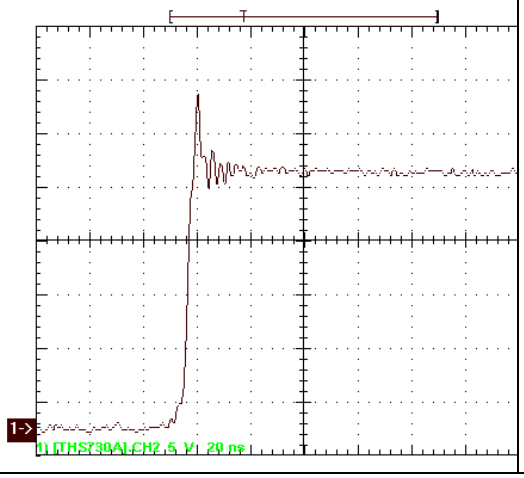


Figure 6

Ch1 => switchnode
5V/div

1µs/div

full bandwidth



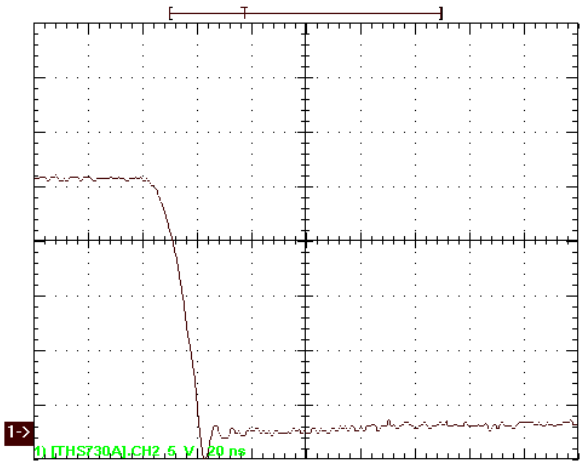


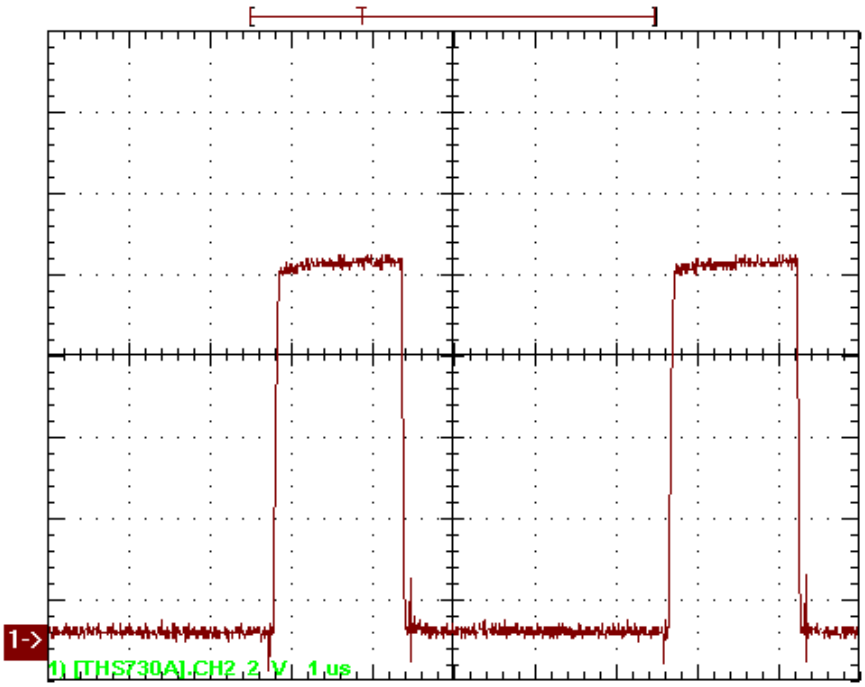
Figure 7

Ch1 => switchnode
5V/div

20ns/div

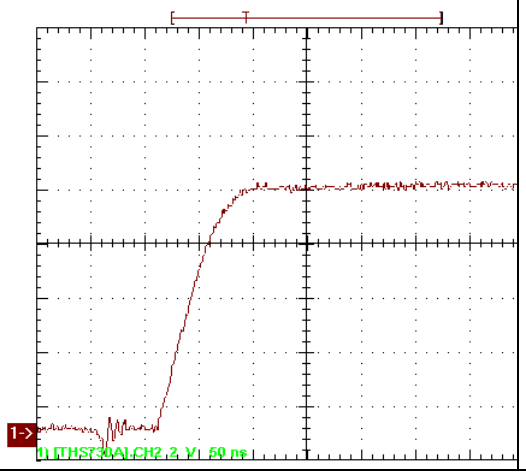
full bandwidth

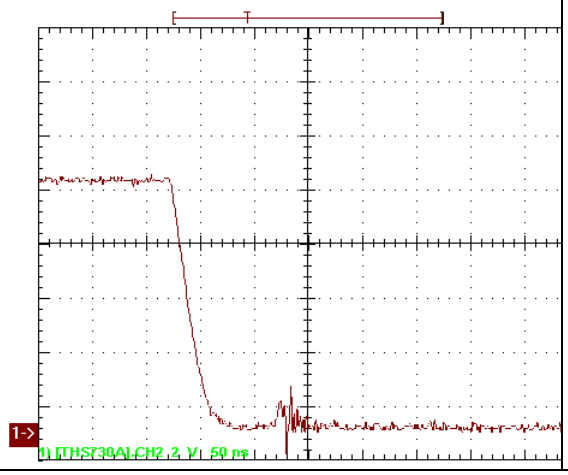
Figure 8 shows the waveform at the gate (to gnd)



Ch1 => gate-gnd
2V/div

1µs/div
full bandwidth





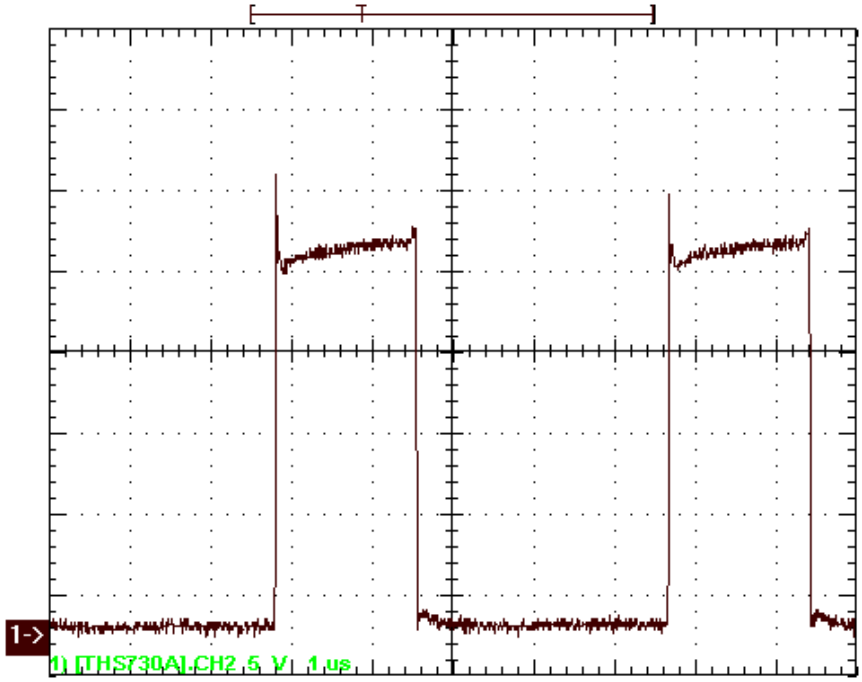
Ch1 => gate-gnd
2V/div

50ns/div
full bandwidth

Figure 8

7 Waveform at the High Side FET

With 10A load results in the waveforms (Vin to switch node) shown in Figure 9 and Figure 10. 24V were applied to the input.

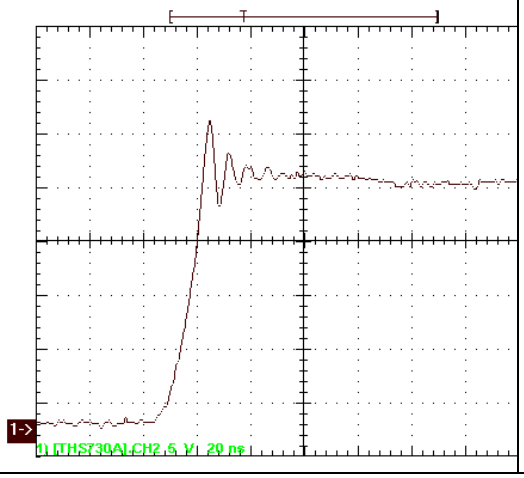


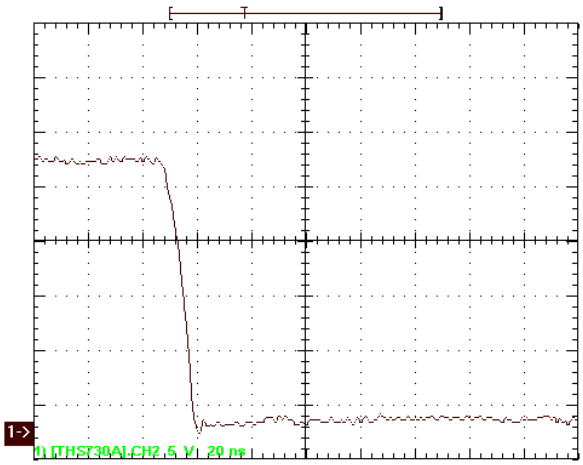
Ch1 => Vin to switchnode
5V/div

1µs/div

full bandwidth

Figure 9





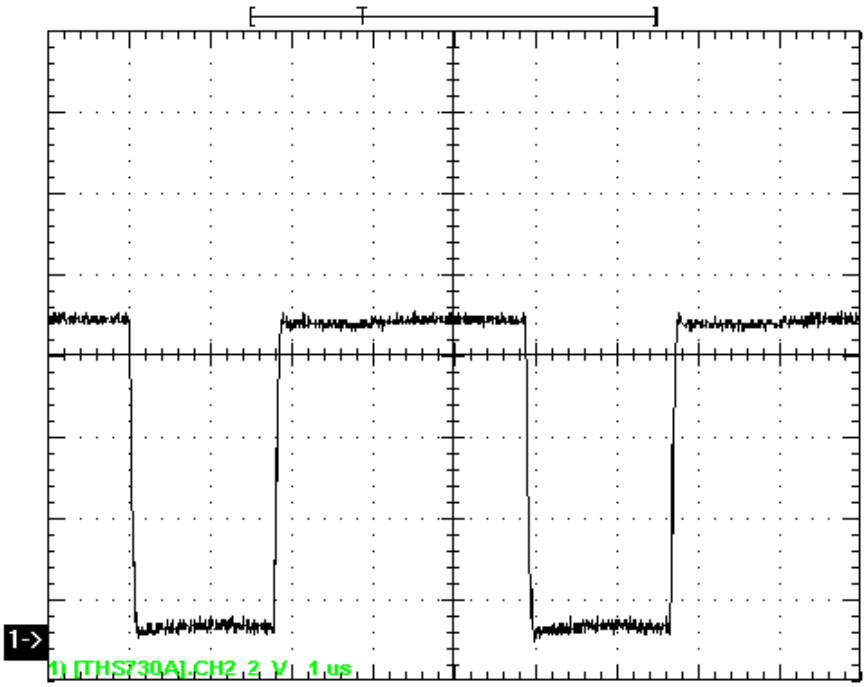
Ch1 => switchnode
10V/div

20ns/div

full bandwidth

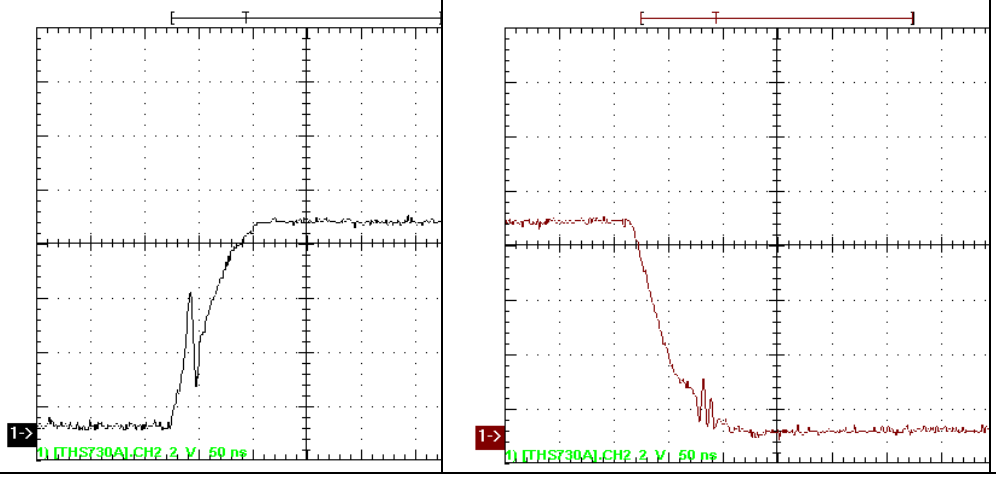
Figure 10

Figure 11 shows the waveform at the gate (to gnd) at the same input voltage



Ch1 => gate-source
2V/div

1µs/div
full bandwidth



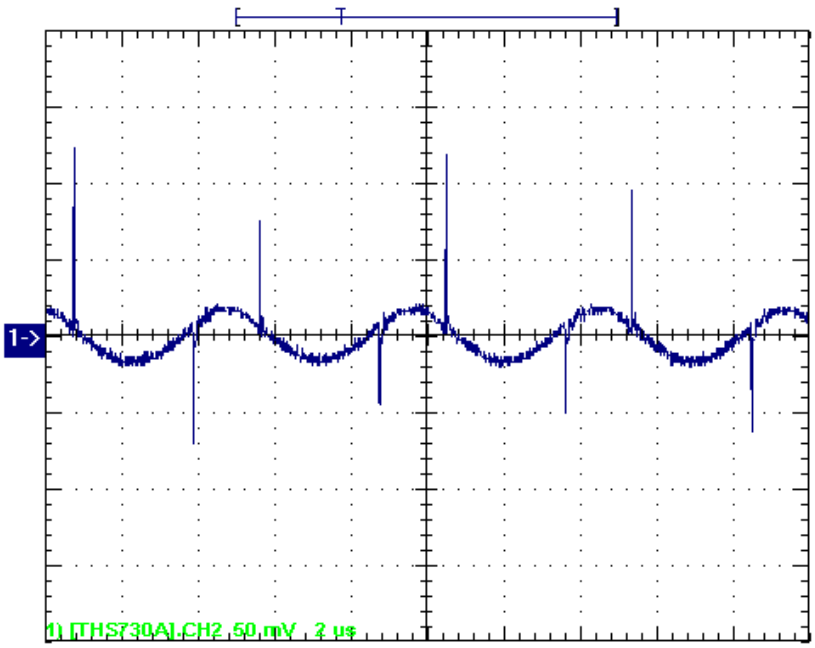
Ch1 => gate-source
2V/div

50ns/div
full bandwidth

Figure 11

8 Ripple Voltages

The output ripple voltage is displayed in Figure 12. The input voltage was set to 24V with output current 10A.

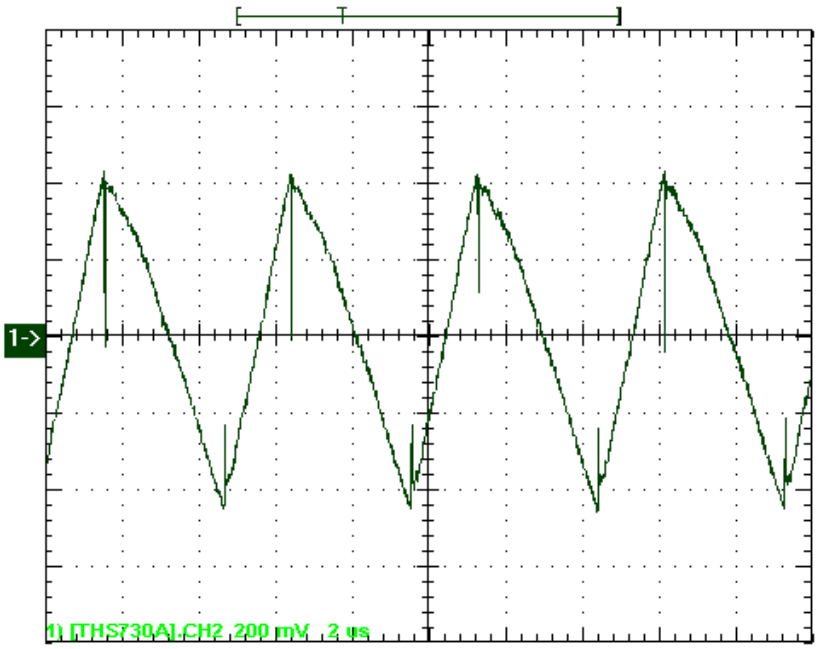


Ch1=> output voltage
50mV/div

2µs/div
AC coupling
20MHz bandwidth

Figure 12

The input ripple voltage is displayed in. The input voltage was set to 24V with output current 10A.



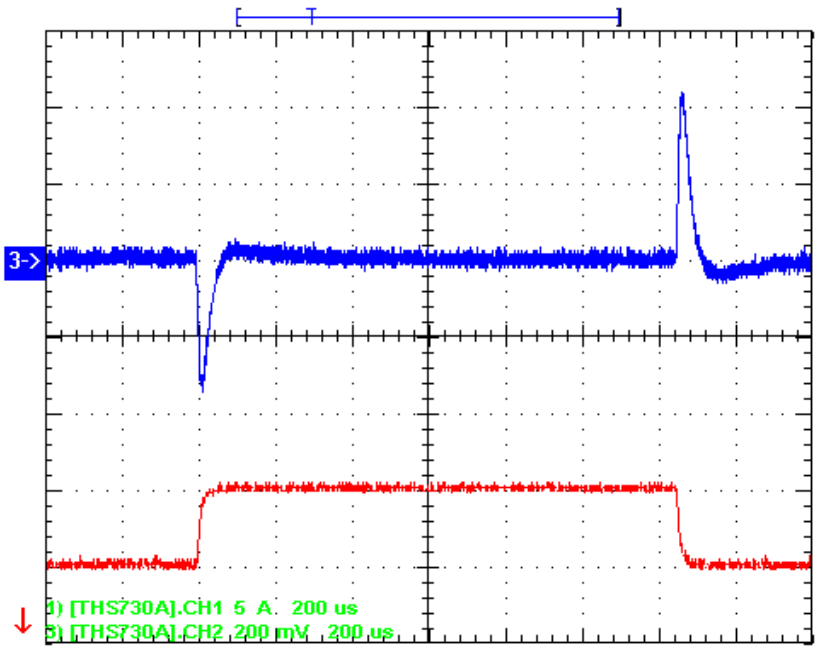
Ch2=> input voltage
200mV/div

2µs/div
AC coupling
20MHz bandwidth

Figure 13

9 Load Transients

A output current change from 5A to 10A (400Hz) results in following Figure 14.The input voltage was set 24V.



Ch3=> output voltage@16Vin AC coupled 200mV/div

Ch1=> output current 5A/div

200µs/div

20MHz bandwidth

Figure 14

10 Thermal Image

Figure 15 and Figure 16 shows the thermal image with 10A output current and 24V input voltage

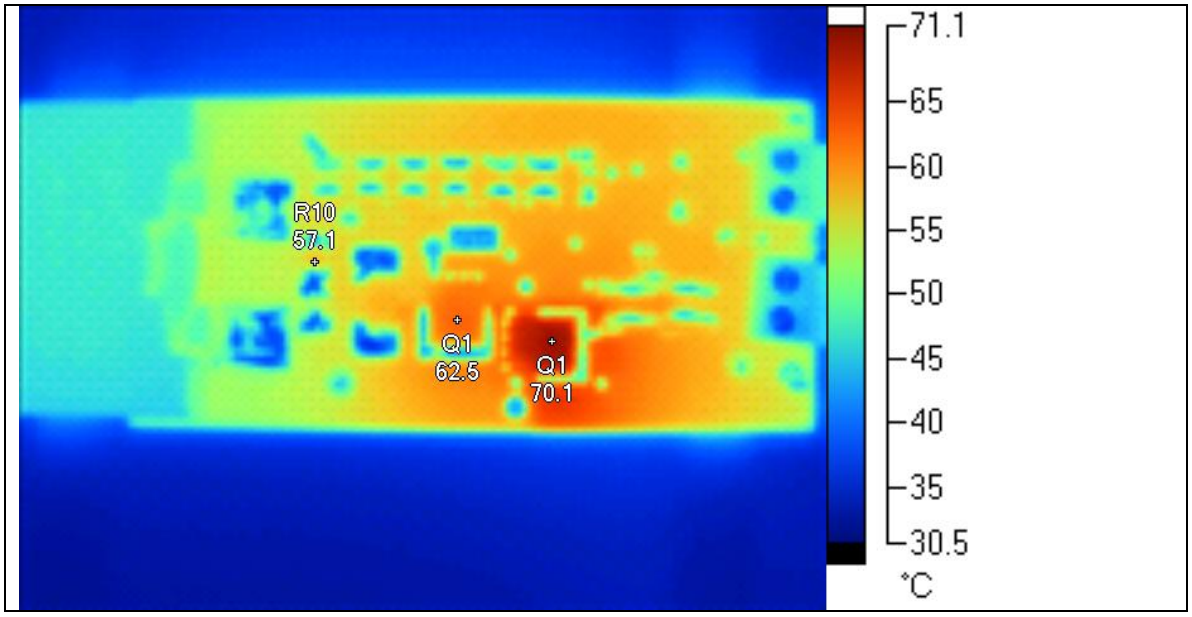


Figure 15 Top side image

Name	Temperature
Q1	70.1°C
Q1	62.5°C
R10	57.1°C

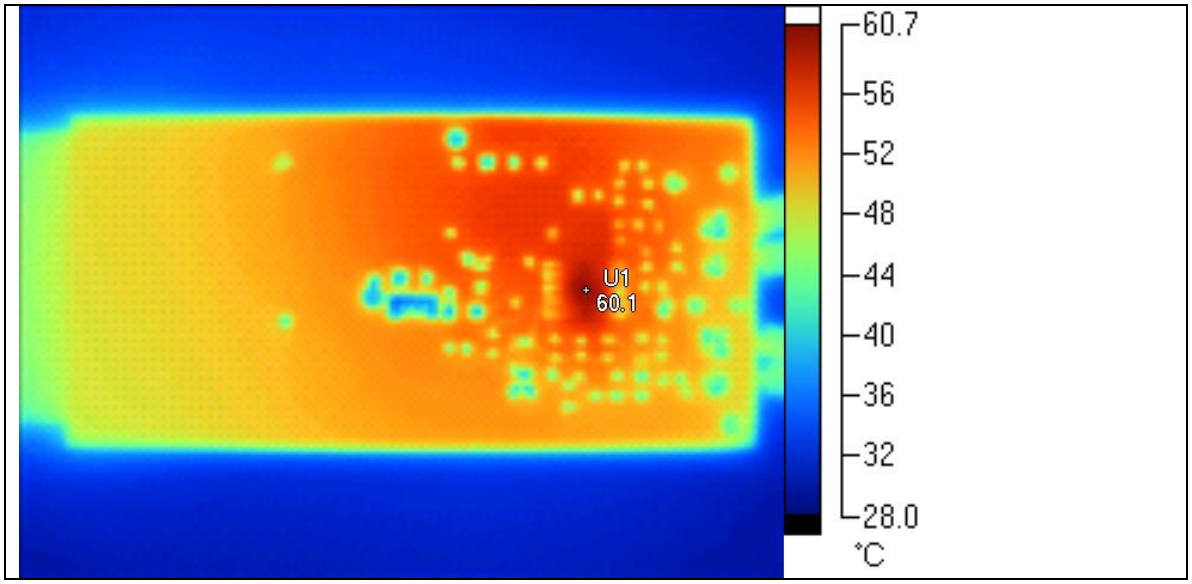


Figure 16 bottom side image

Name	Temperature
U1	60.1°C

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