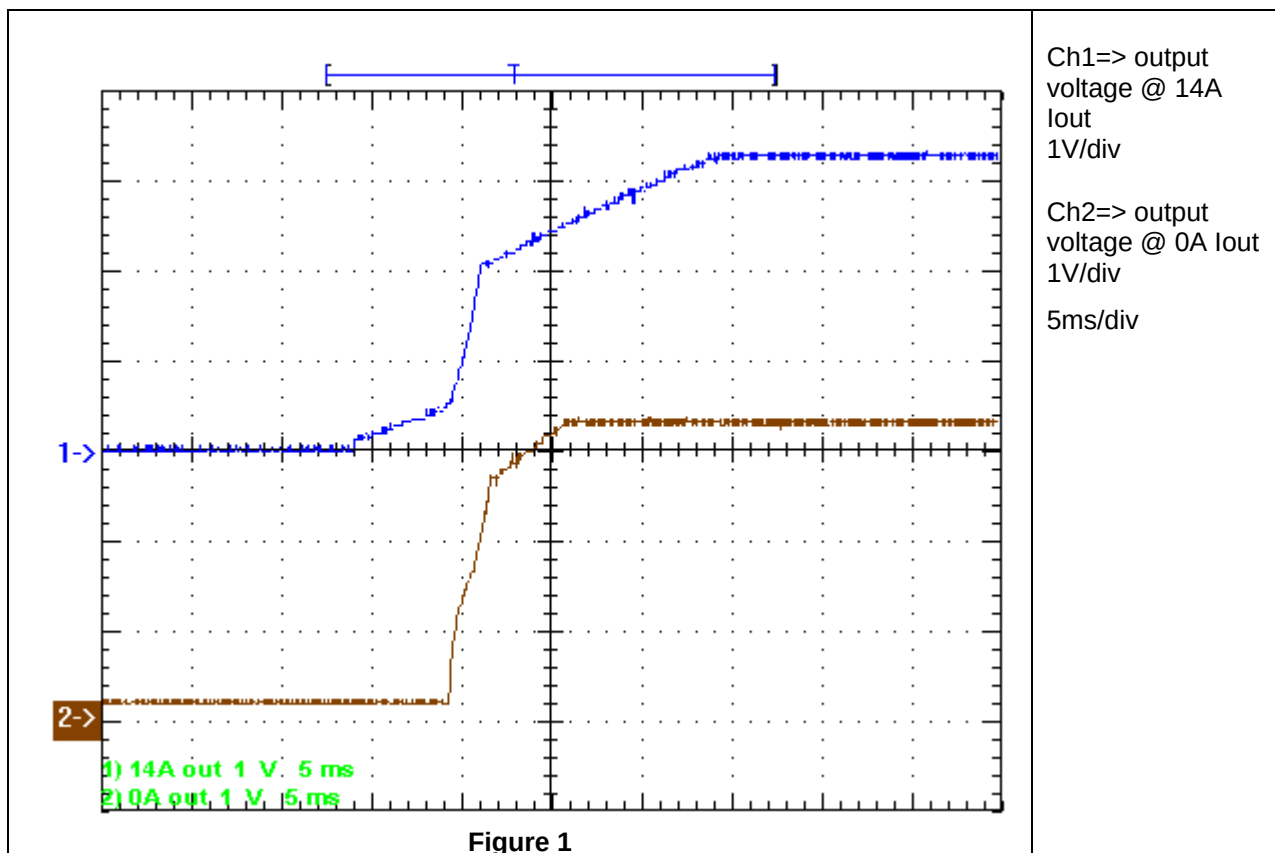


PMP4523RevC Test Results

1 Startup

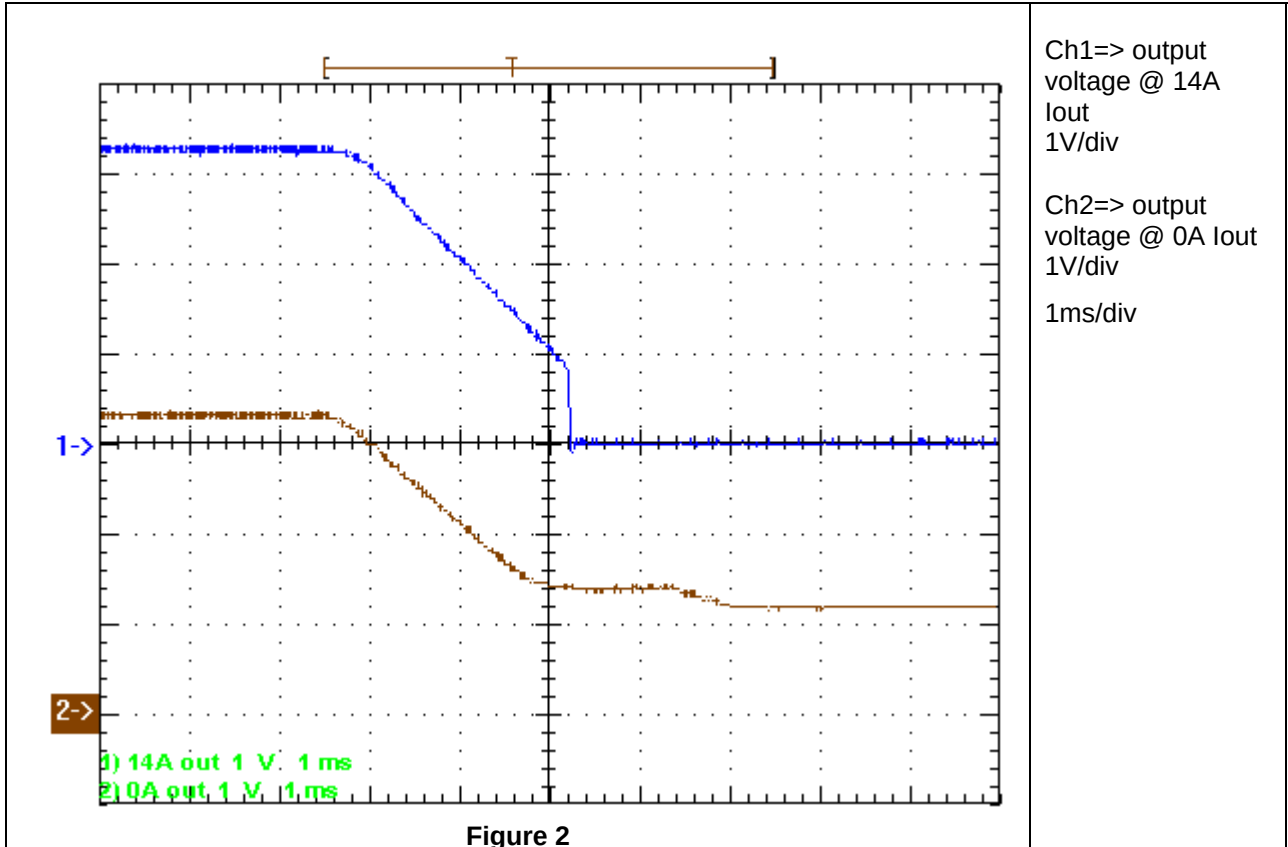
The startup waveform is shown in the Figure 1. The input voltage was set at 48V, with 0A and 14A load at the output.



PMP4523RevC Test Results

2 Shutdown

The shutdown waveform is shown in the Figure 2. The input voltage was set at 48V, with 0A and 14A load on the output.



3 Efficiency

The efficiency is shown in the Figure 3 below. The curves represent different input voltages.

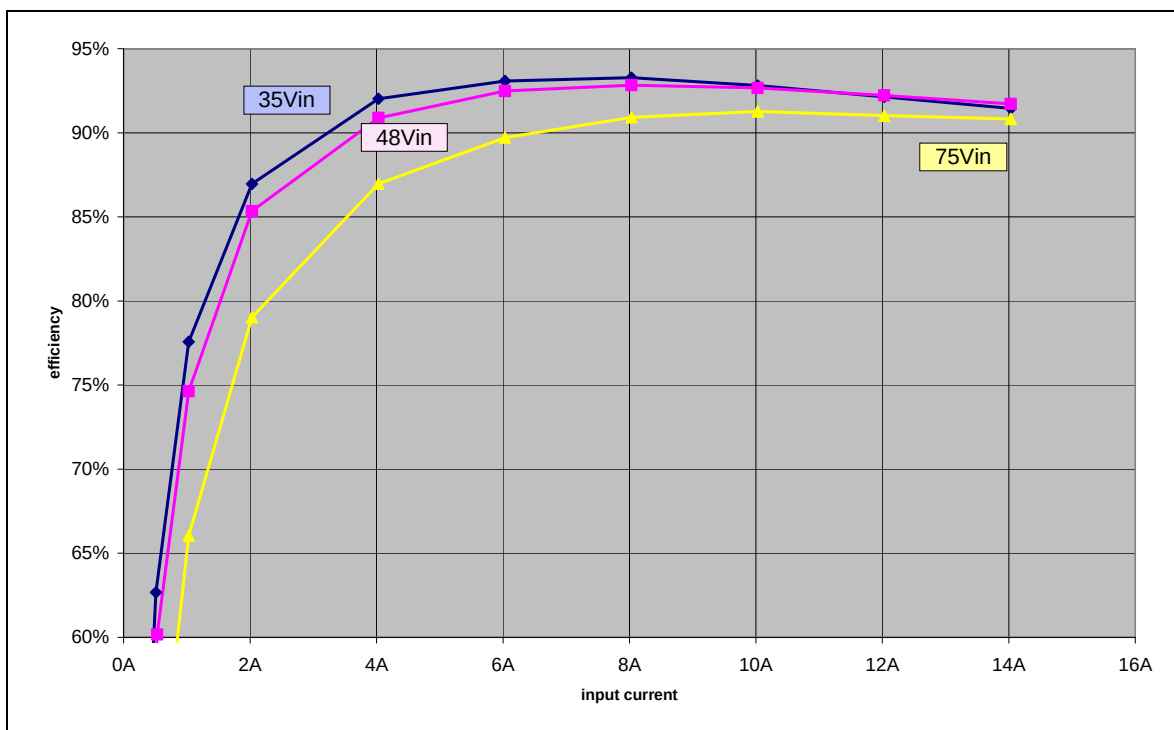


Figure 3

Figure 4 show the efficiency dependency to the input voltage.

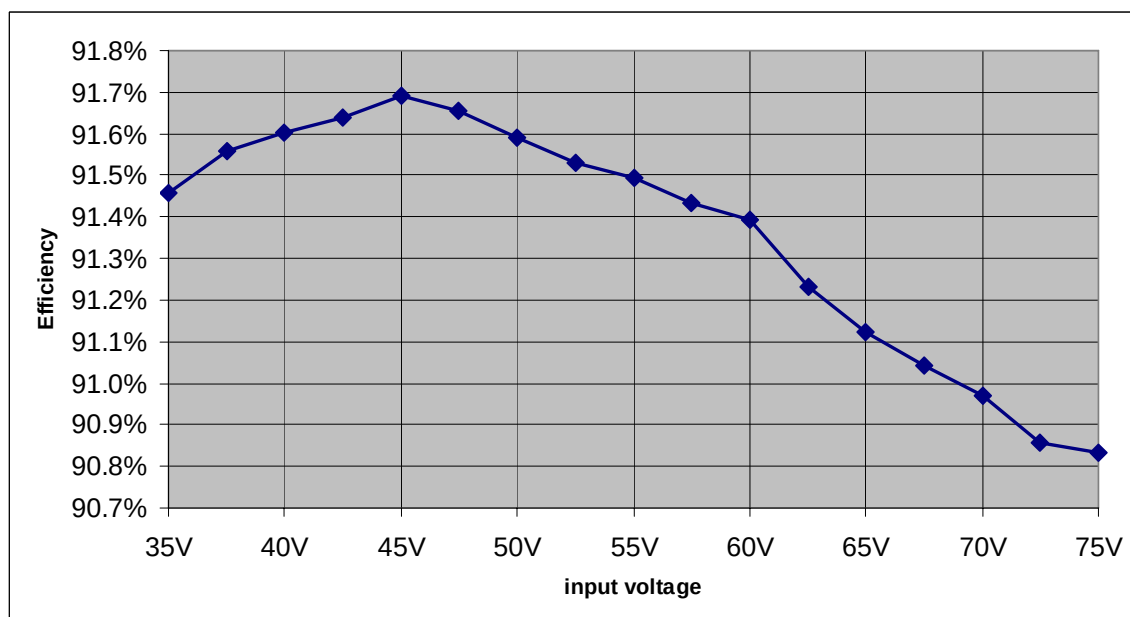


Figure 4

PMP4523RevC Test Results

3 Load Regulation

The load regulation of the output is shown in the Figure 5 below. The curves represent different input voltages, <3mV across full output current range.

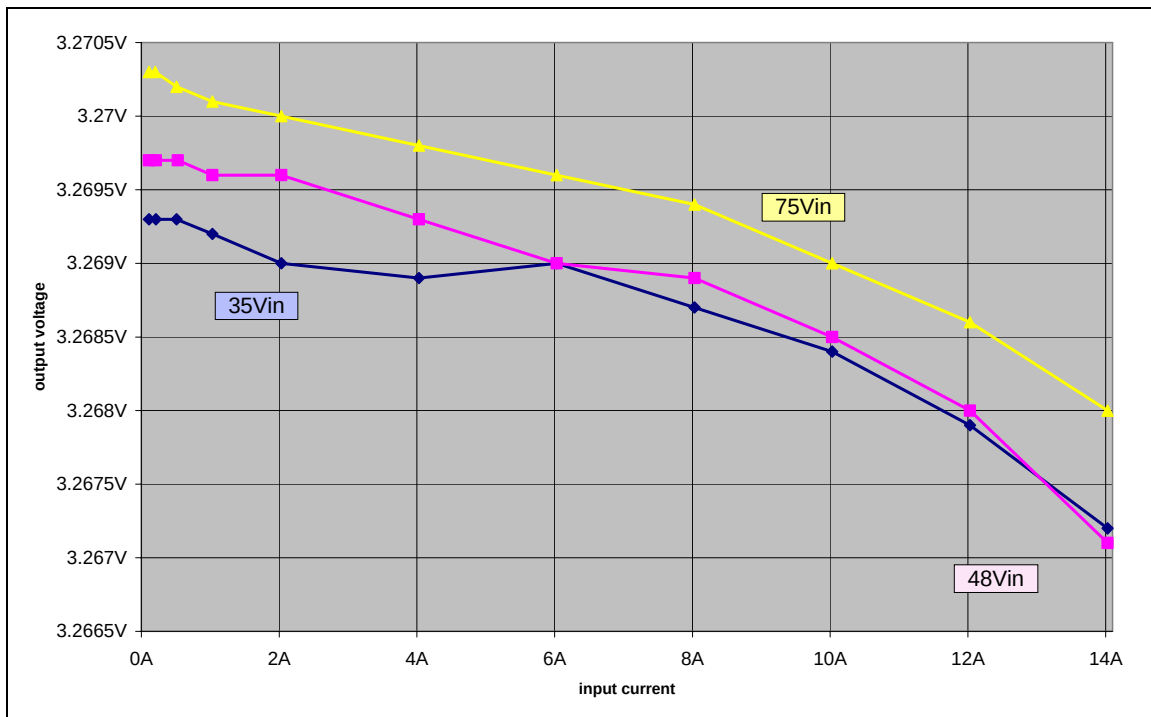


Figure 5

4 Line Regulation

The dependency of the output voltage to the input voltage shows Figure 6. The current was set to 14A, <1mV across full input voltage range.

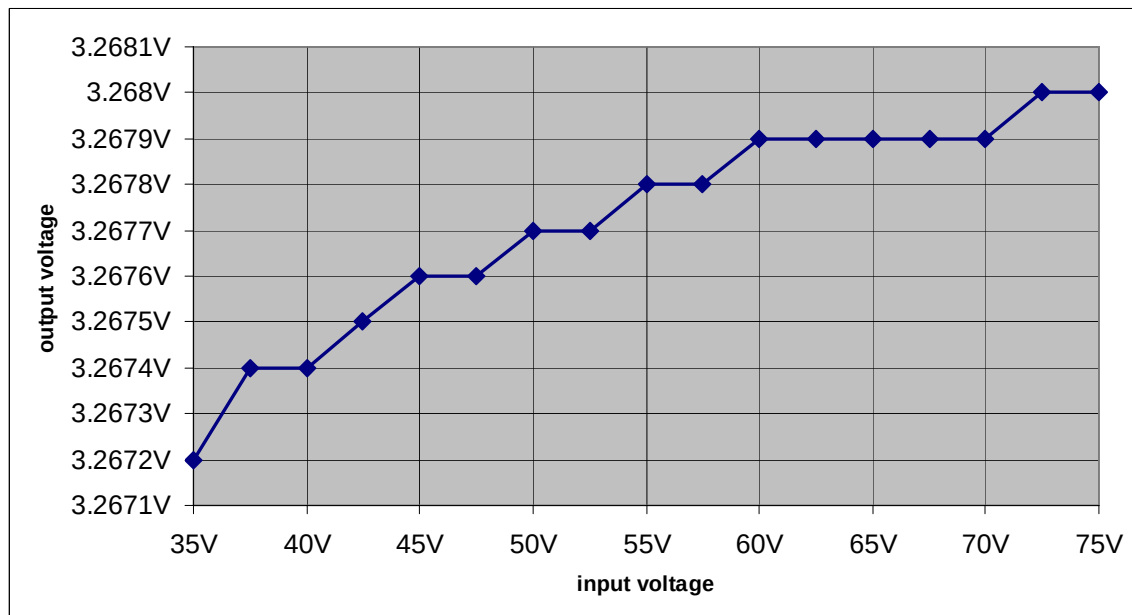


Figure 6

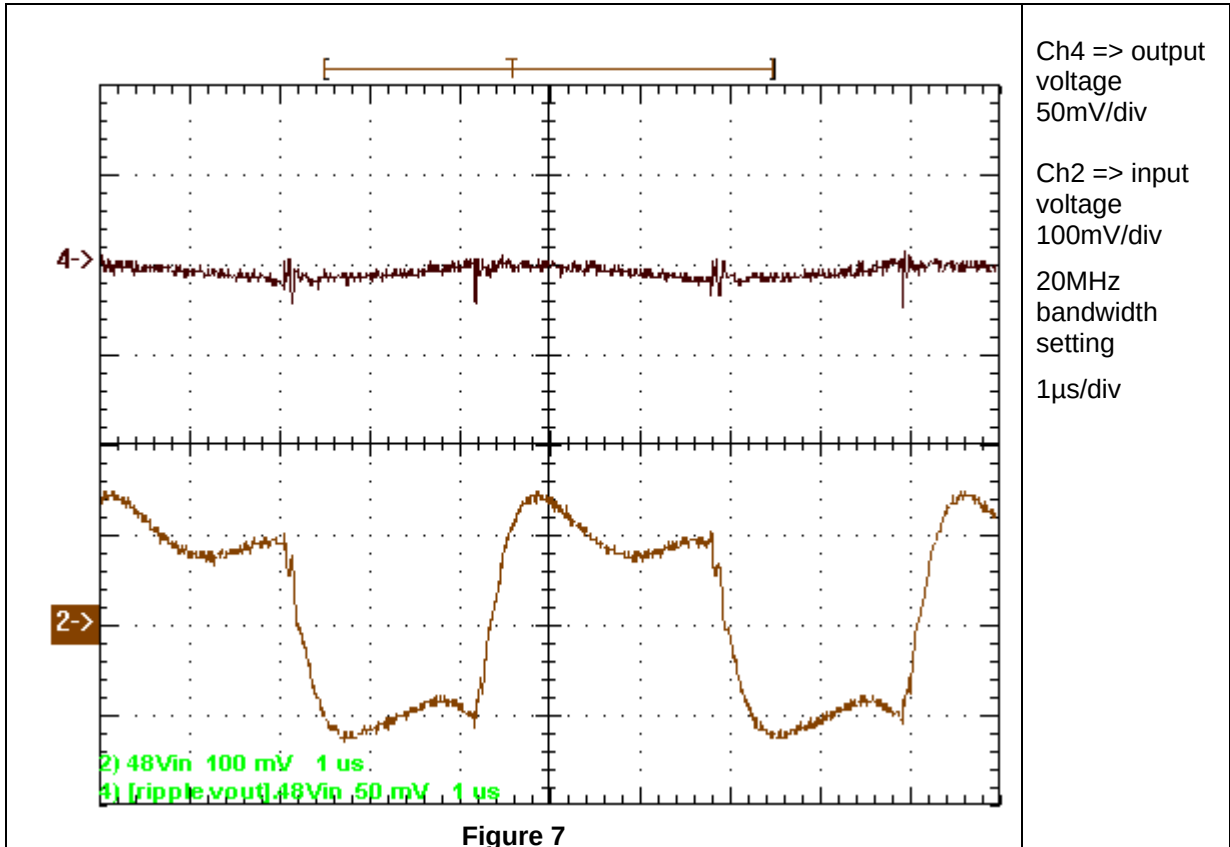
PMP4523RevC Test Results

5 Ripple Voltage

The ripple voltages are shown in Figure 7. The image was taken with a 14 A load and 48V at the input. Curves were captured separately both were triggered with the primary switch node.

Ch4 is output ripple voltage <20mVpp,

Ch 2 is reflected input ripple voltage w/ bulk capacitance 220uF/160V



6 Control Loop Frequency Response

Figure 8 shows the loop response with 14A load and 48V input.

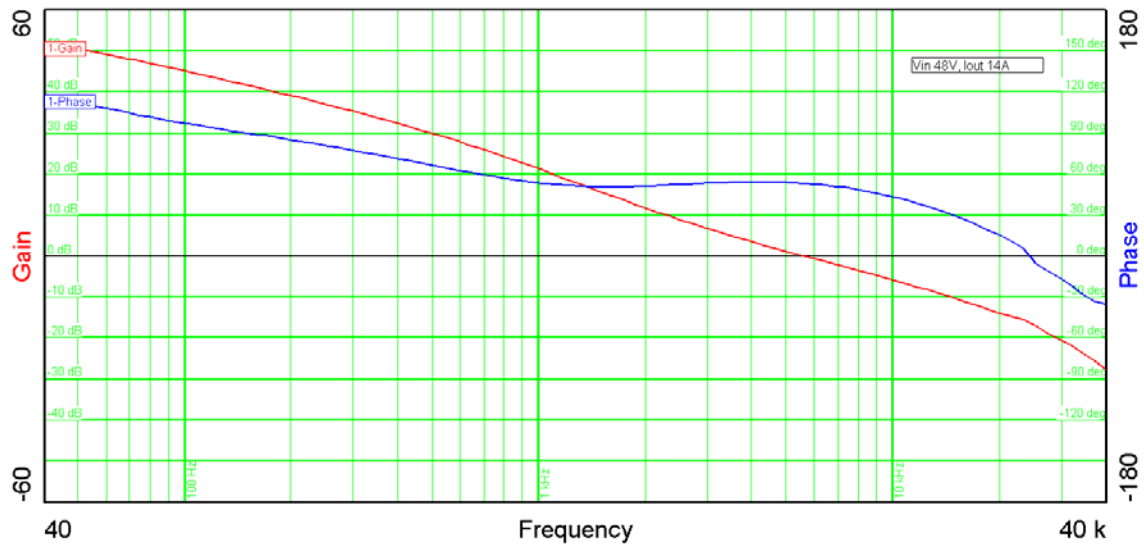


Figure 8

Table 1 summarizes the results from Figure 8

Bandwidth (kHz)	5.62
Phasemargin	53.34°
slope	
(20dB/decade)	-1.19
gain margin (dB)	-16.18
slope	
(20dB/decade)	-1.94
freq (kHz)	24.21

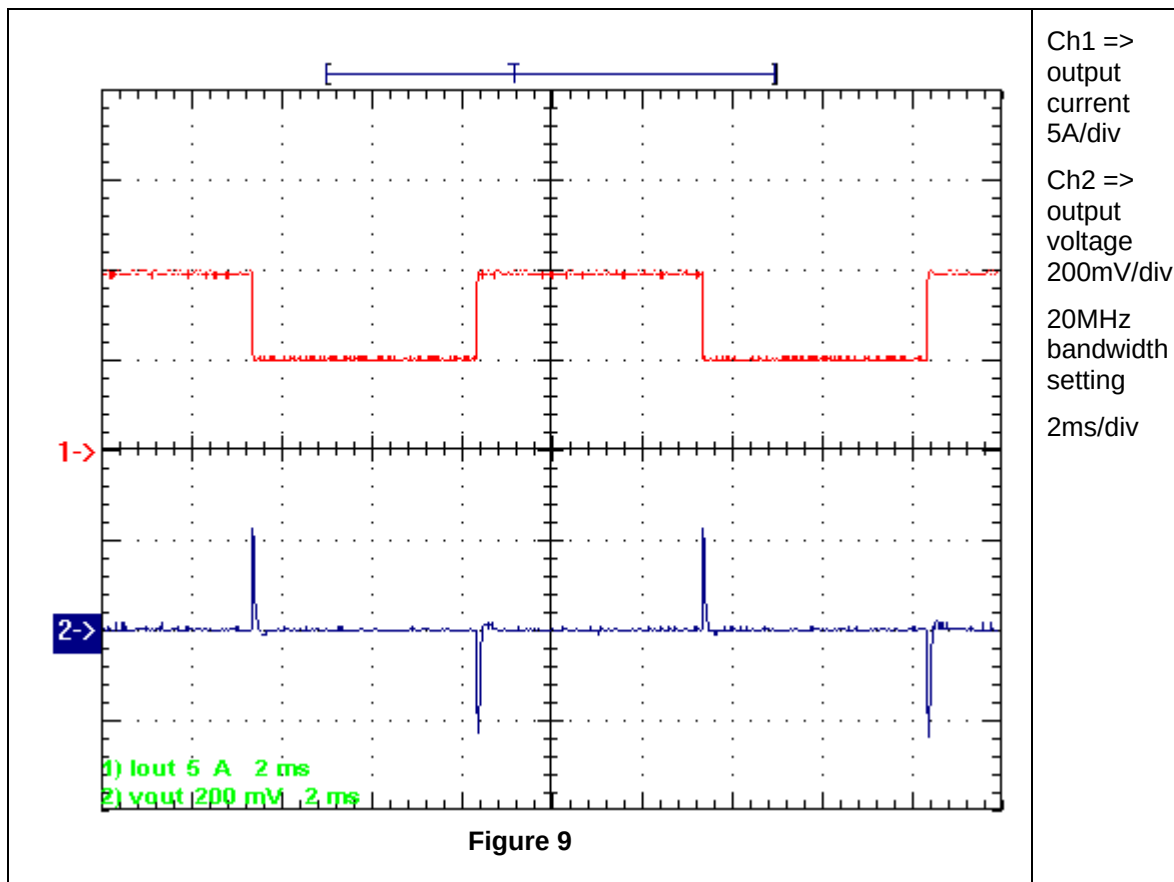
Table 1

PMP4523RevC Test Results

7 Load Transients

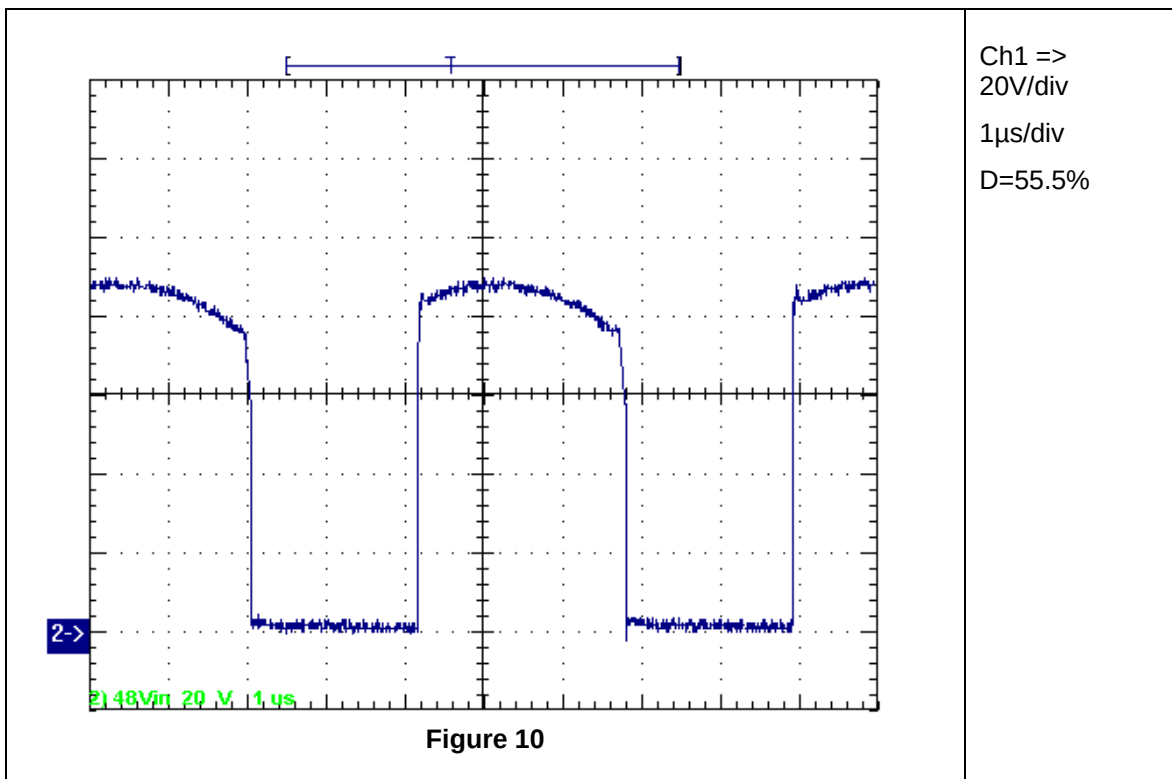
The Figure 9 shows the response to load transients. The load is switching from 5A to 10A with 100Hz frequency. The input voltage was set to 48V.

du = 240mV w/ output capacitance 2 x 180uF



8 Switch Node Waveform

With input voltage set to 48V and 14A lout results in the waveform shown in Figure 10 (primary side).



The waveform of the secondary switch node is shown in Figure 11. (the same setup as above)

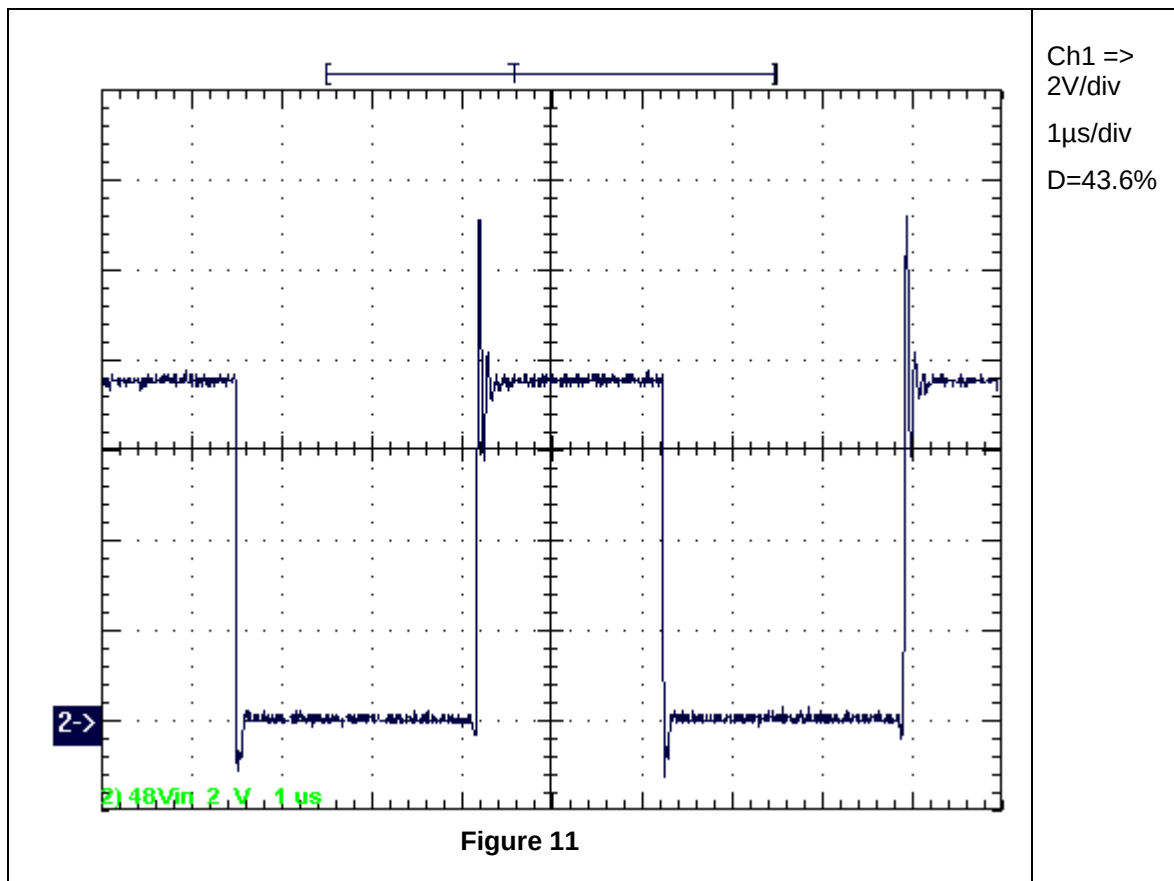
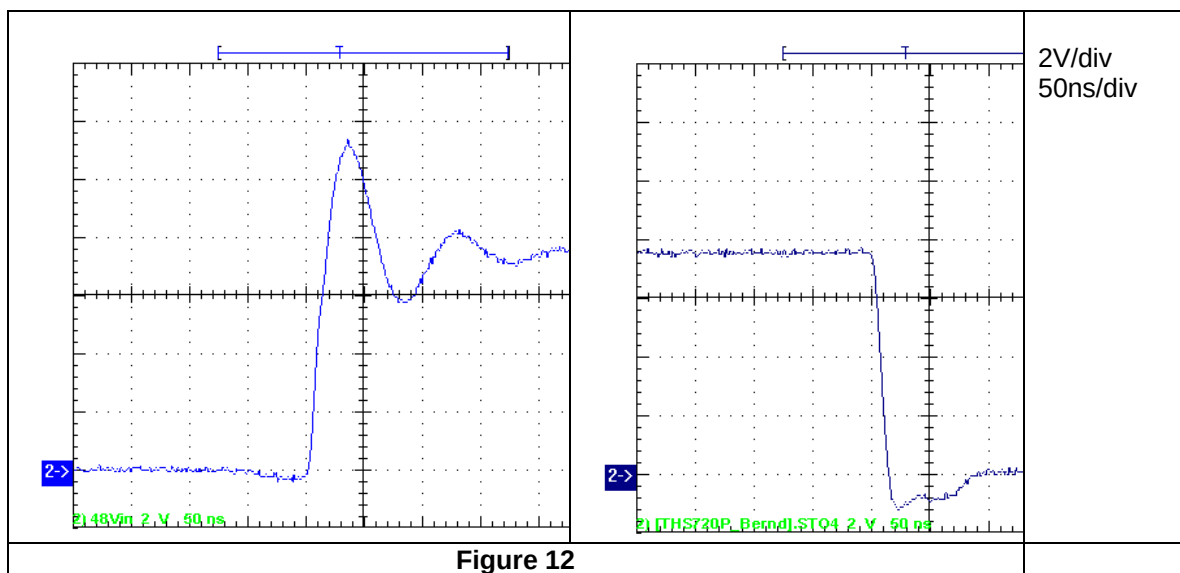


Figure 12 shows the same with other time base.



PMP4523RevC Test Results

Figure 13 shows the primary OFF time (1-D) at various input voltages and secondary duty cycle.

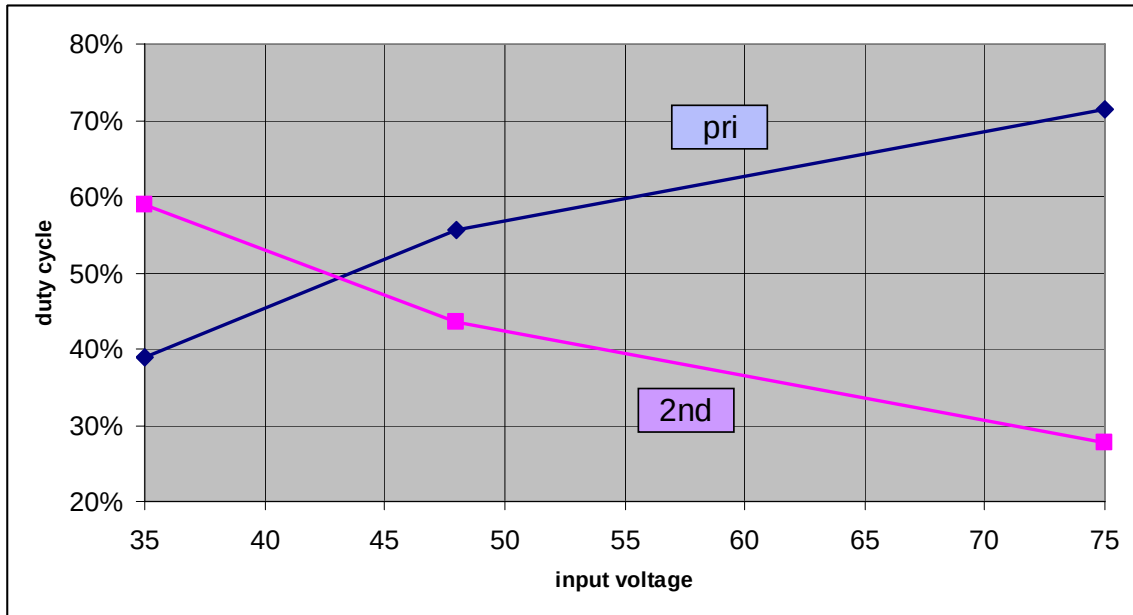


Figure 13

9 Thermal Image

Topside image is shown on Figure 14.

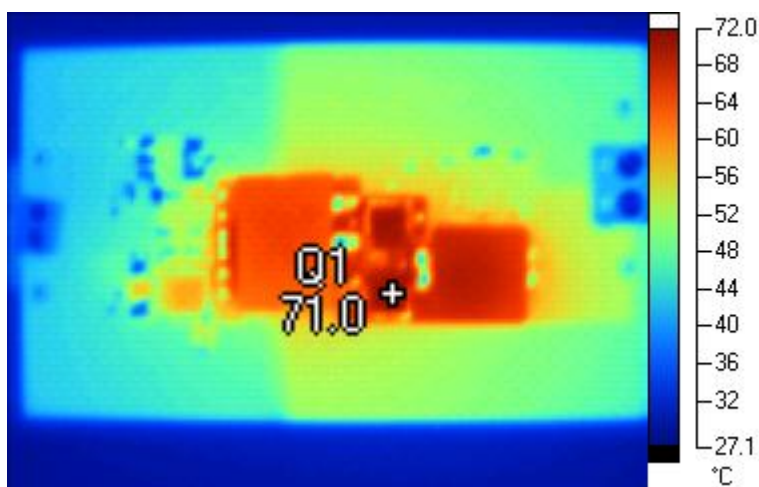


Figure 14

Bottomside image is shown on Figure 15.

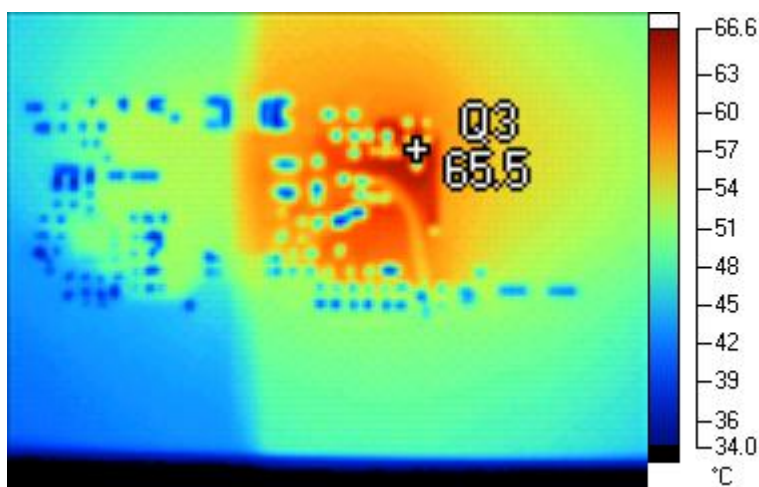


Figure 15

(thermal images were taken after 1hr. maximum load 14Amps and 48V input voltage)

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