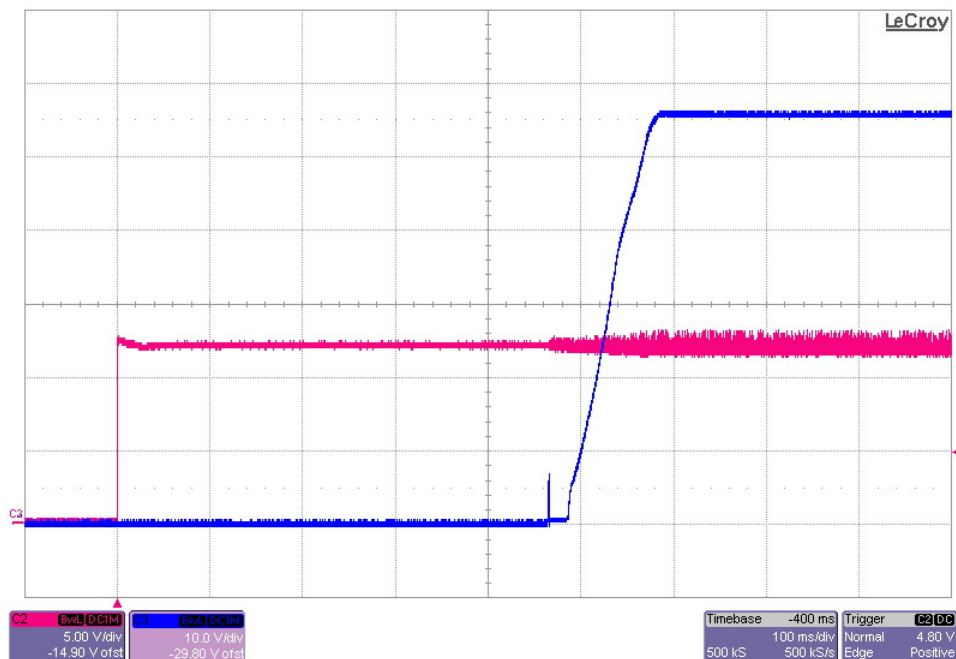
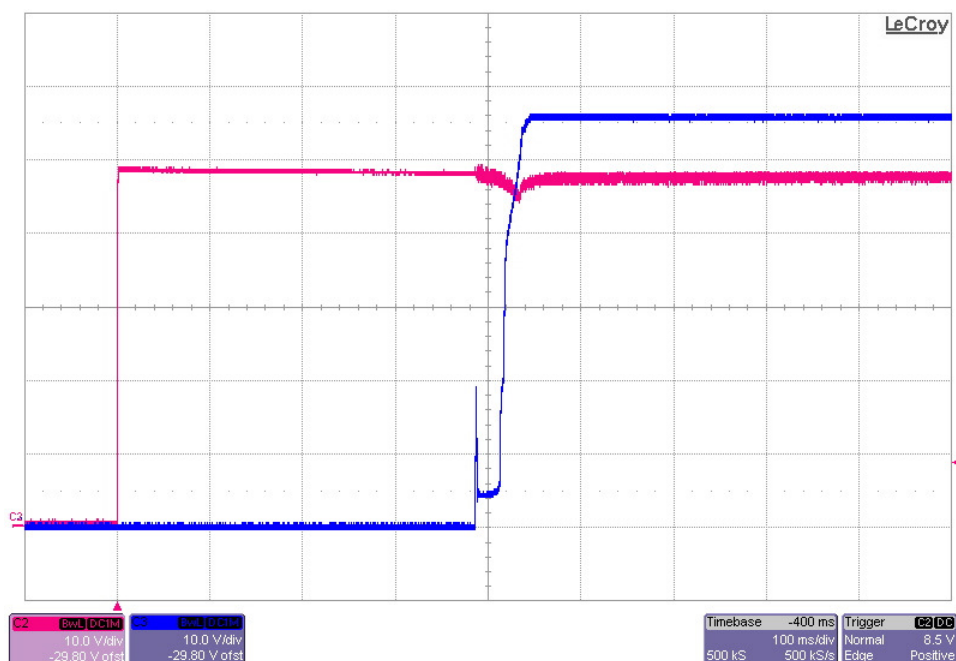


1 Output Voltage Startup

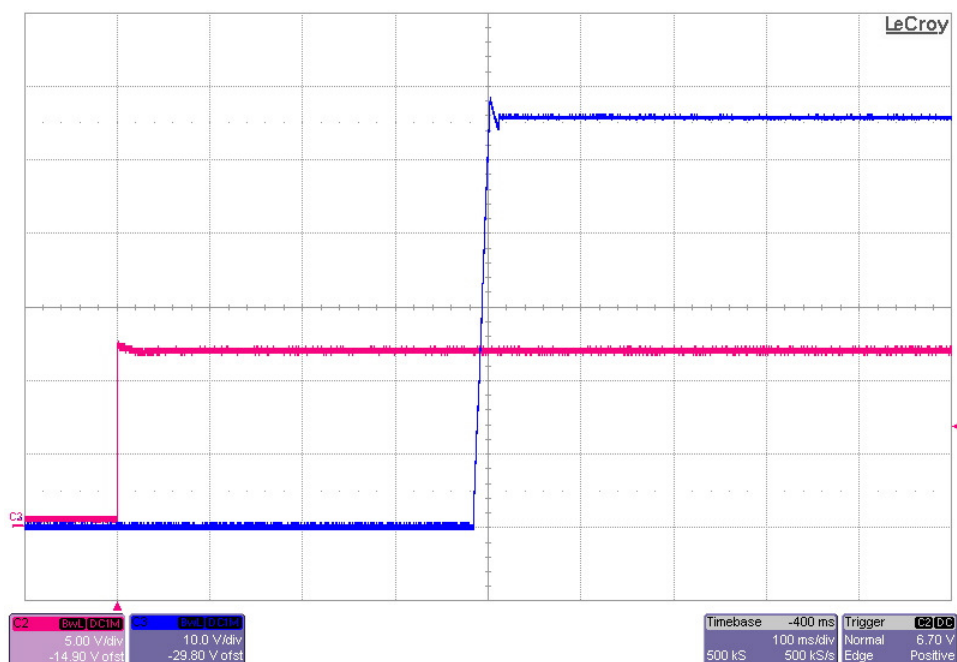
The photo below shows the 56V output voltage startup waveforms after the application of 12Vdc in. The output was loaded to 0.35A. (Vin is 5V/DIV, Vout is 10V/DIV, 100mS/DIV)



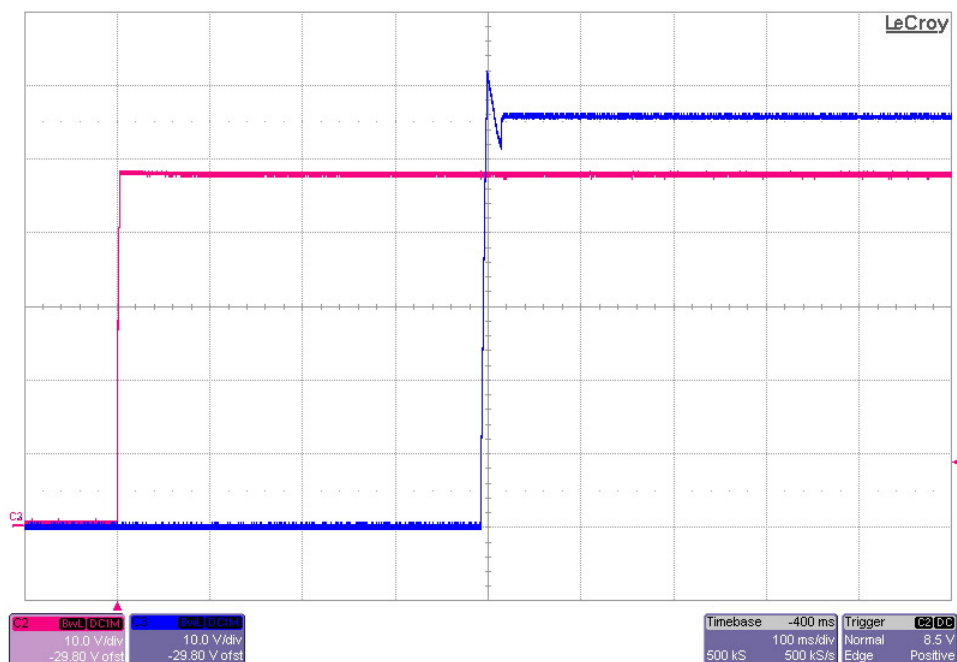
The photo below shows the 56V output voltage startup waveforms after the application of 48Vdc in. The output was loaded to 0.35A. (Vin is 10V/DIV, Vout is 10V/DIV, 100mS/DIV)



The photo below shows the 56V output voltage startup waveforms after the application of 12Vdc in. The output was loaded to 0A. (Vin is 5V/DIV, Vout is 10V/DIV, 100mS/DIV)

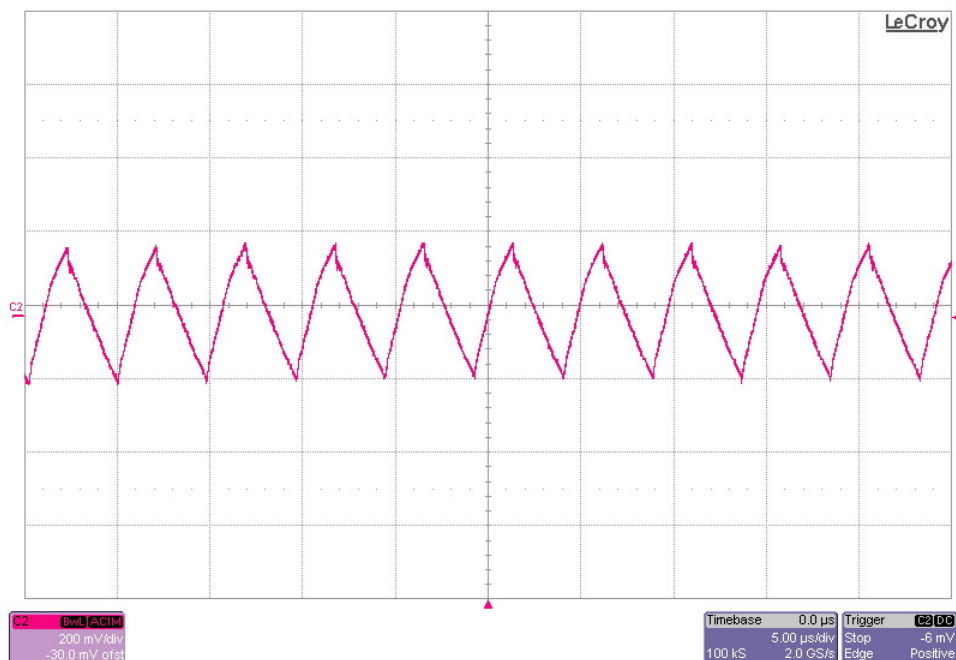


The photo below shows the 56V output voltage startup waveforms after the application of 48Vdc in. The output was loaded to 0A. (Vin is 10V/DIV, Vout is 10V/DIV, 100mS/DIV)

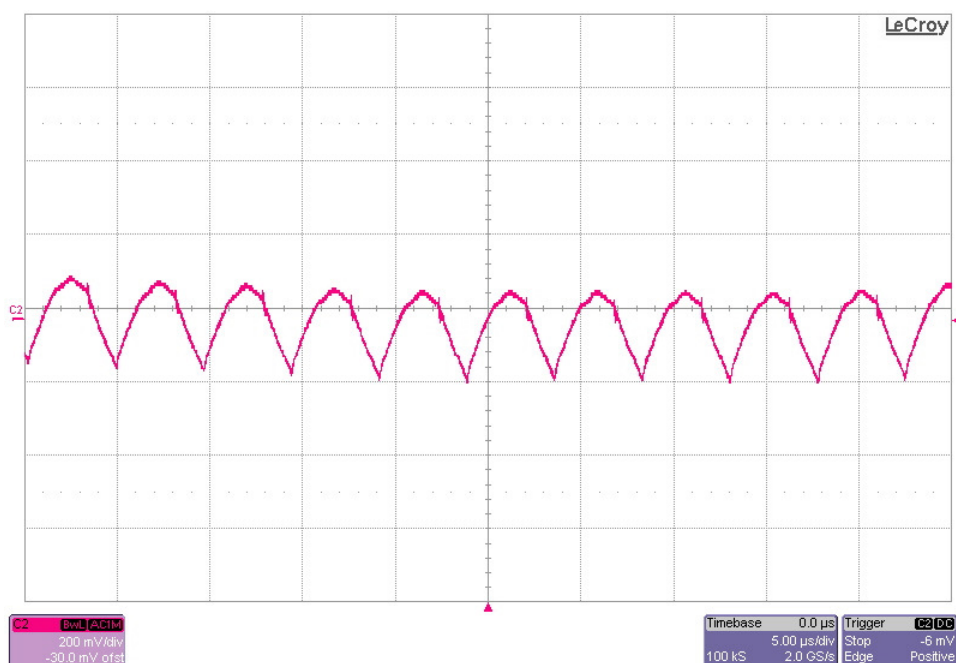


2 Output Ripple Voltage

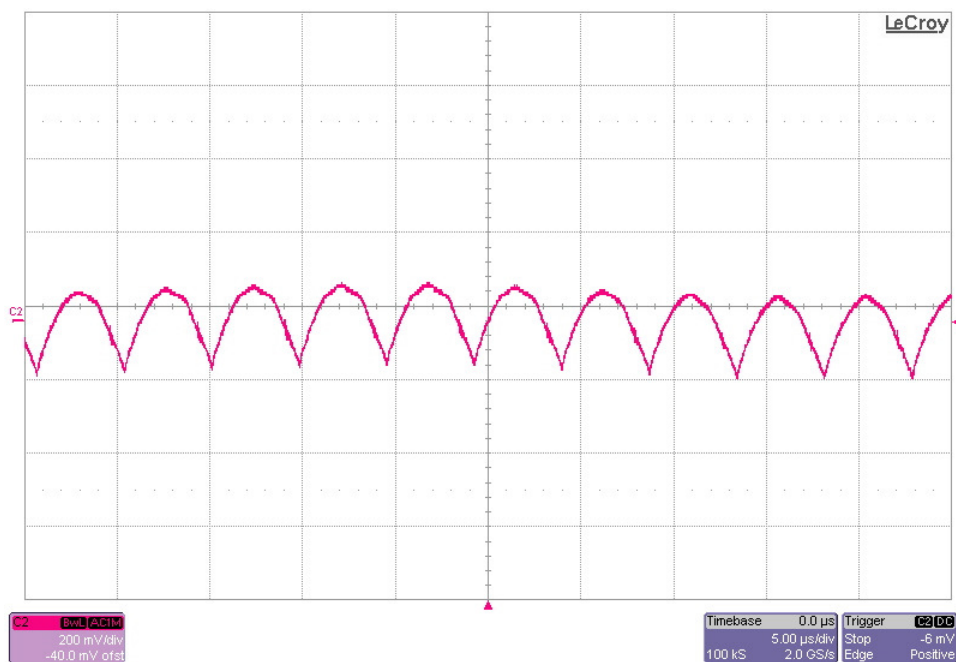
The 56V output ripple voltage is shown in the figure below. The image was taken with the output loaded at 0.35A and the input voltage set to 9Vdc. (200mV/DIV, 5uS/DIV)



The 56V output ripple voltage is shown in the figure below. The image was taken with the output loaded at 0.35A and the input voltage set to 24Vdc. (200mV/DIV, 5uS/DIV)

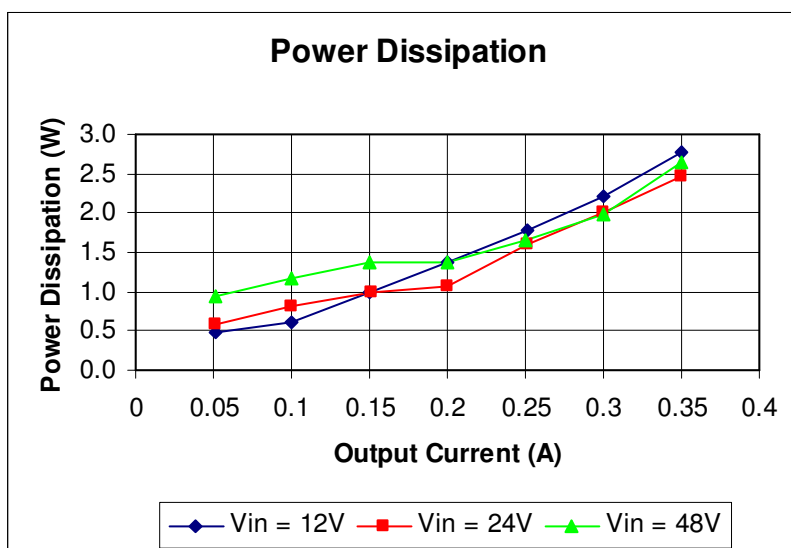
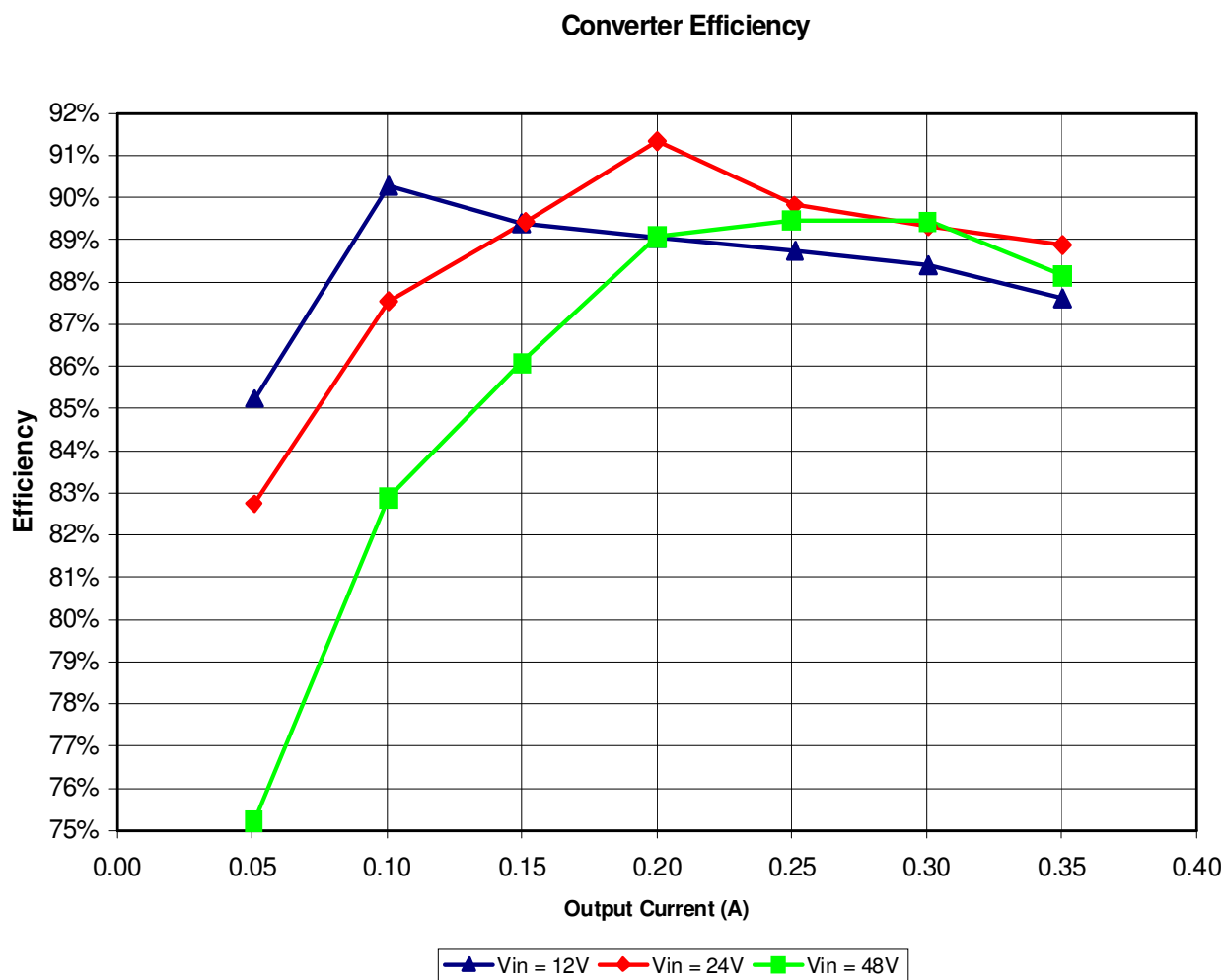


The 56V output ripple voltage is shown in the figure below. The image was taken with the output loaded at 0.35A and the input voltage set to 57Vdc. (200mV/DIV, 5uS/DIV)



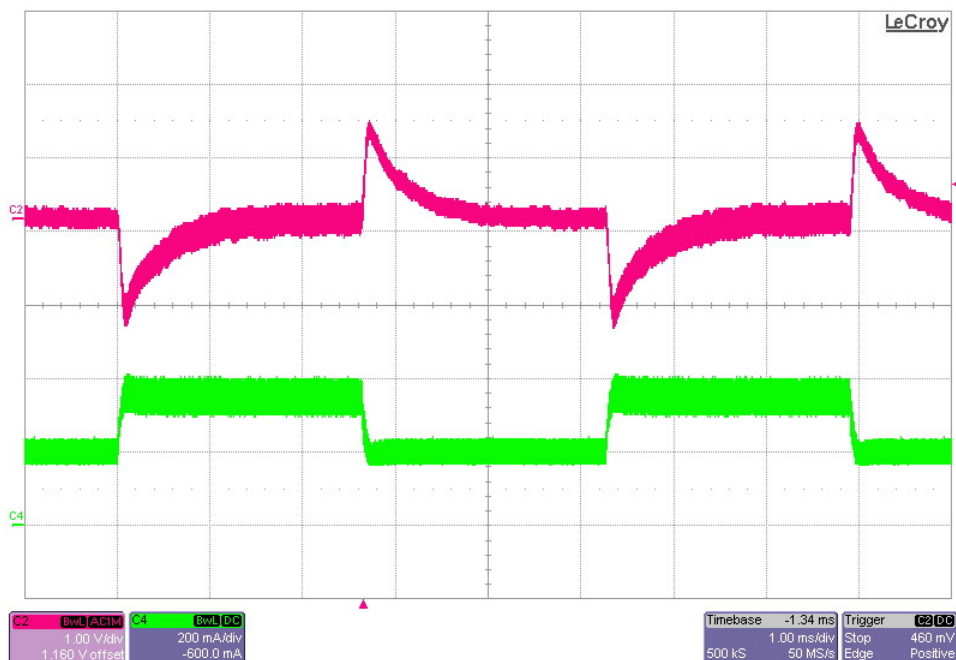
3 Efficiency

The flyback converter efficiency is shown in the figure below.

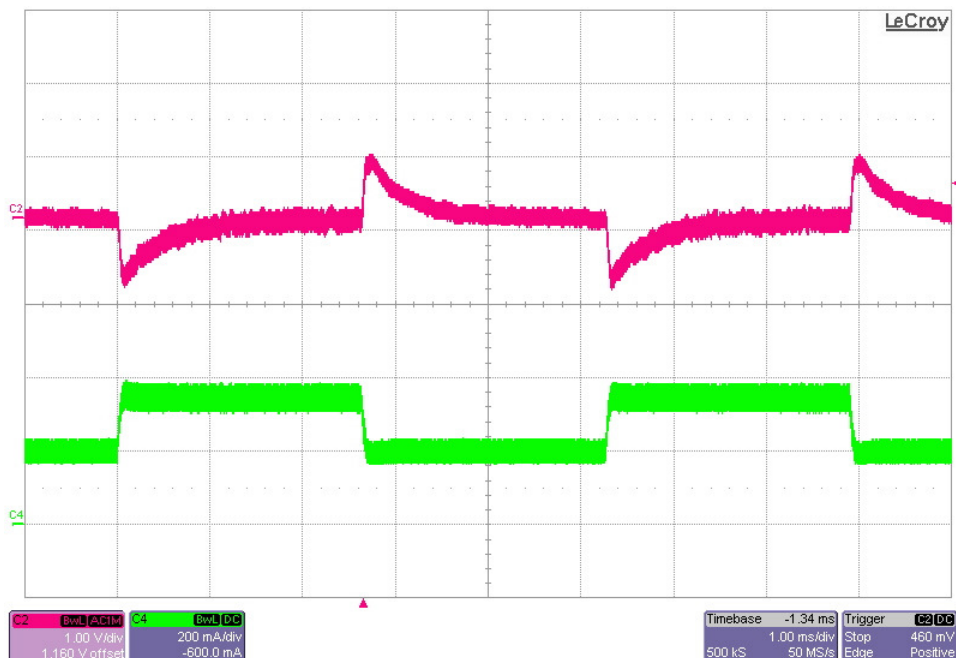


4 Load Transients

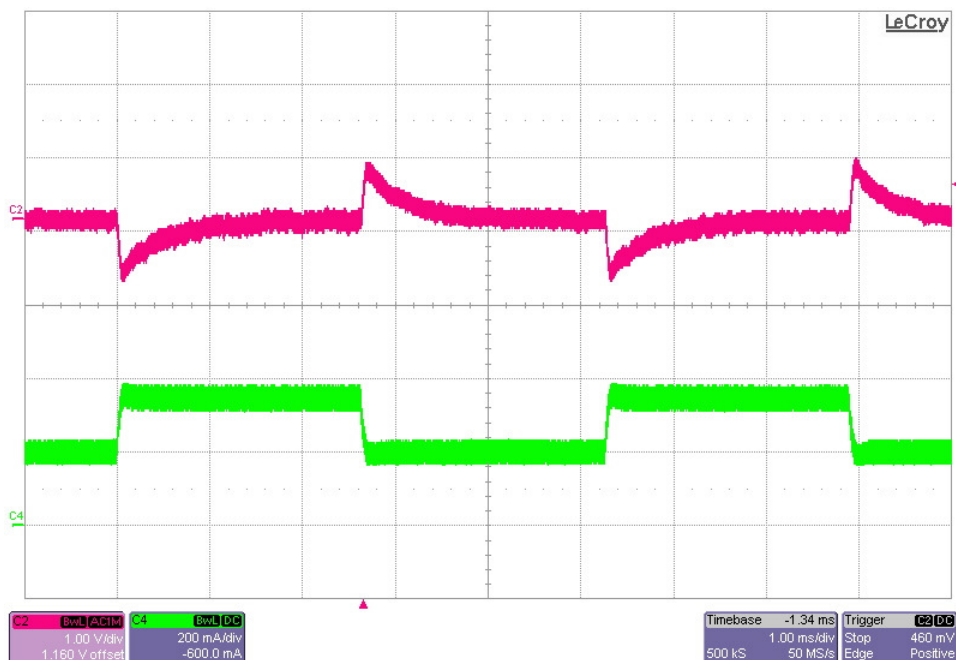
The photo below shows the response of the 56V output voltage (ac coupled) to the load current stepping between 0.20A and 0.35A. $V_{in} = 9V_{dc}$. (1V/DIV, 200mA/DIV, 1mS/DIV)



The photo below shows the response of the 56V output voltage (ac coupled) to the load current stepping between 0.20A and 0.35A. $V_{in} = 24V_{dc}$. (1V/DIV, 200mA/DIV, 1mS/DIV)

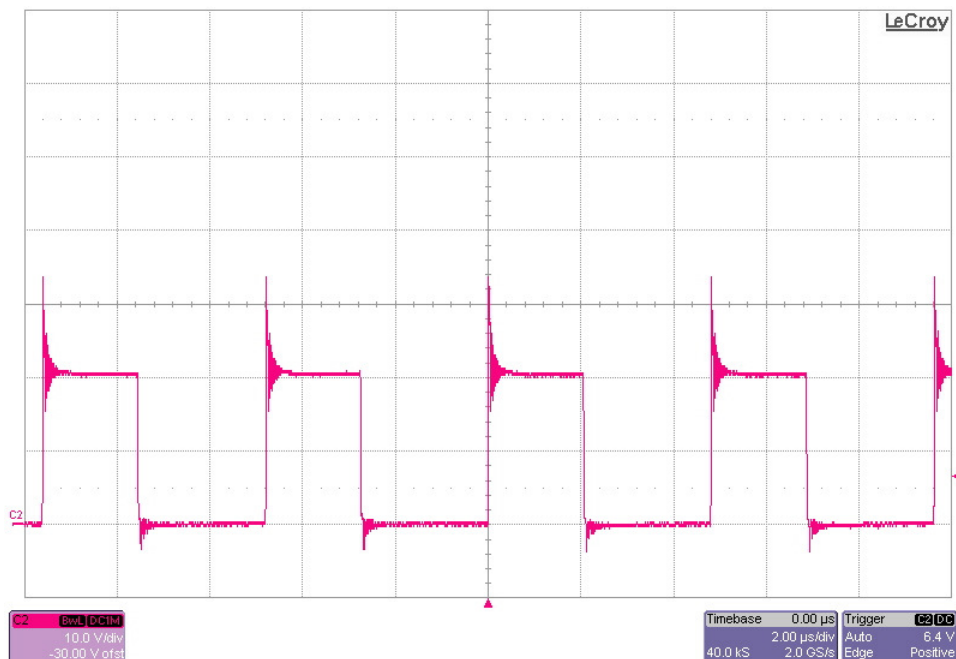


The photo below shows the response of the 56V output voltage (ac coupled) to the load current stepping between 0.20A and 0.35A. $V_{in} = 48V_{dc}$. (1V/DIV, 200mA/DIV, 1mS/DIV)

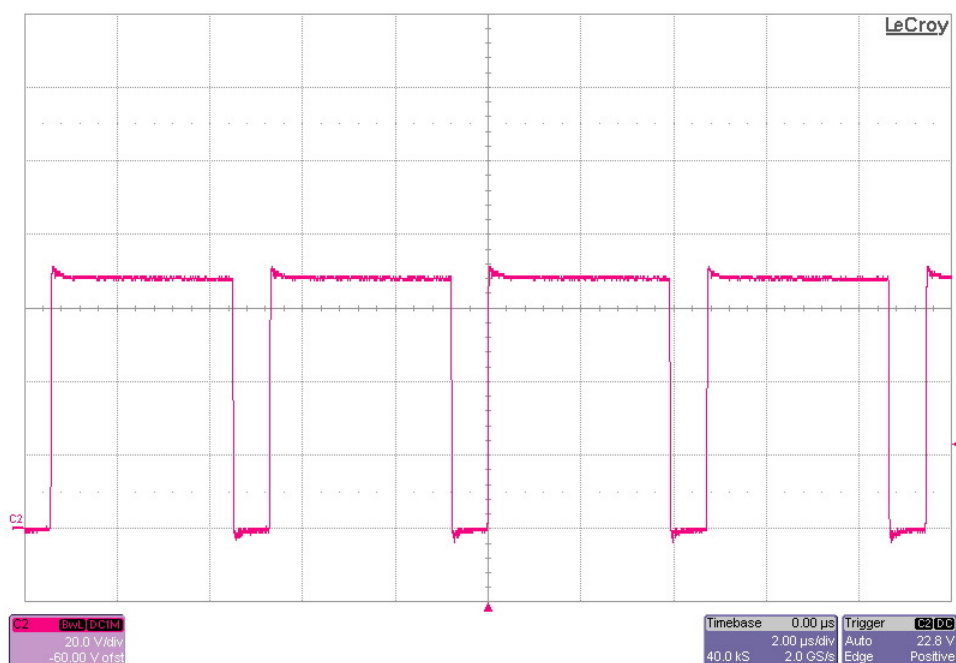


5 Switch Node Waveforms

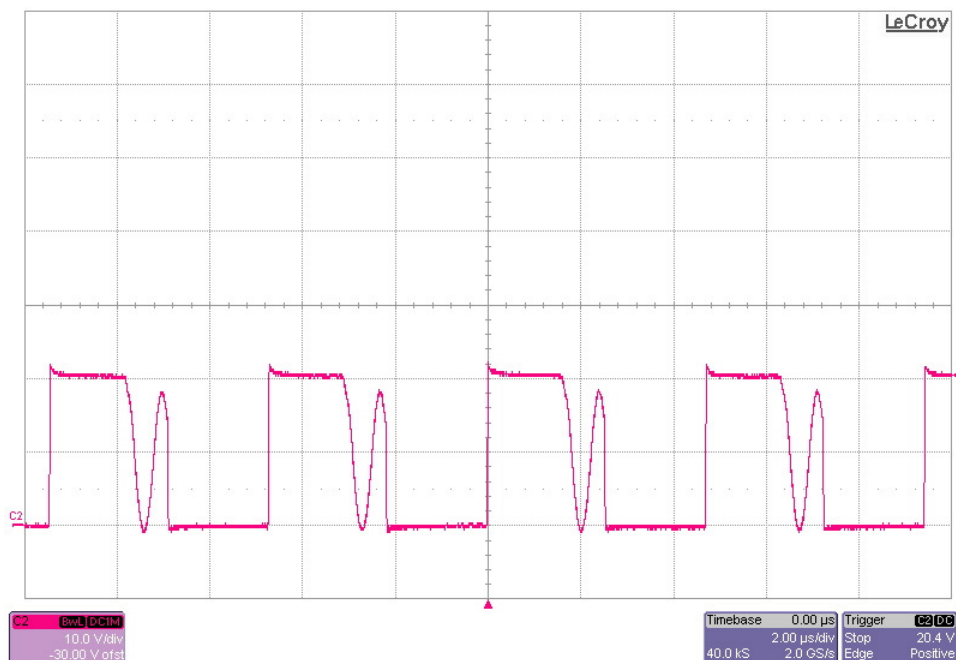
The photos below show the FET drain voltage at TP3. The input voltage is 9V and the output is loaded to 0.35A. (10V/DIV, 2uS/DIV)



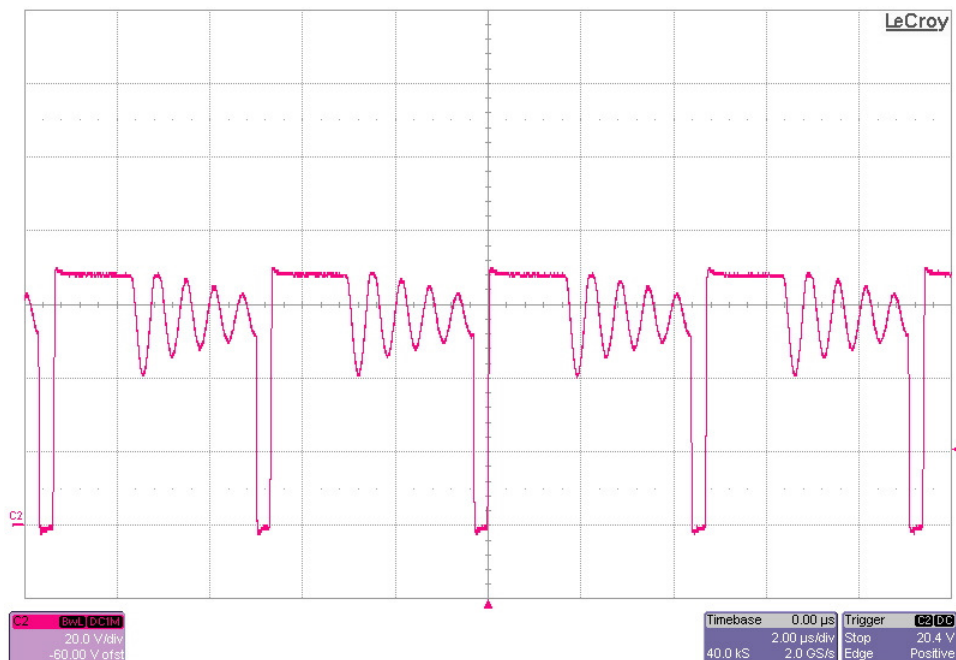
The photos below show the FET drain voltage at TP3. The input voltage is 57V and the output is loaded to 0.35A. (20V/DIV, 2uS/DIV)



The photos below show the FET drain voltage at TP3. The input voltage is 9V and the output is loaded to 0.05A. (10V/DIV, 2uS/DIV)



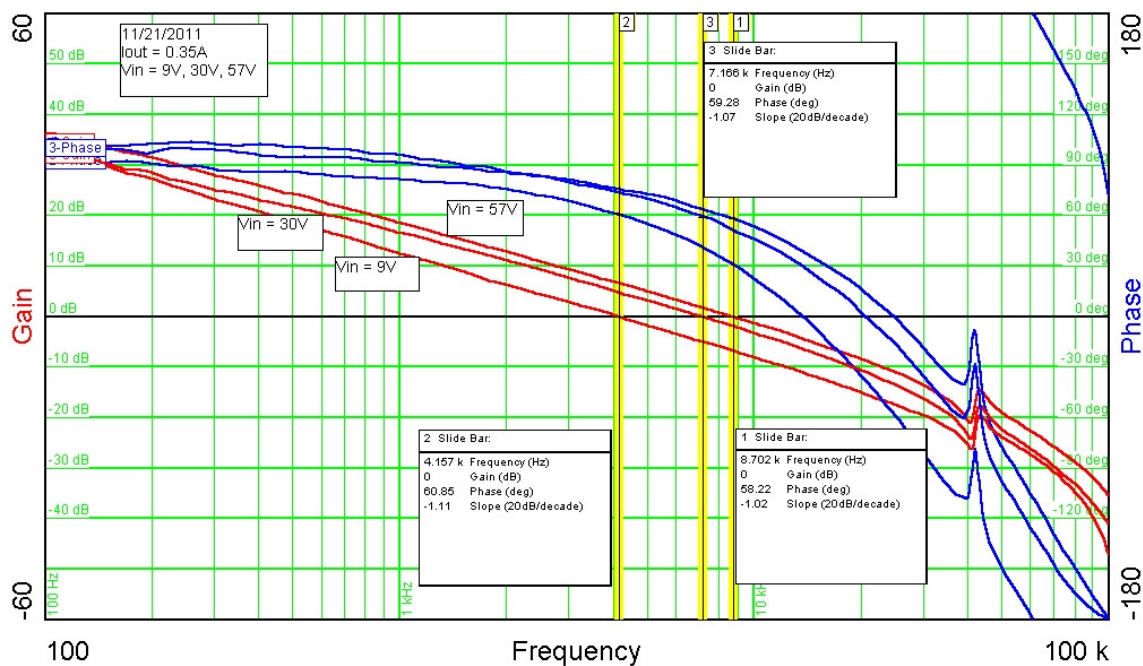
The photos below show the FET drain voltage at TP3. The input voltage is 57V and the output is loaded to 0.05A. (20V/DIV, 2uS/DIV)



6 Loop Gain

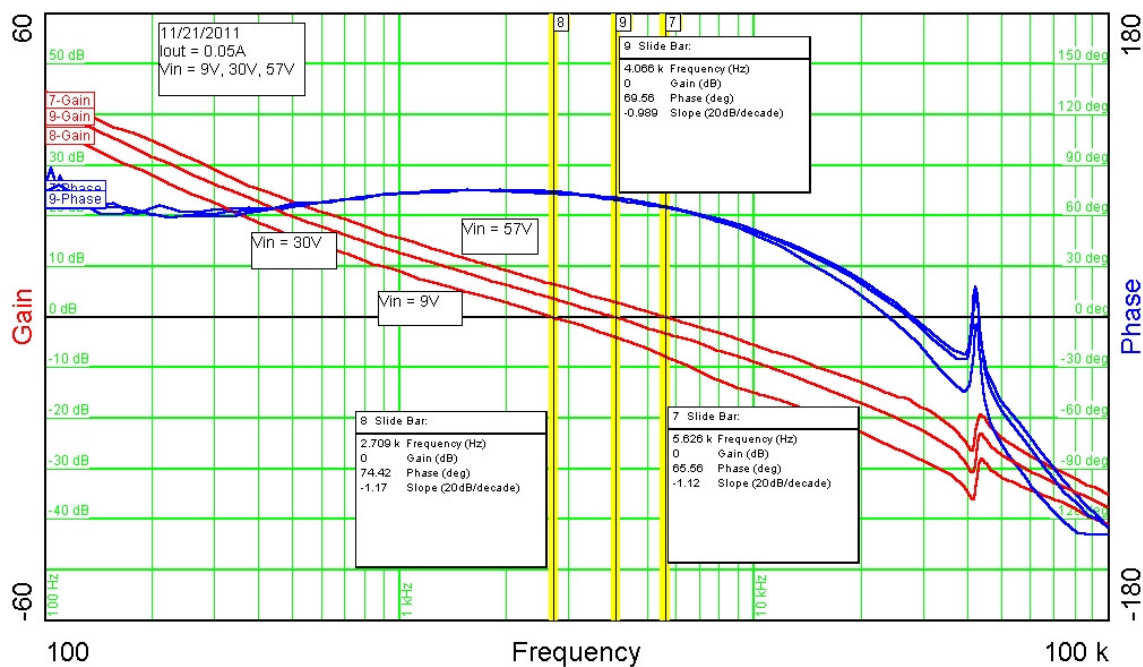
The closed loop gain is plotted below for an output current of 0.35A and input voltages of 9V, 30V, and 57V.

Bandwidth = 4.16KHz	Phase Margin = 61 degrees	(Vin = 9V)
Bandwidth = 7.17KHz	Phase Margin = 59 degrees	(Vin = 30V)
Bandwidth = 8.70KHz	Phase Margin = 58 degrees	(Vin = 57V)



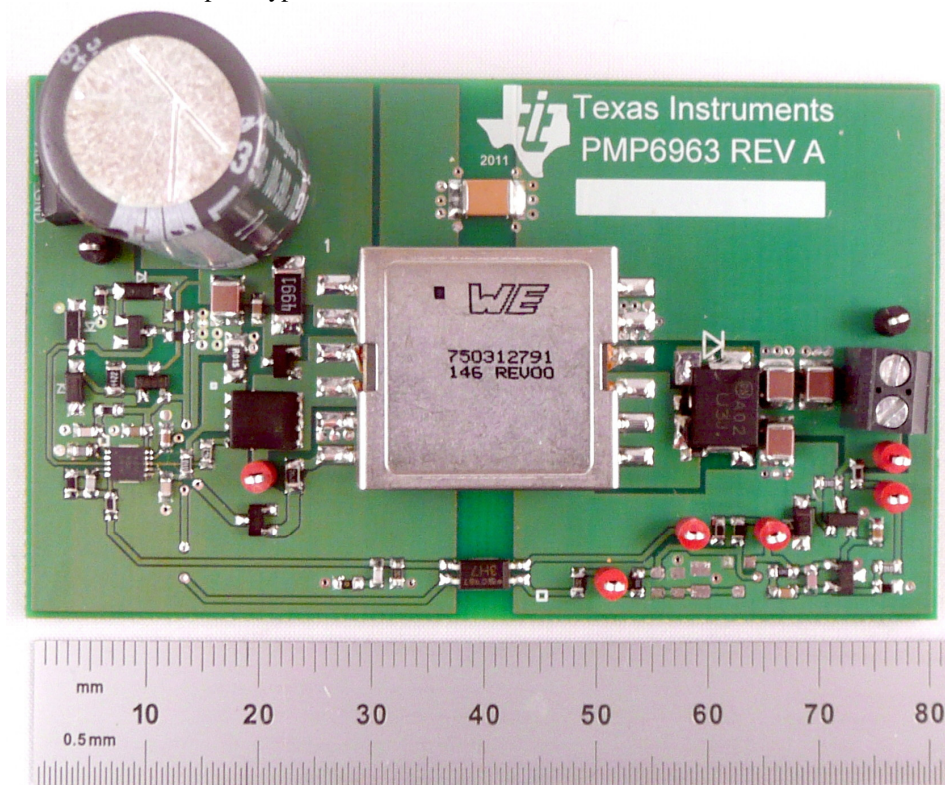
The closed loop gain is plotted below for an output current of 0.05A and input voltages of 9V, 30V, and 57V.

Bandwidth = 2.71KHz	Phase Margin = 74 degrees	(Vin = 9V)
Bandwidth = 4.07KHz	Phase Margin = 70 degrees	(Vin = 30V)
Bandwidth = 5.63KHz	Phase Margin = 66 degrees	(Vin = 57V)



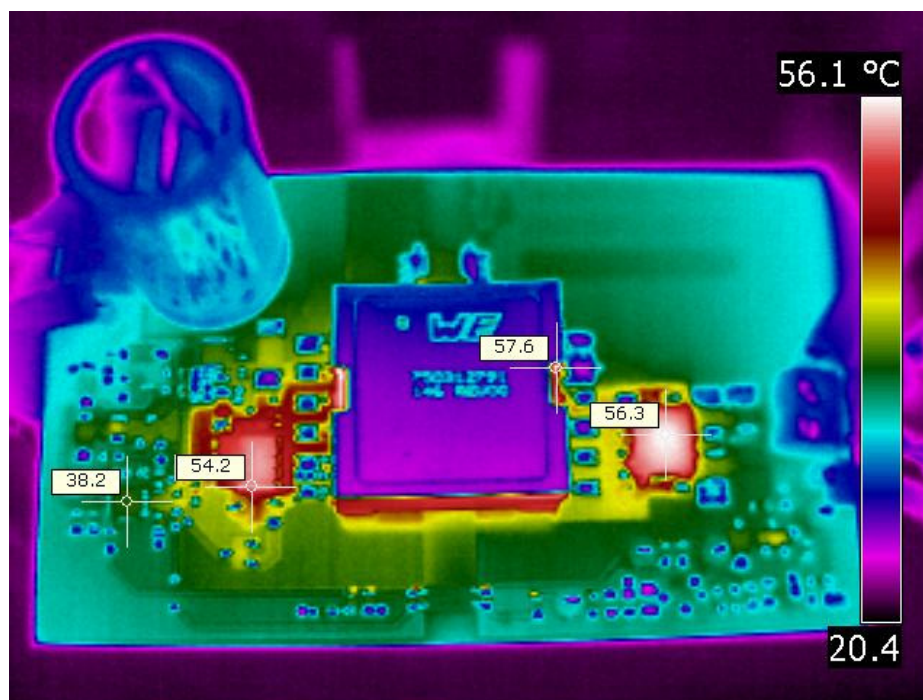
7 Photo

The photo below shows the prototype PMP6963 REVB circuit.

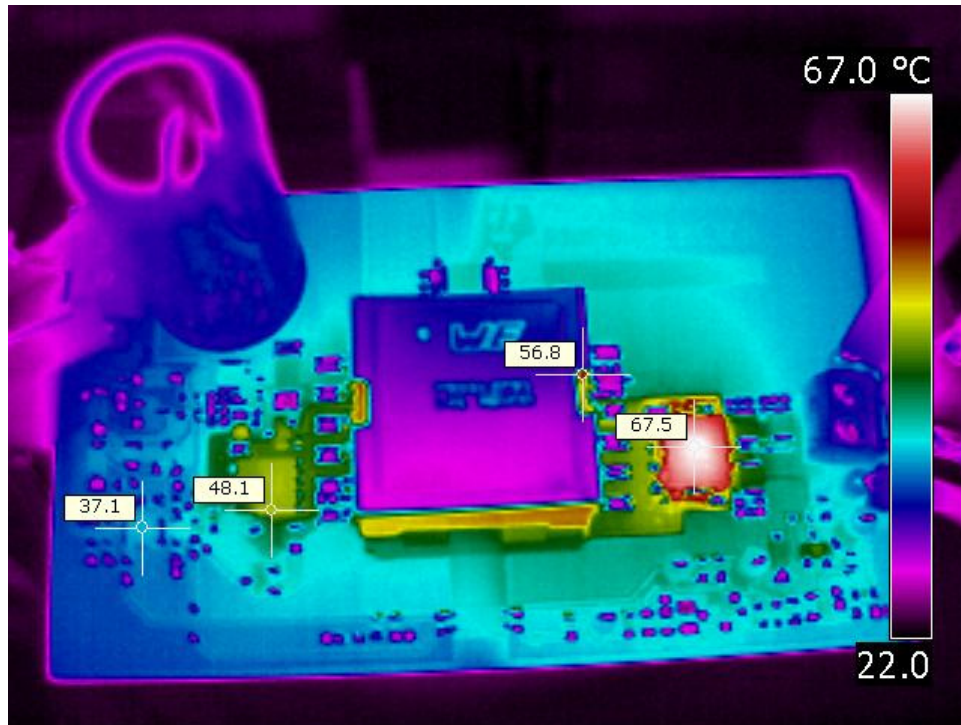


8 Thermal Image

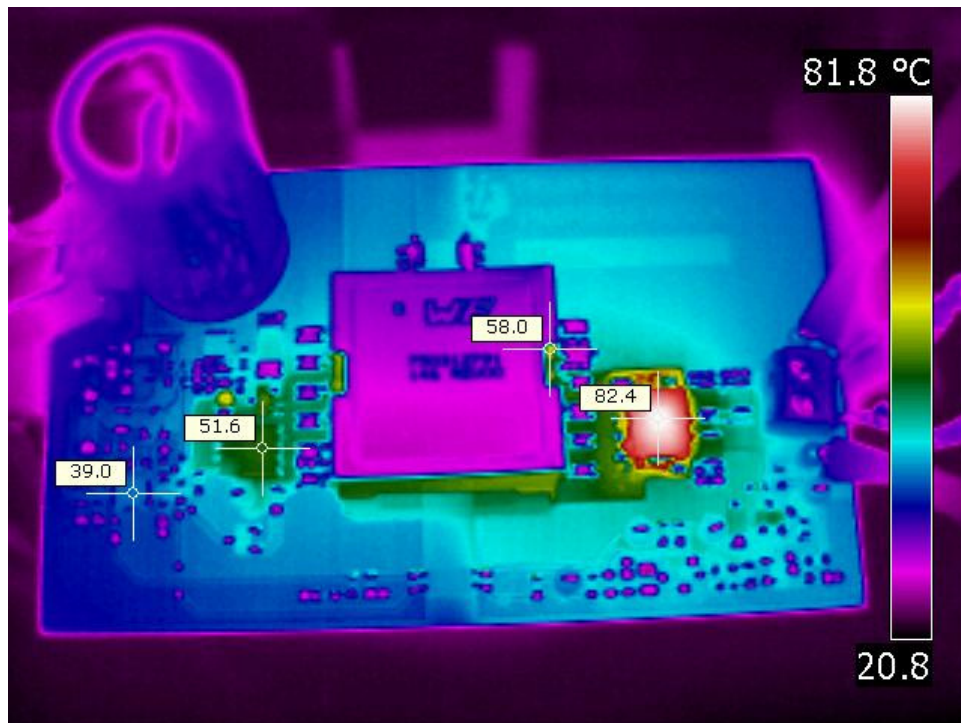
A thermal image is shown below when operating at 48V input and 0.35A output.



A thermal image is shown below when operating at 24V input and 0.35A output.



A thermal image is shown below when operating at 12V input and 0.35A output.



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