

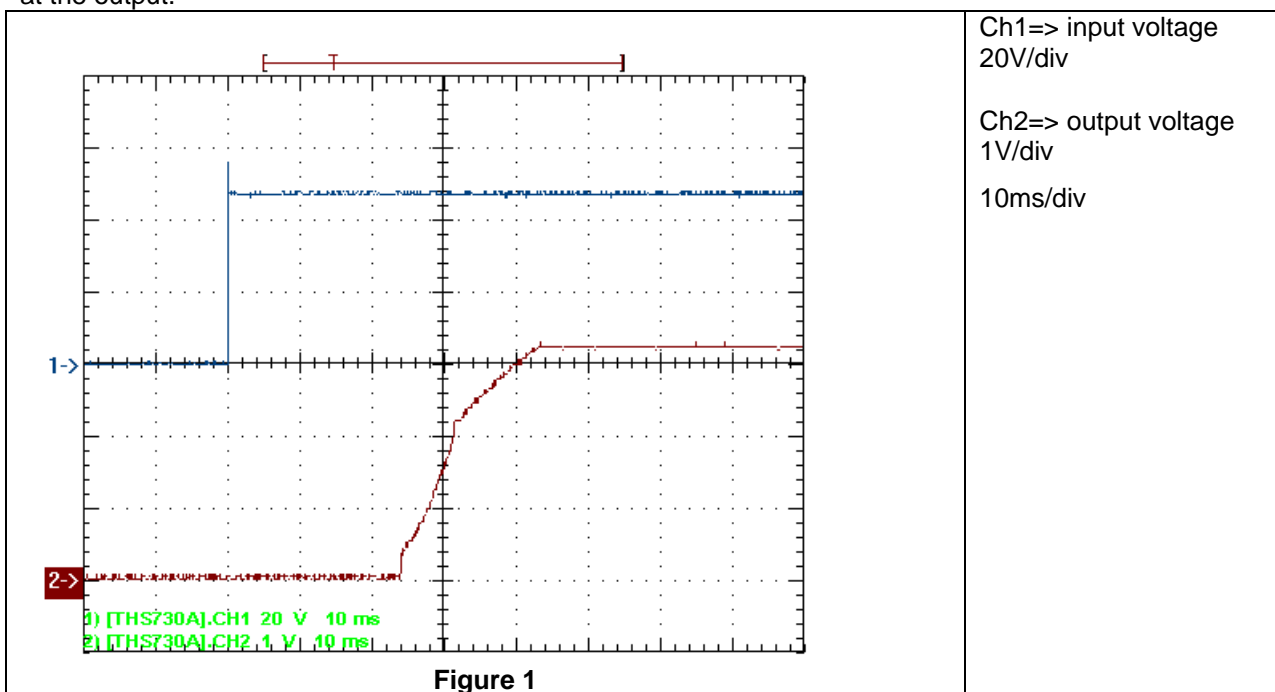
PMP7094RevB Test Results

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Topology: Active Clamp Forward
Device: UCC2897A, TLV431A

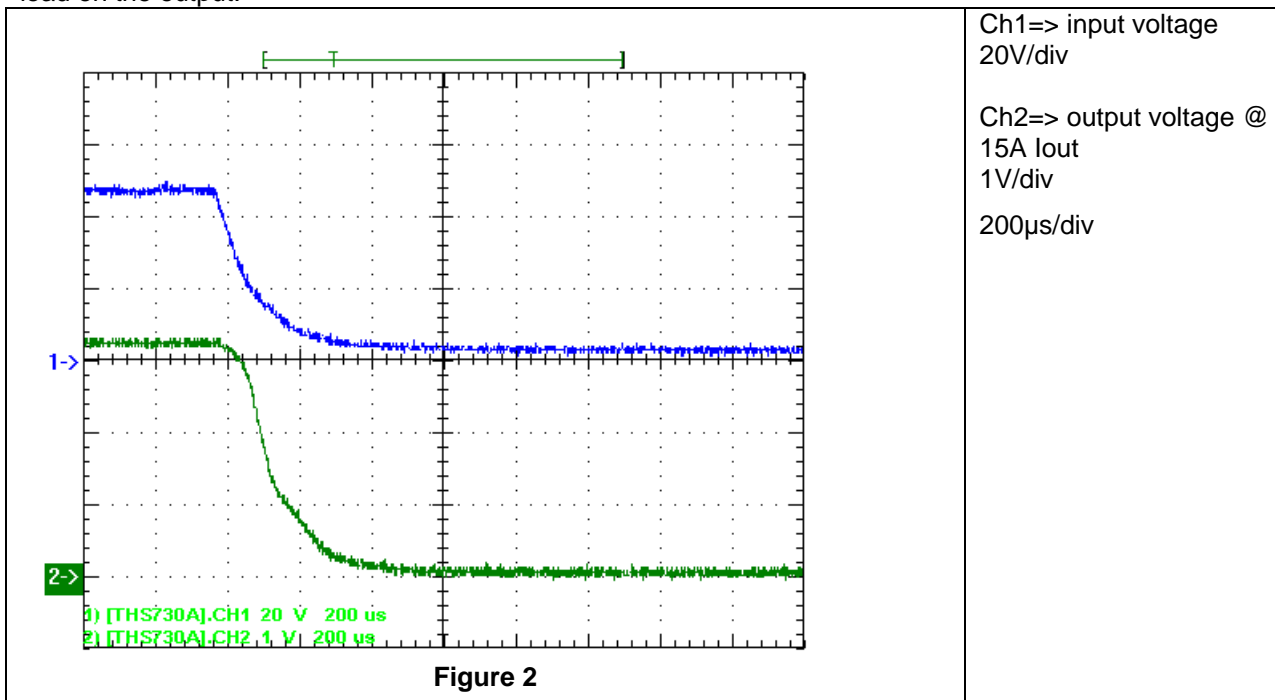
1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 48V, with 15A load at the output.



2 Shutdown

The shutdown waveform is shown in the Figure 2. The input voltage was set at 48V, with 15A load on the output.



3 Efficiency

The efficiency is shown in the Figure 3 below. The curves represent different input voltages.

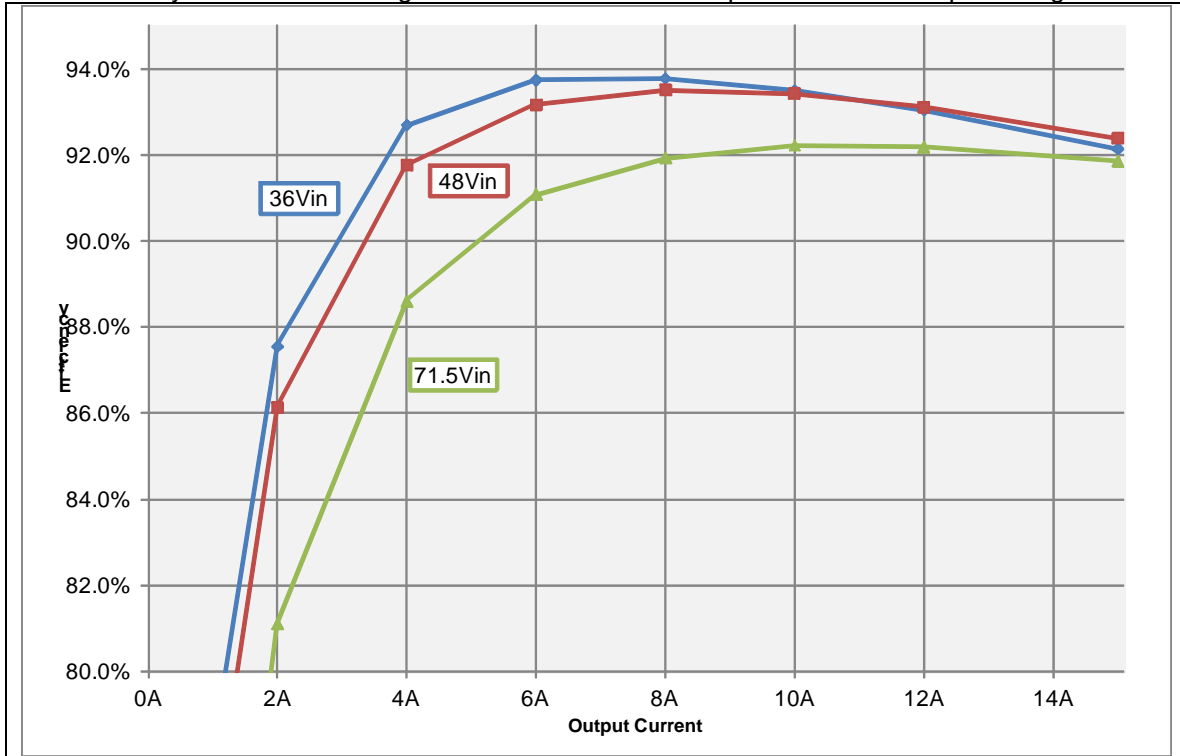


Figure 3

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4 Load Regulation

The load regulation of the output is shown in the Figure 4 below. The curves represent different input voltages.

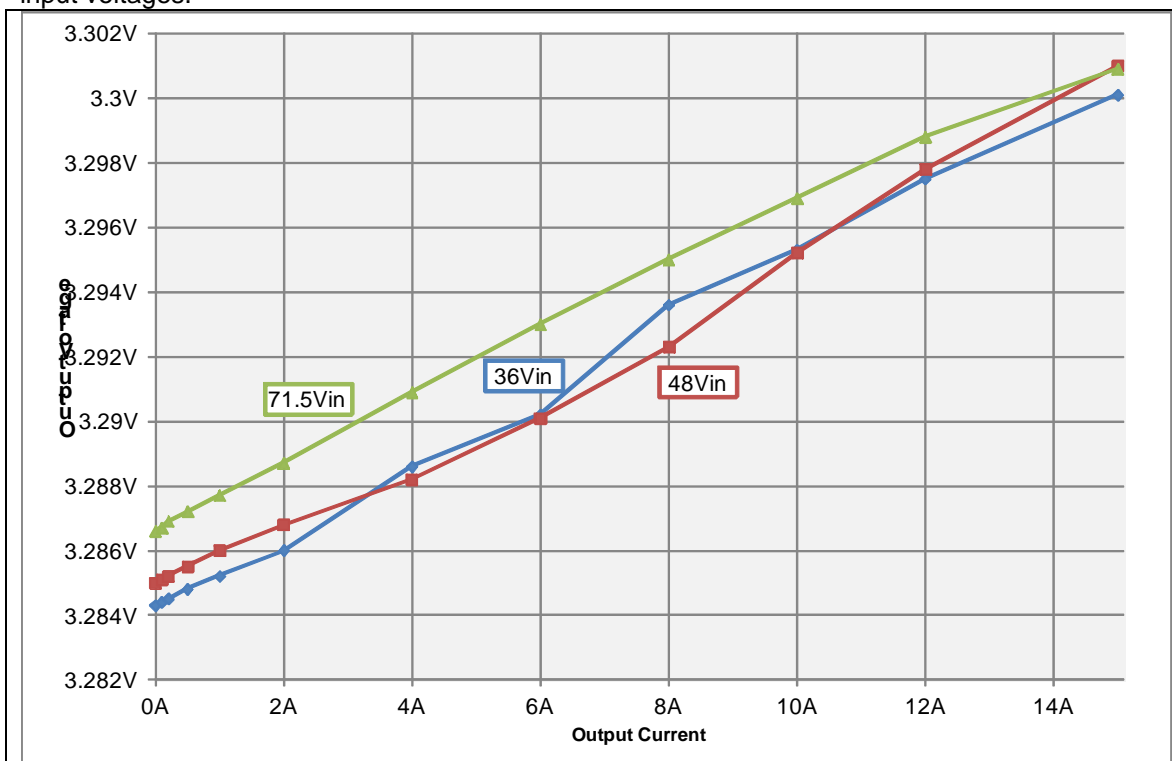


Figure 4

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5 Line Regulation

The dependency of the output voltage to the input voltage shows Figure 5. The current was set to 15A.

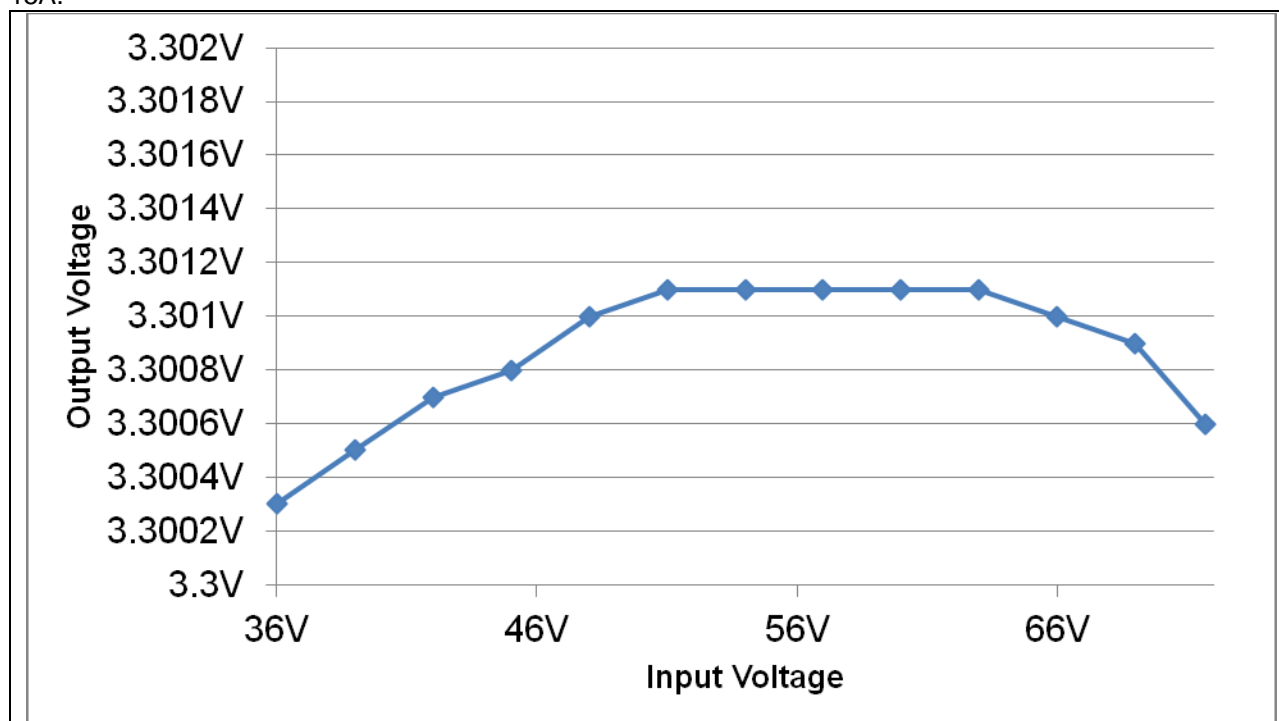


Figure 5

With the measurement above also the efficiencies were calculated.

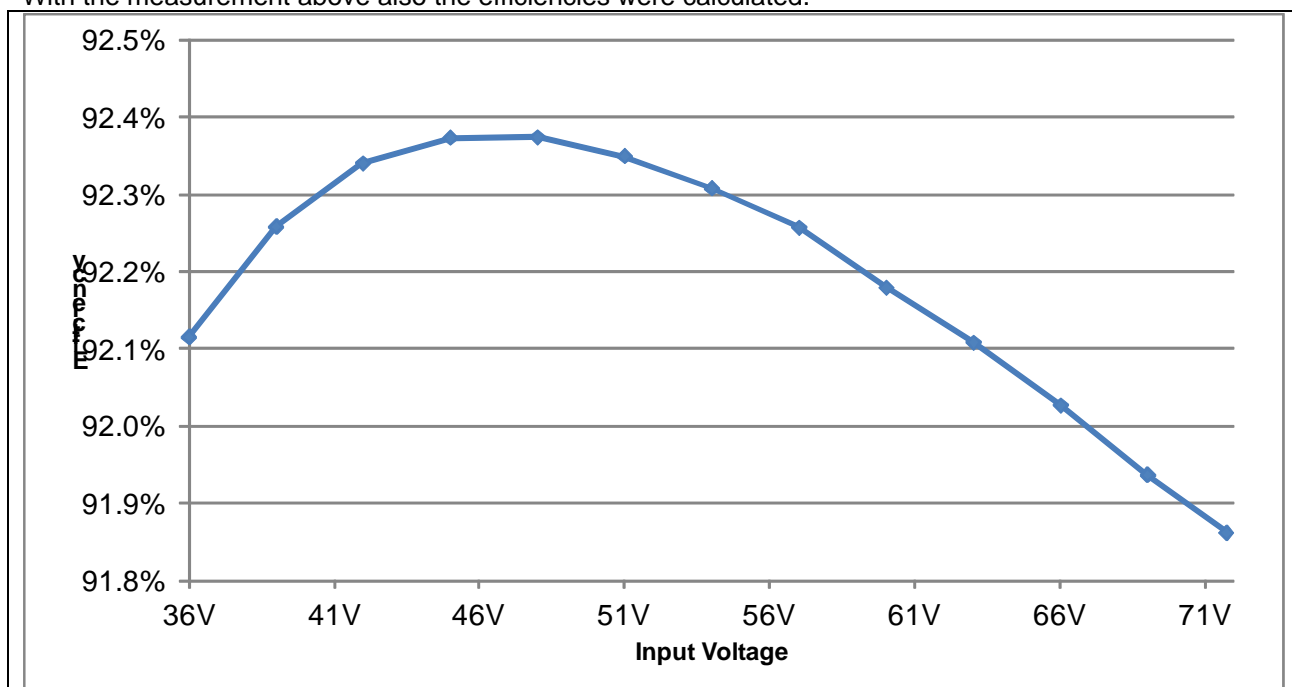


Figure 6

6 Ripple Voltage

The output ripple voltage is shown in Figure 7. The image was taken with a 15 A load and 36, 48V and 72V at the input. Curves were captured separately.

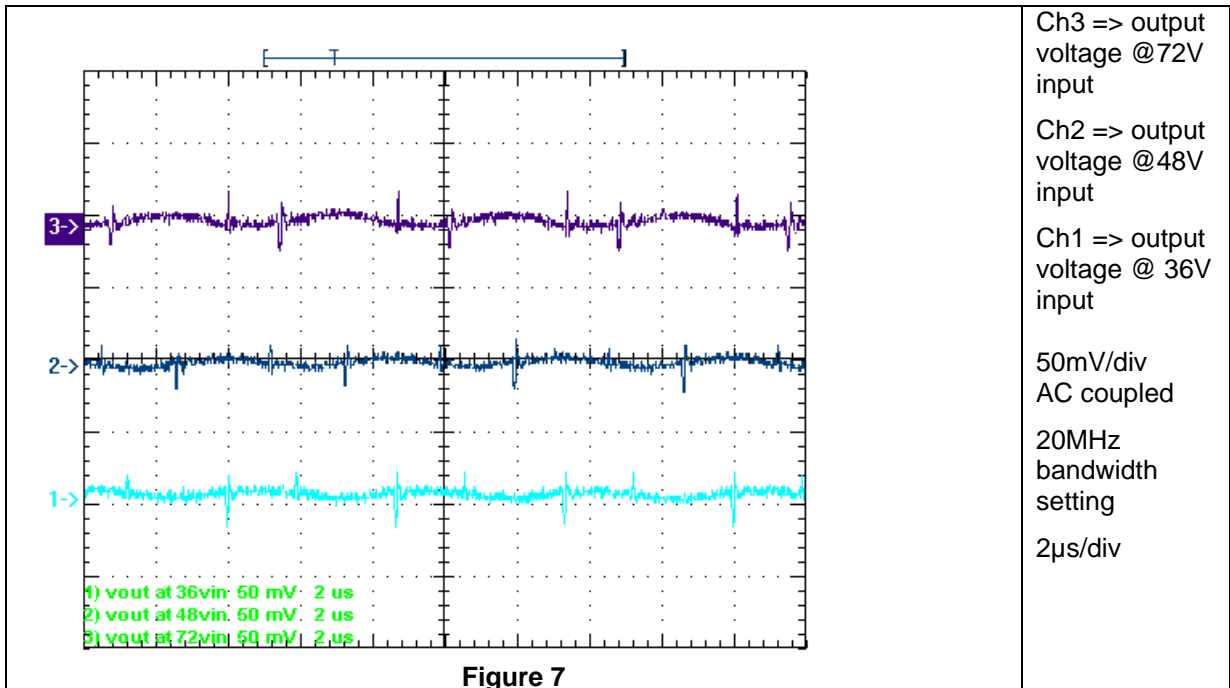


Figure 7

The input ripple voltage is shown in Figure 8. The image was taken with a 15 A load and 36, 48V and 72V at the input. Curves were captured separately – no additional bulk cap.

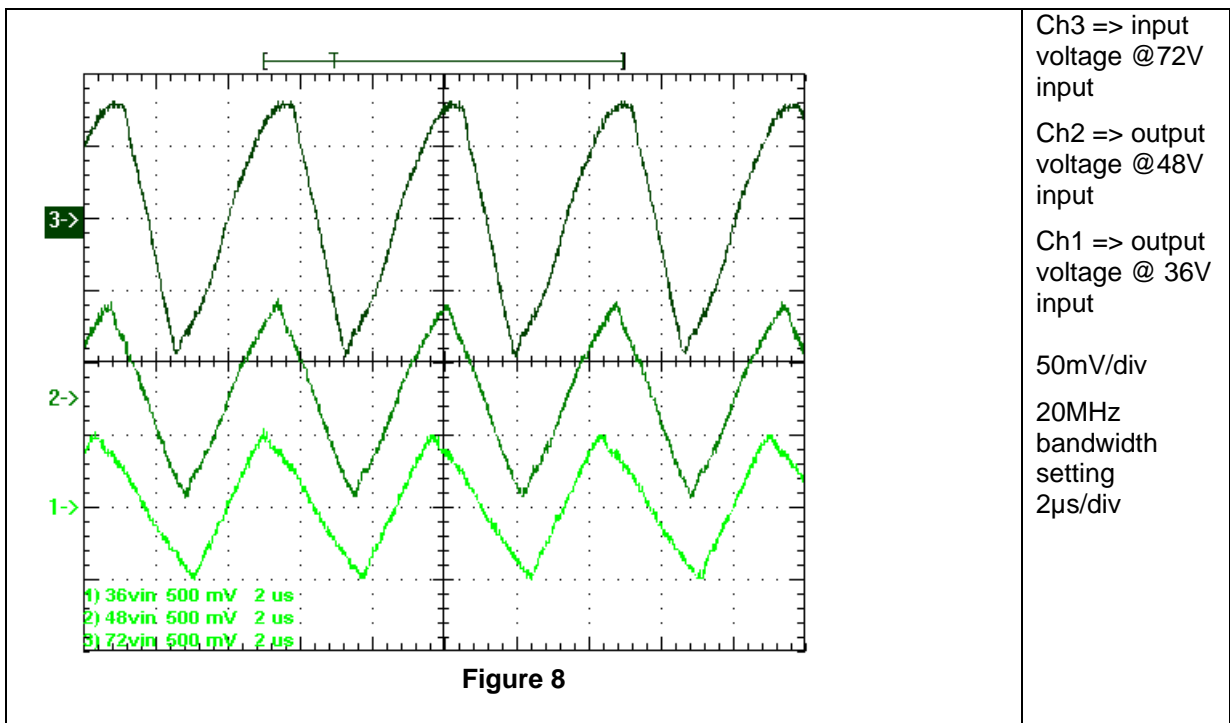


Figure 8

7 Control Loop Frequency Response

Figure 9 shows the loop response with 15A load and 48V input.

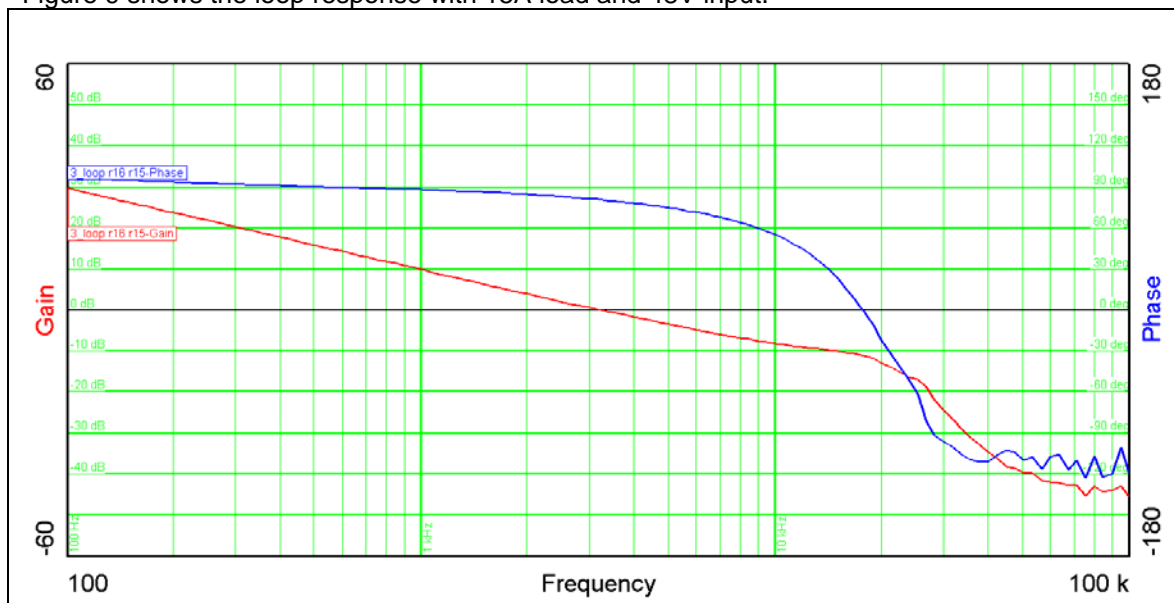


Figure 9

Table 1 summarizes the results from Figure 9

Bandwidth (kHz)	3.2
Phasemargin slope (20dB/decade)	80.8
gain margin (dB)	-0.95
gain margin slope (20dB/decade)	-11.2
gain margin freq (kHz)	-1.11
gain margin	17.7

Table 1

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8 Load Transients

The Figure 10 shows the response to load transients. The load is switching from 7.5A to 15A. with 400Hz frequency. The input voltage was set to 48V

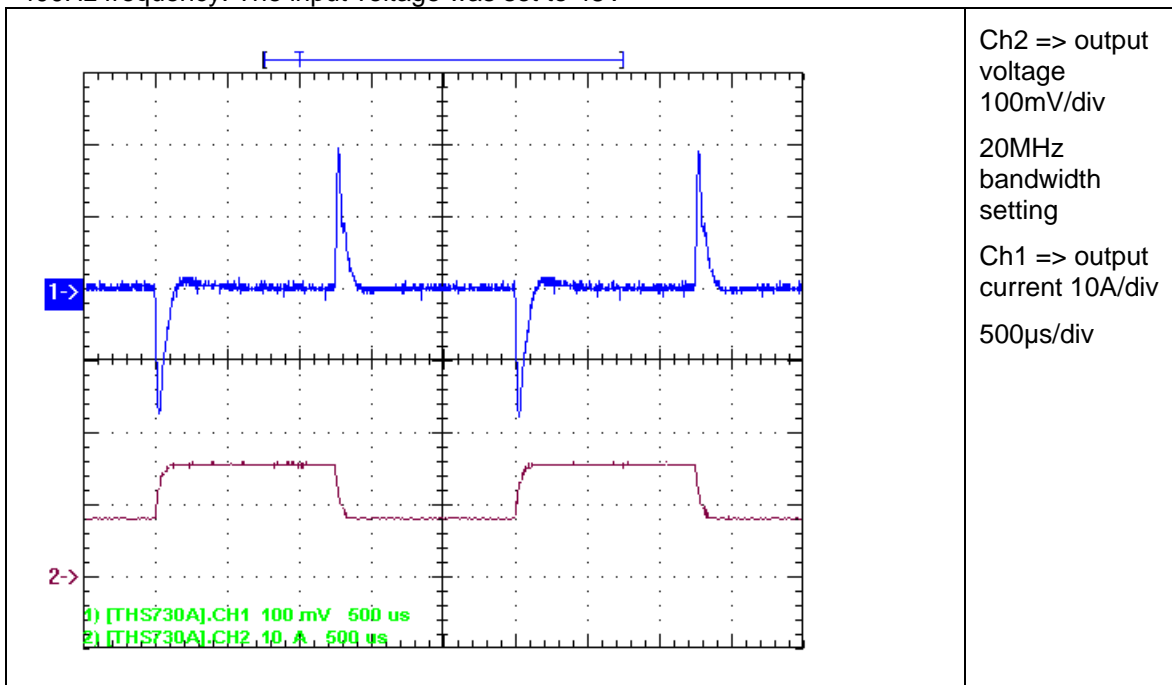


Figure 10

9 Miscellaneous Waveforms

9.1 Switch node primary side

With input voltage set to 48V and 15A lout results in the waveform shown in Figure 11 (primary side).

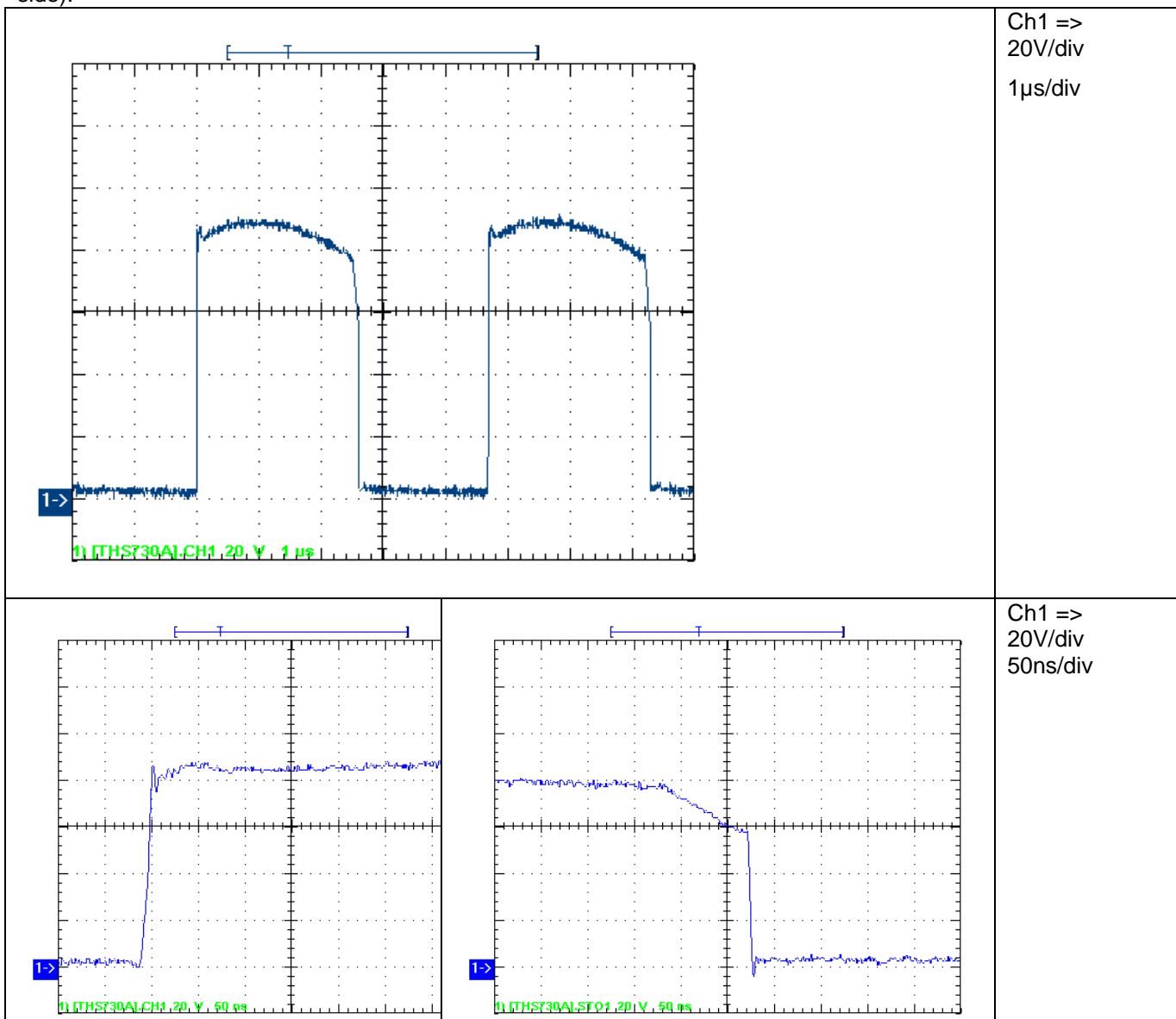


Figure 11

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9.2 Gate of primary MOS-FET

With input voltage set to 48V and 15A lout results in the waveform shown in Figure 11 (primary side).

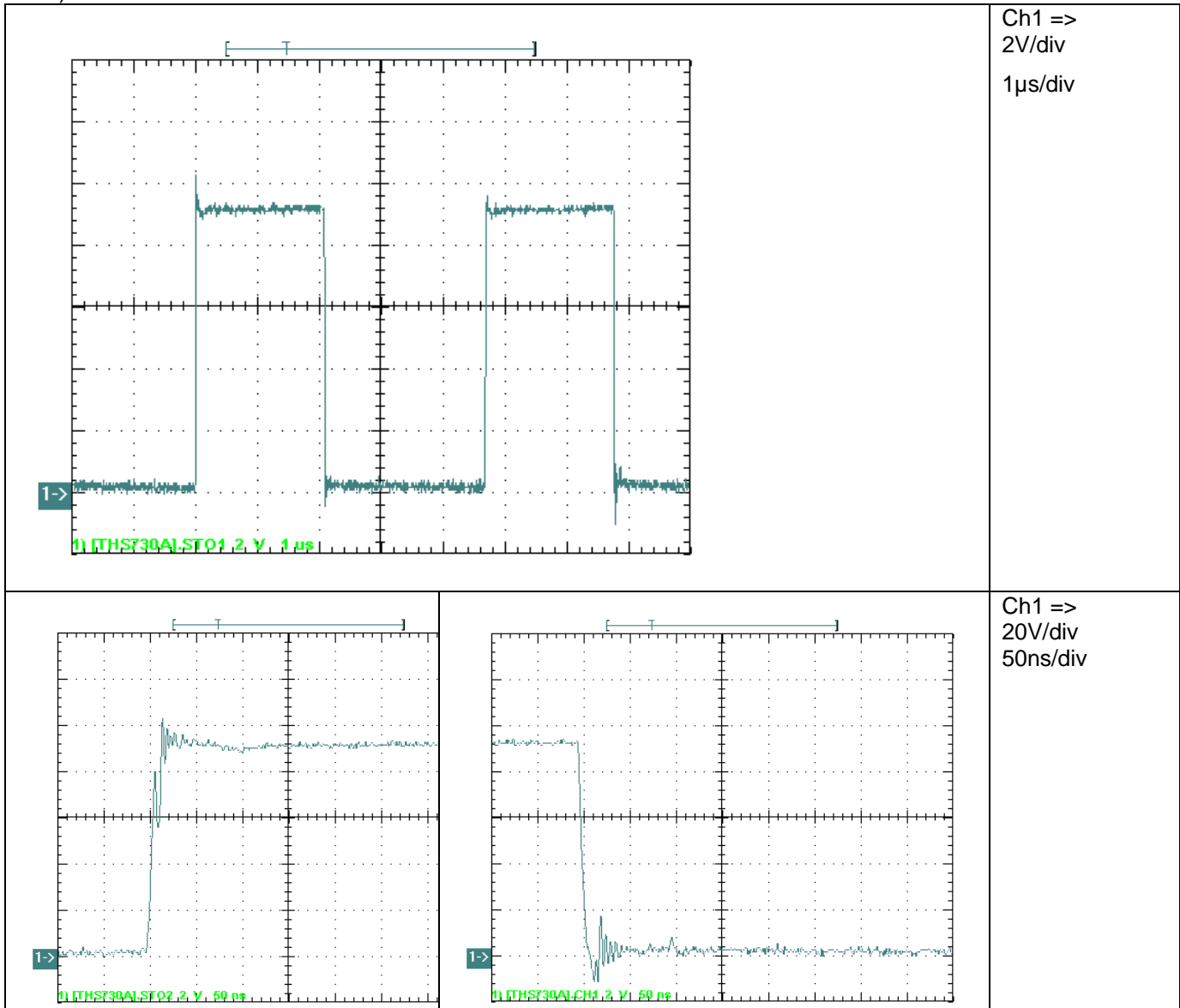


Figure 12

9.3 Active clamp

The waveform of the active clamp transistor is shown in **Figure 13**. (the same setup as above)

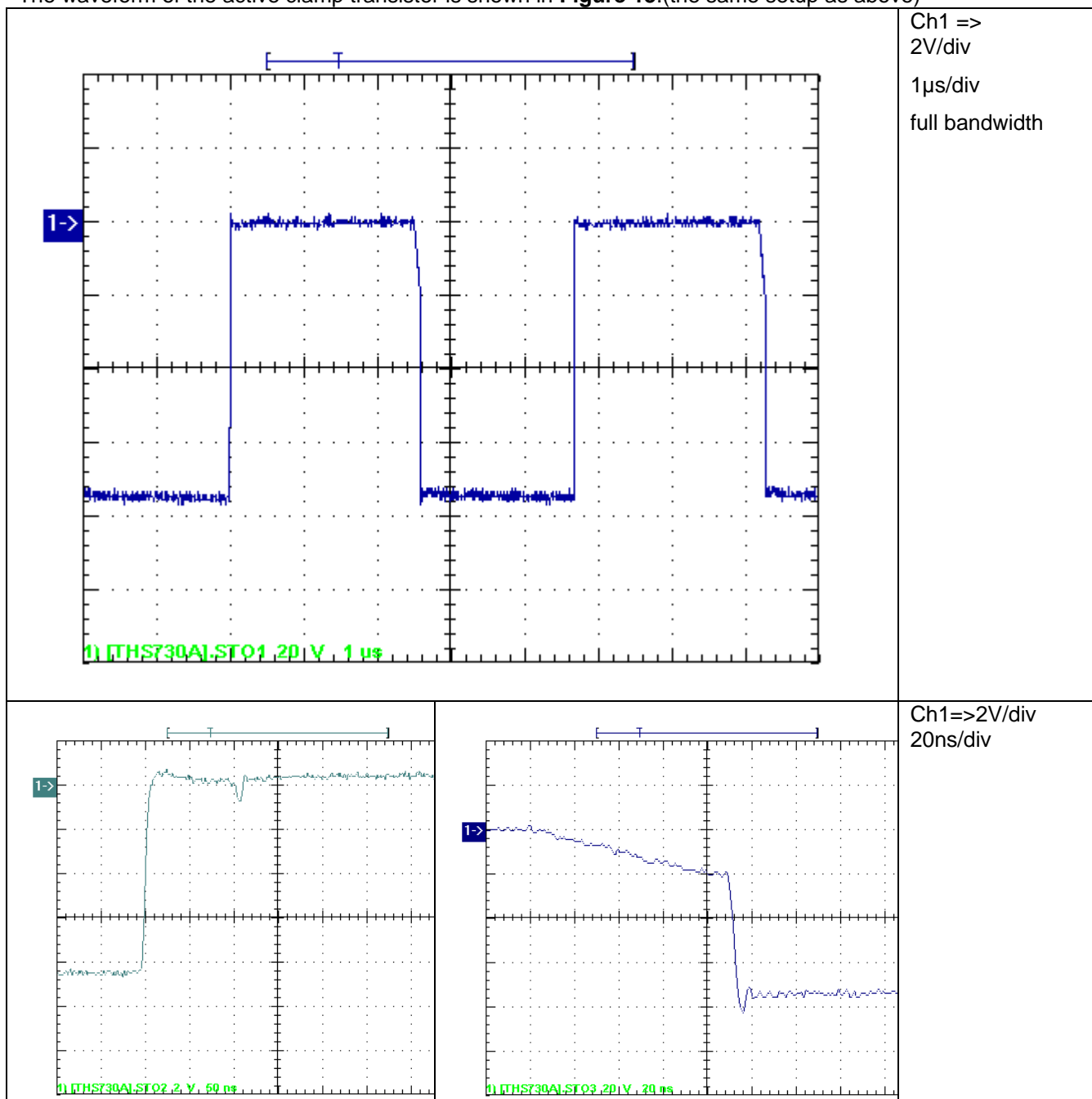


Figure 13

9.4 Active Clamp Gate

The waveform of the active clamp transistor is shown in Figure 14.

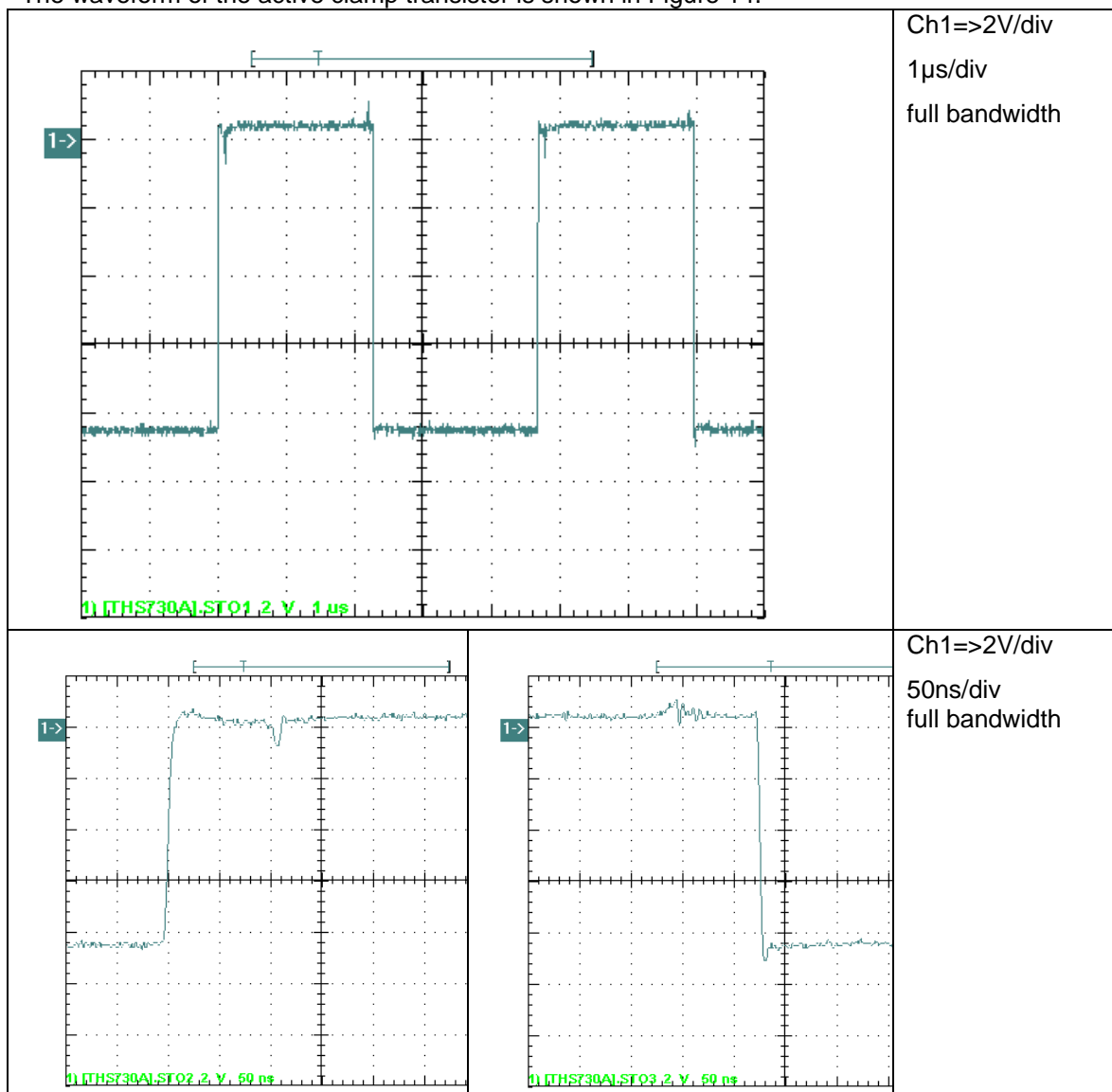


Figure 14

9.5 Secondary Switch node

The waveform of the secondary side switchnode is shown in Figure 15.

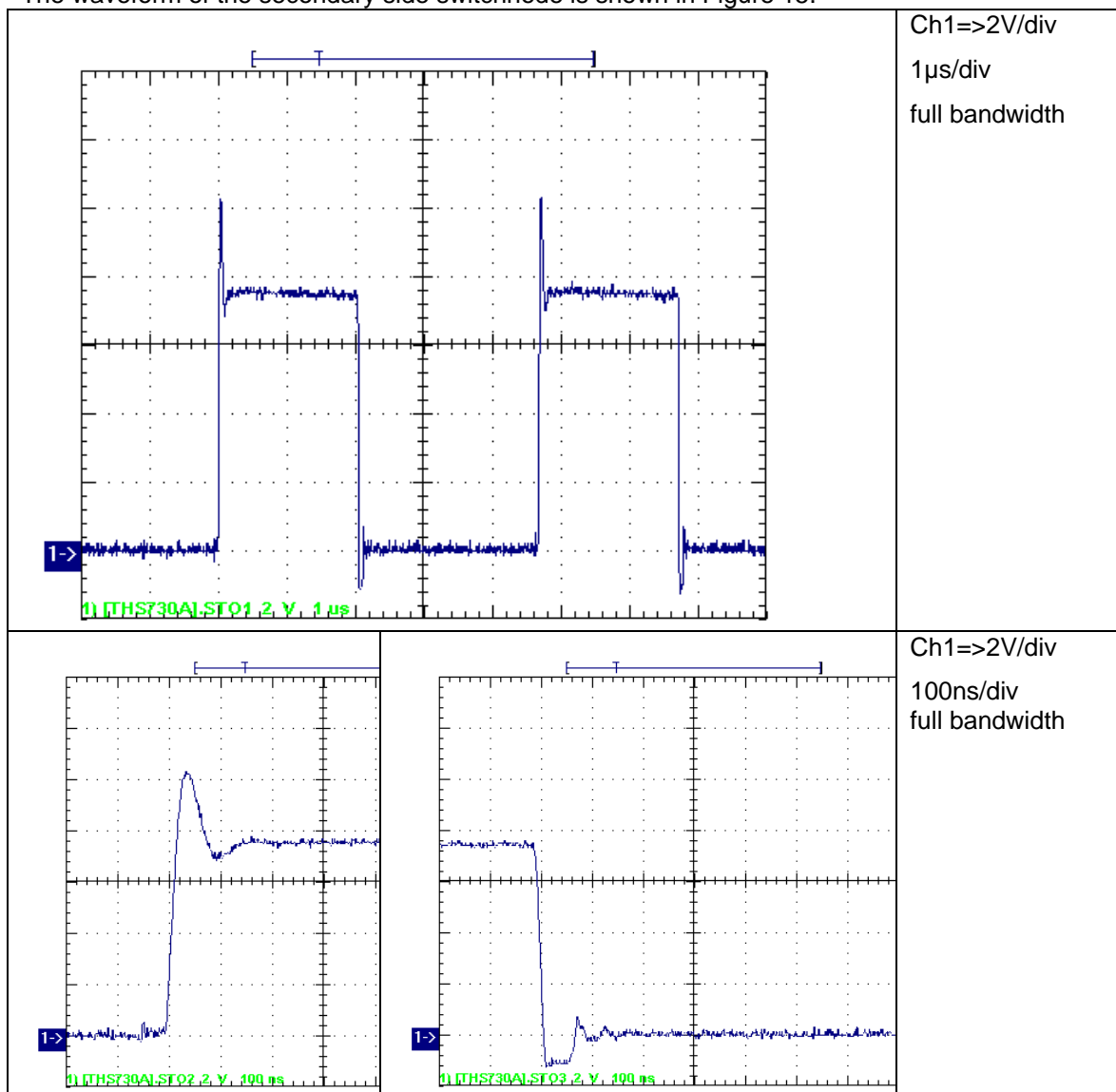


Figure 15

9.6 Q1 gate

The waveform of Q1 gate is shown in Figure 16

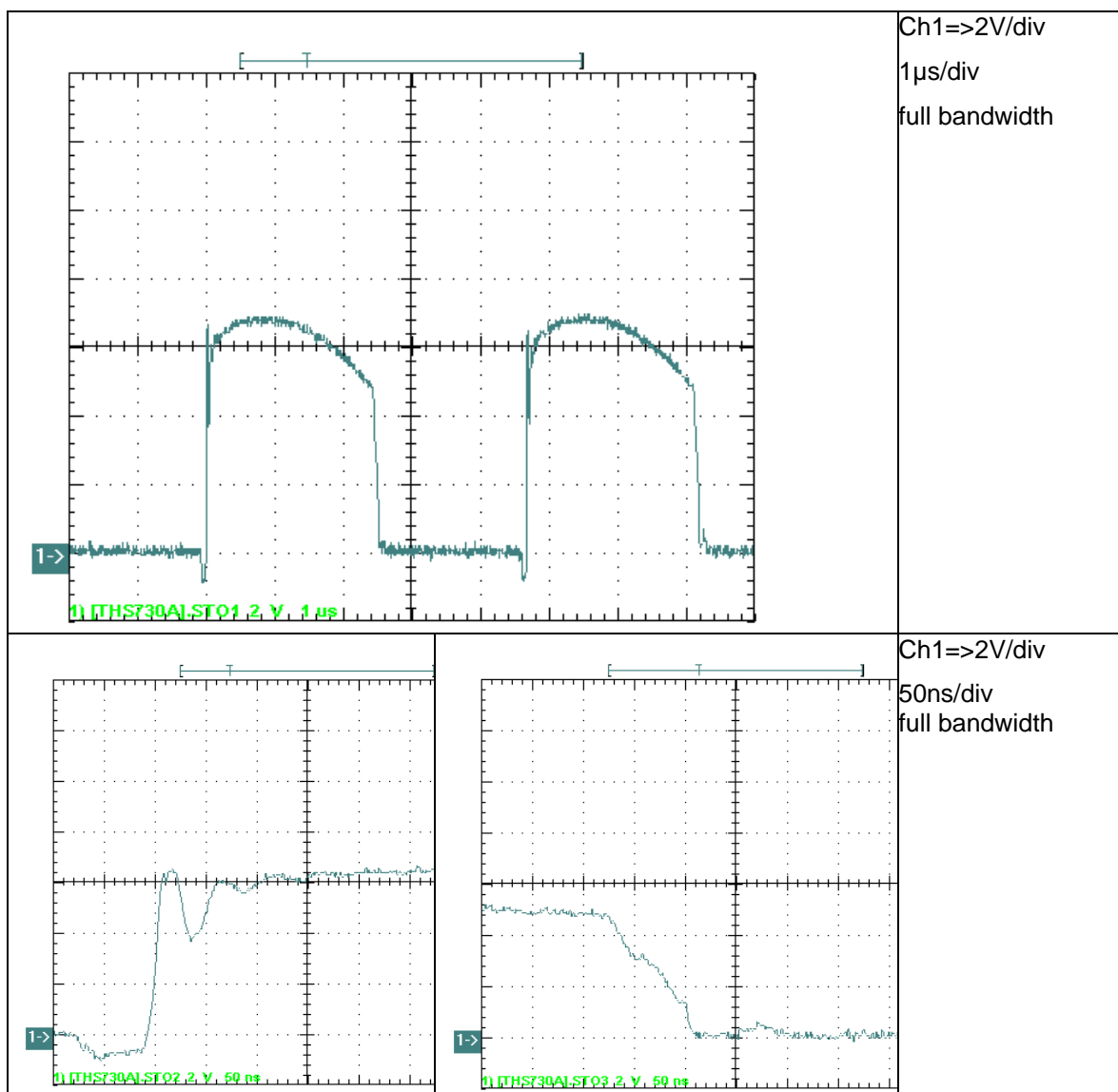


Figure 16

9.7 Q2

The waveform of the Q2 is shown in Figure 17.

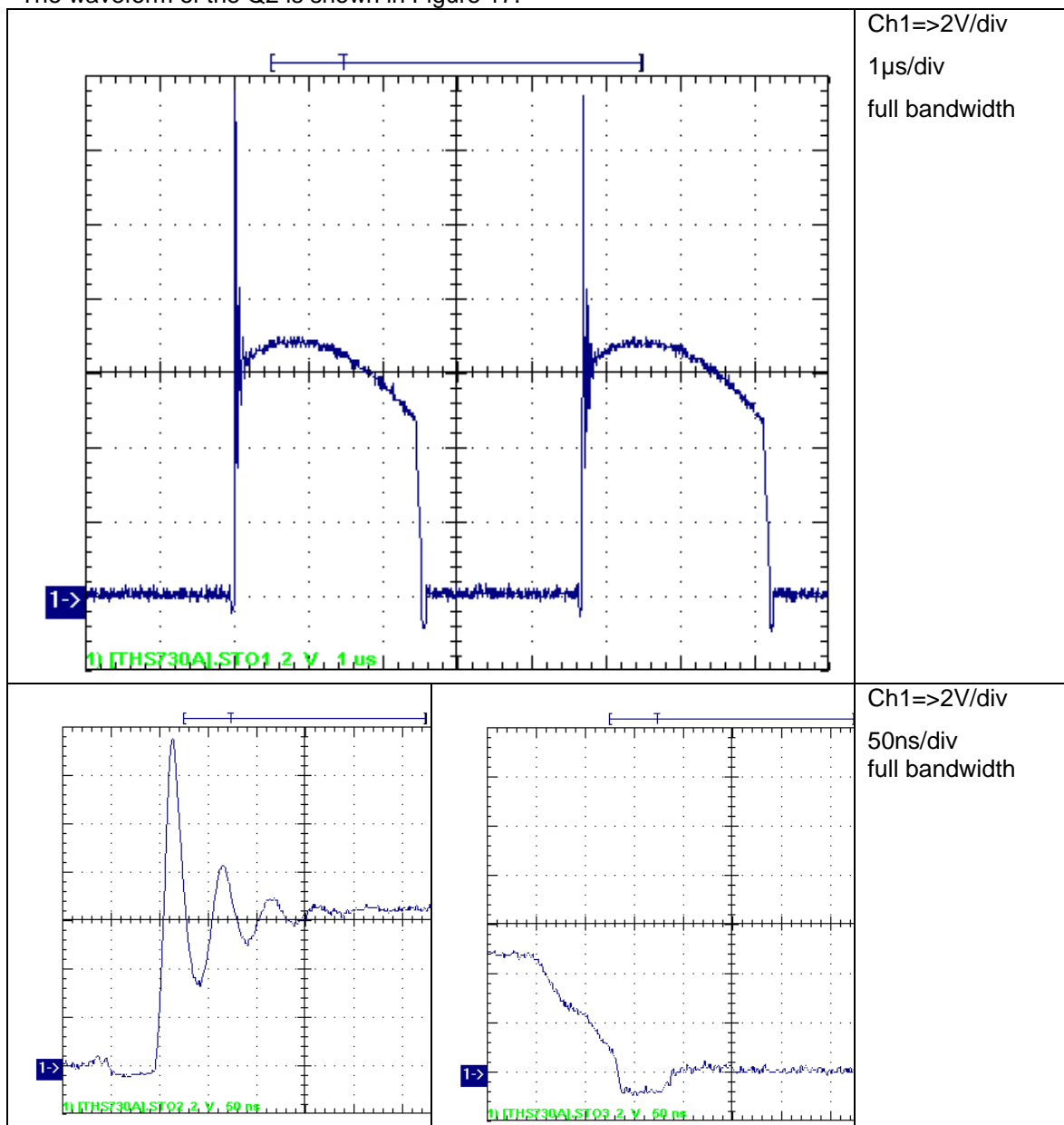
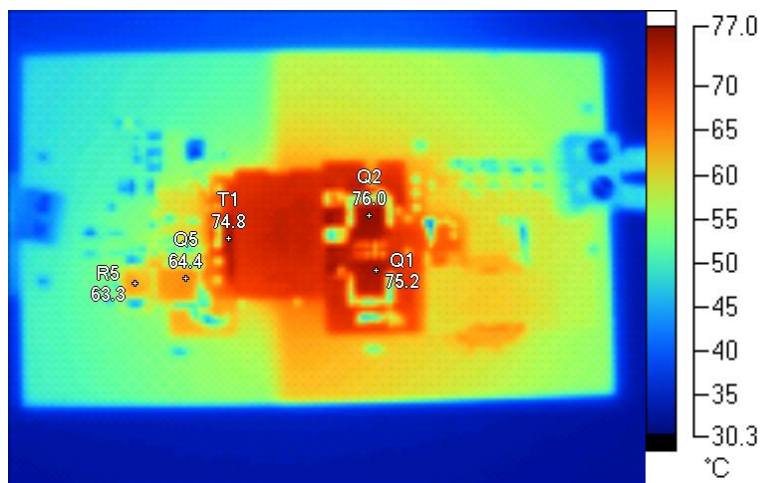


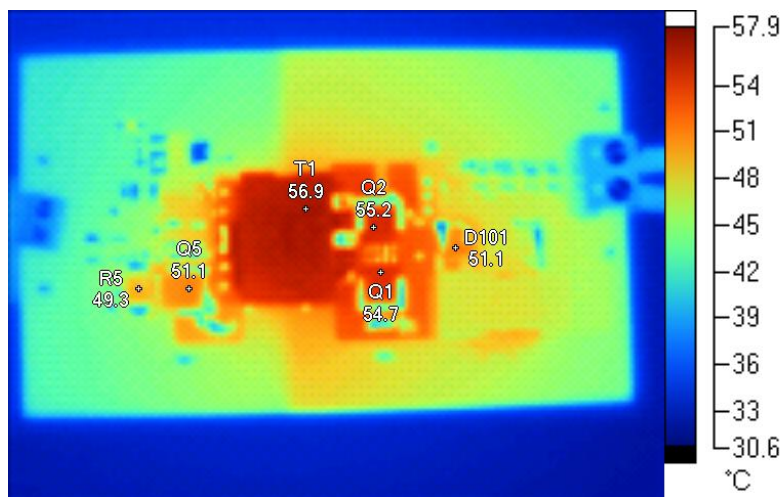
Figure 17

10.1 Thermal Images, here full load 15Amps, natural convection:



Name	Temperature
Q2	76.0°C
Q1	75.2°C
T1	74.8°C
Q5	64.4°C
R5	63.3°C

10.2 Thermal Images, here 10Amps load, natural convection:



Name	Temperature
T1	56.9°C
Q2	55.2°C
Q1	54.7°C
Q5	51.1°C
R5	49.3°C
D101	51.1°C

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