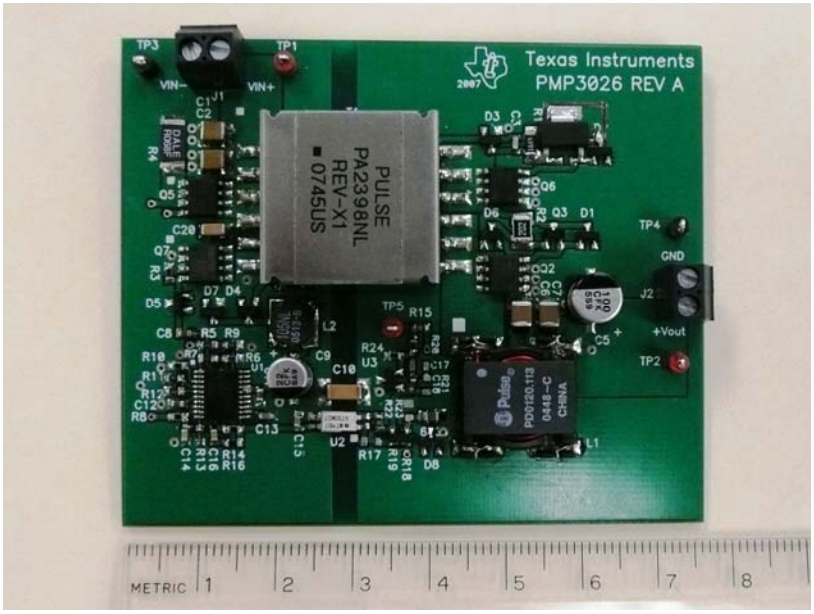
1 Photo

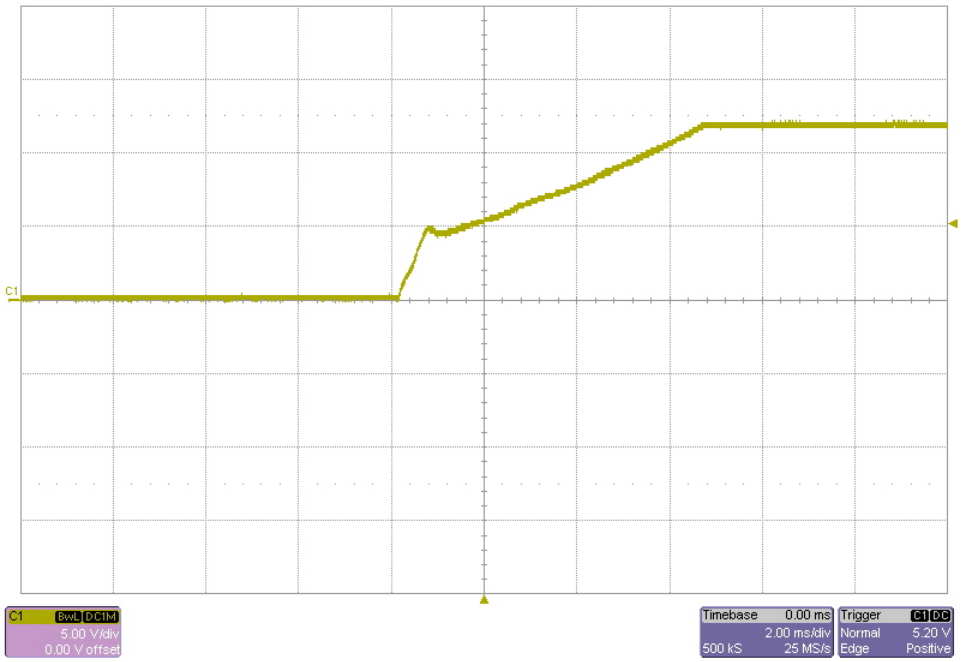
The photograph below shows a top view of the PMP4752 Rev B demo board. The circuit is built on a PMP3026 Rev A PWB.



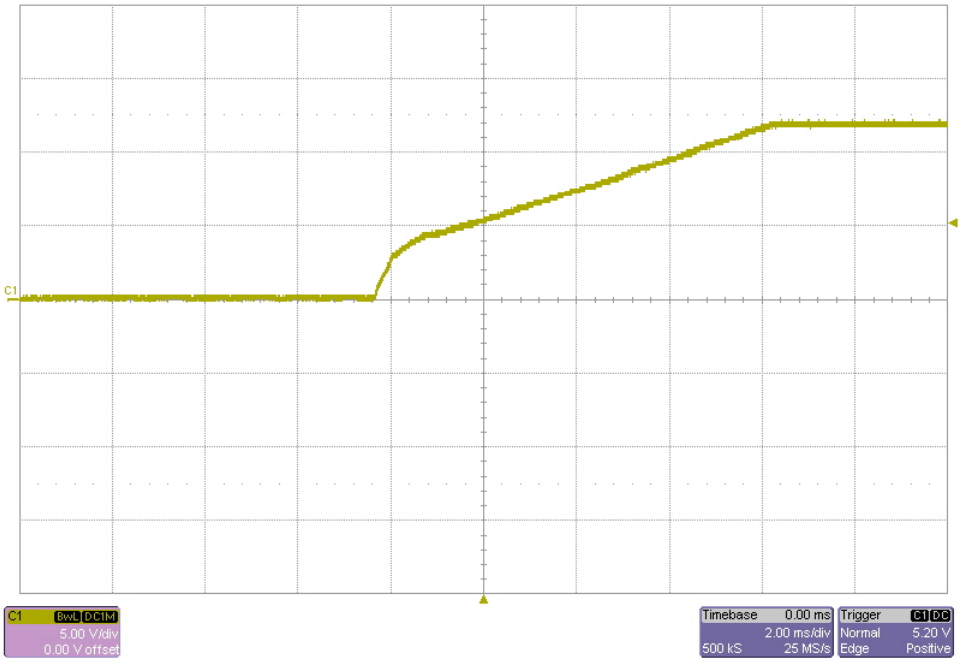
2 Startup

The output voltage at startup is shown in the images below. The input was 70VDC.

2.1 No Load

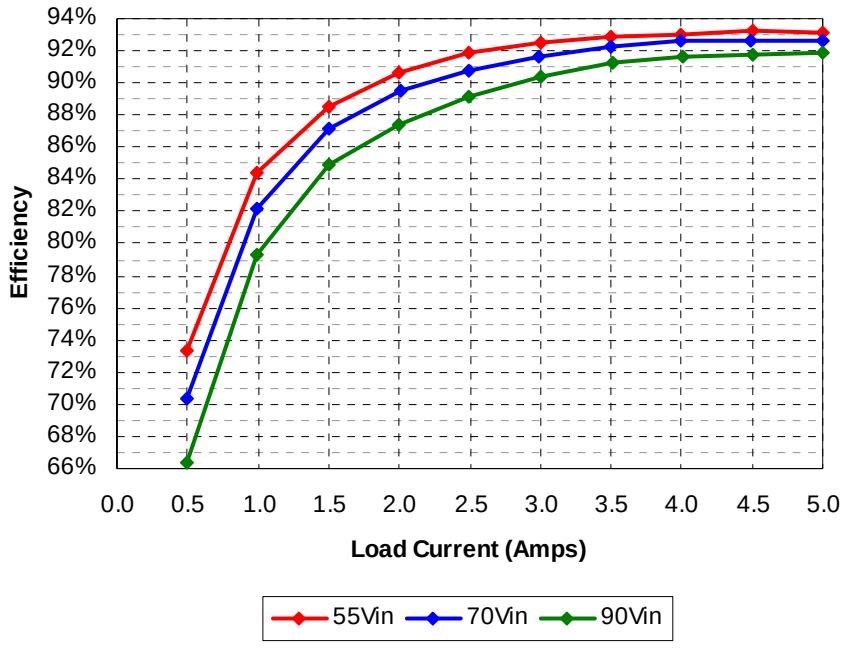


2.2 Full Load



3 Efficiency

The efficiency data is shown in the tables and graph below.



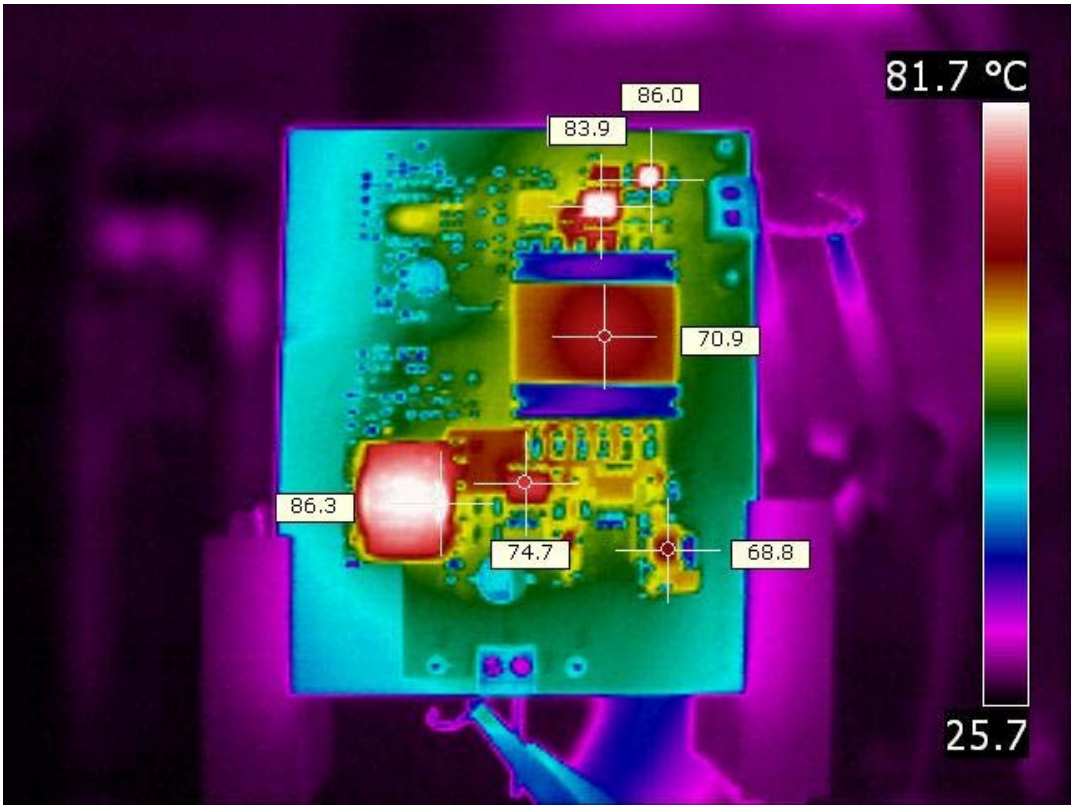
Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	12.02	54.98	0.040	0.00	2.199	0.0%
0.500	12.01	54.99	0.149	6.01	2.189	73.3%
0.998	12.01	55.00	0.258	11.99	2.204	84.5%
1.503	12.01	54.98	0.371	18.05	2.347	88.5%
2.004	12.01	54.99	0.483	24.07	2.492	90.6%
2.490	12.01	55.00	0.592	29.90	2.655	91.8%
3.006	12.01	55.02	0.709	36.10	2.907	92.5%
3.501	12.01	55.00	0.823	42.05	3.218	92.9%
3.998	12.01	55.01	0.938	48.02	3.583	93.1%
4.50	12.01	55.02	1.054	54.05	3.946	93.2%
5.00	12.01	55.00	1.173	60.05	4.465	93.1%

Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	12.01	70.0	0.036	0.00	2.520	0.0%
0.500	12.01	70.0	0.122	6.01	2.535	70.3%
0.997	12.01	70.0	0.208	11.97	2.586	82.2%
1.503	12.01	70.0	0.296	18.05	2.669	87.1%
2.014	12.01	70.0	0.386	24.19	2.832	89.5%
2.498	12.01	70.0	0.472	30.00	3.039	90.8%
2.995	12.01	70.0	0.561	35.97	3.300	91.6%
3.496	12.01	70.0	0.650	41.99	3.513	92.3%
3.998	12.01	70.0	0.741	48.02	3.854	92.6%
4.49	12.01	70.0	0.832	53.92	4.315	92.6%
5.00	12.01	70.0	0.926	60.05	4.770	92.6%

Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	12.01	90.0	0.034	0.00	3.060	0.0%
0.497	12.01	90.0	0.100	5.97	3.031	66.3%
0.998	12.01	90.0	0.168	11.99	3.134	79.3%
1.508	12.01	90.0	0.237	18.11	3.219	84.9%
1.999	12.01	90.0	0.305	24.01	3.442	87.5%
2.499	12.01	90.0	0.374	30.01	3.647	89.2%
3.000	12.01	90.0	0.443	36.03	3.840	90.4%
3.506	12.01	90.0	0.513	42.11	4.063	91.2%
4.008	12.01	90.0	0.584	48.14	4.424	91.6%
4.50	12.01	90.0	0.654	54.05	4.815	91.8%
5.00	12.01	90.0	0.726	60.05	5.290	91.9%

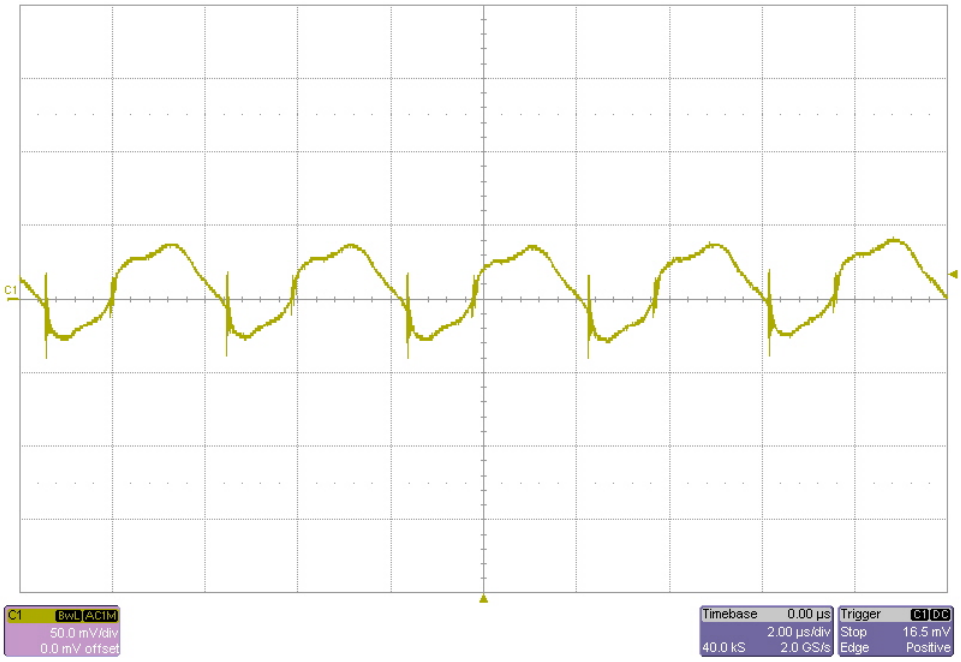
4 Thermal Image

The image below shows a top thermal image of the board. The ambient temperature was 26ºC with no forced air flow. The input was set to 70V, and the output was loaded with 5A. The output inductor (L1) was the hottest component on the board and measured 86.3ºC.



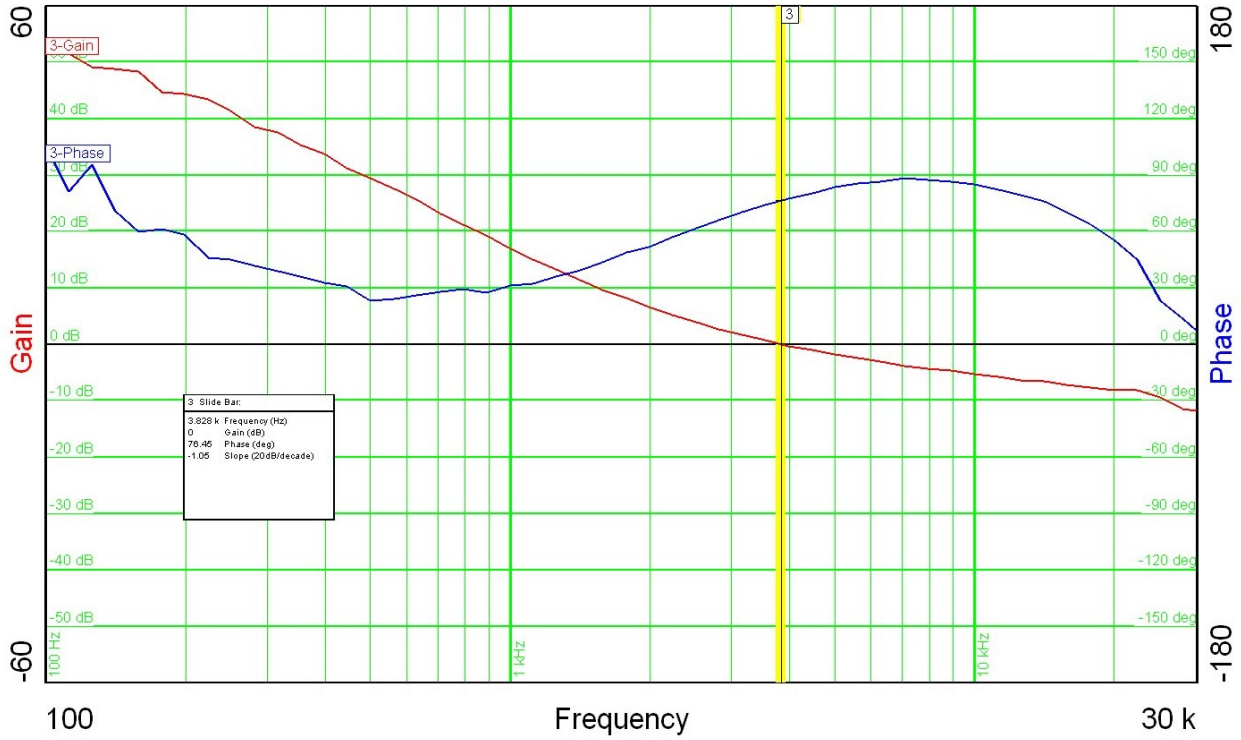
5 Output Ripple Voltage

The output ripple voltage is shown in the plot below. The input was set to 70VDC and the output was loaded with 5A.



6 Frequency Response

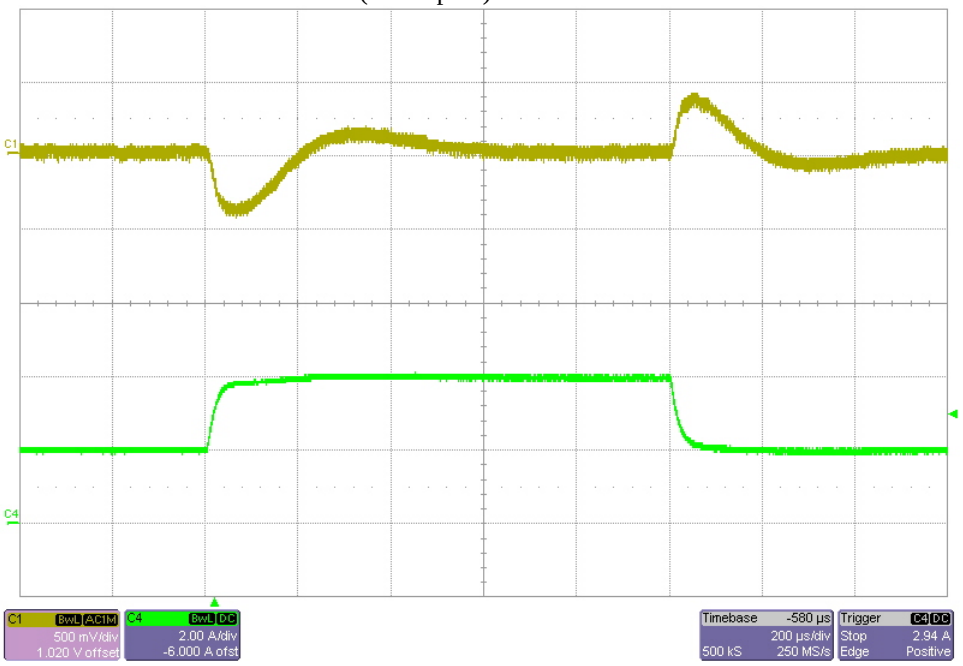
The frequency response of the feedback loop is shown below. The input was set to 70V and the output was loaded with 5A.



7 Load Transients

The response to a load step from 2A to 4A is shown in the image below. The input was set to 70V.

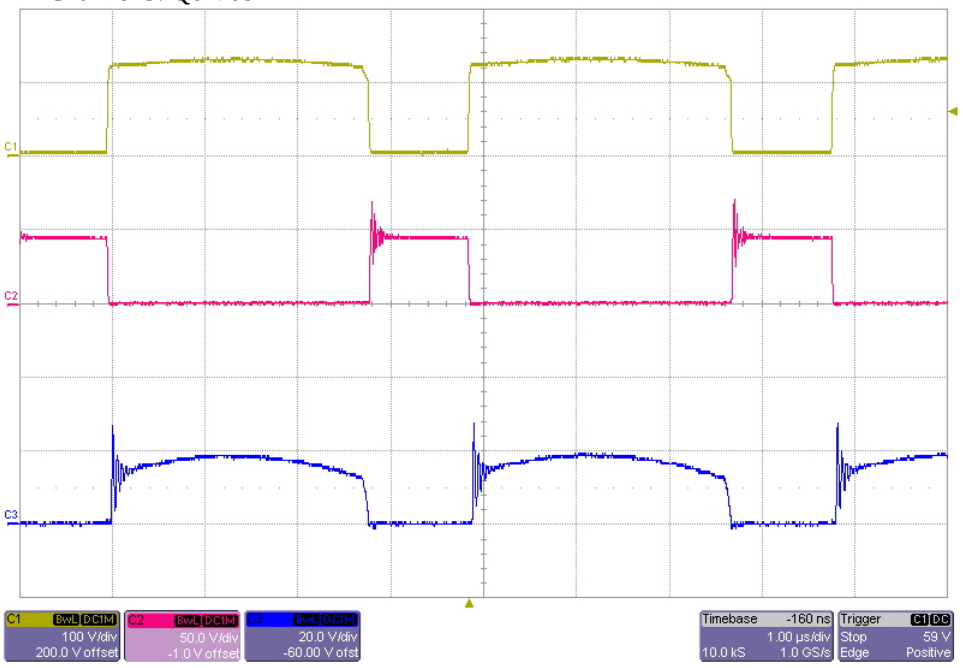
Channel 1: Vout 500mV/div (ac coupled) Channel 4: Iout 2A/div

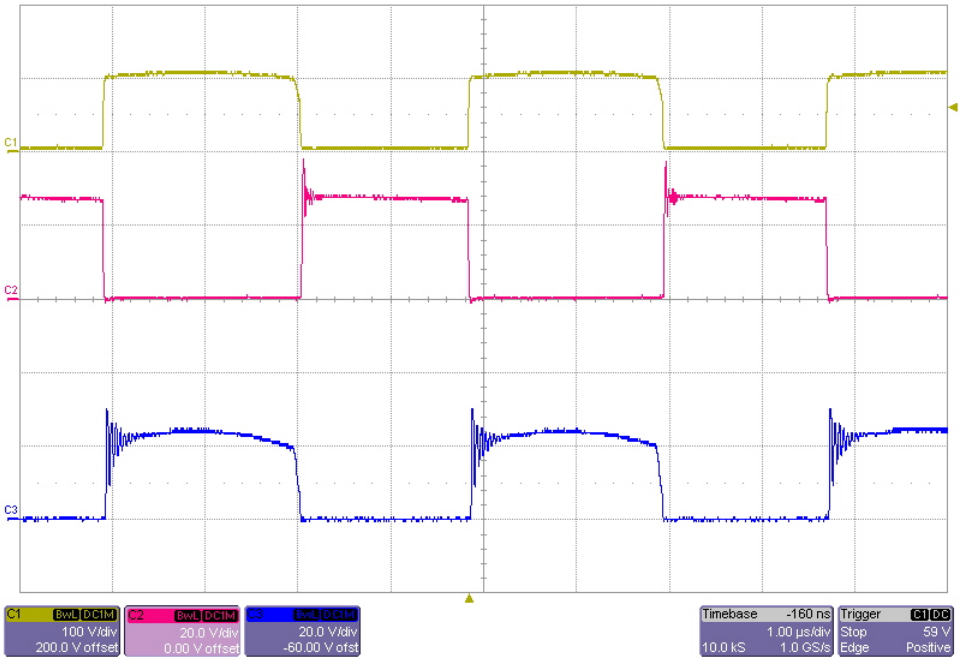


8 Switching Waveforms

The images below show the drain-to-source voltage waveforms on the switching MOSFETs. For the top image, the input was set to 90VDC. For the bottom image, the input was set to 55VDC. The output was loaded with 5A for both images.

Channel 1: Q5 Vds Channel 2: Q2 Vds
Channel 3: Q6 Vds




C1
C2
C3
C1 BwL DC1M
100 V/div
200.0 V offset
C2 BwL DC1M
20.0 V/div
0.00 V offset
C3 BwL DC1M
20.0 V/div
-60.00 V ofst
Timebase -160 ns
1.00 µs/div
10.0 kS 1.0 GS/s
Trigger C1 DC
Stop 59 V
Edge Positive

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