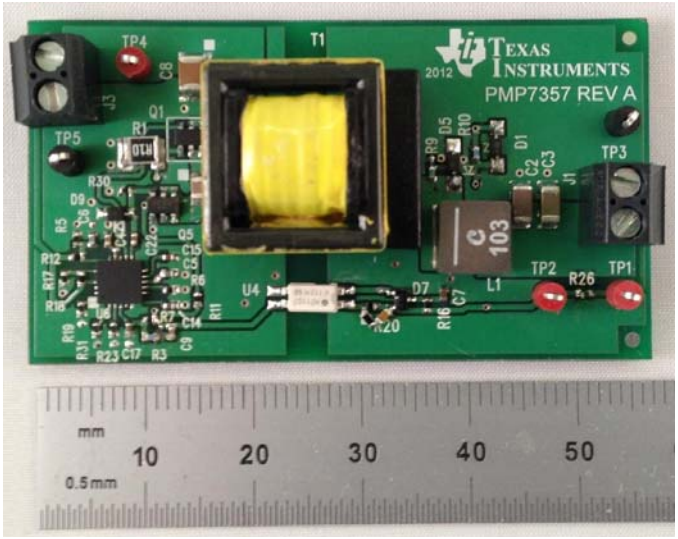
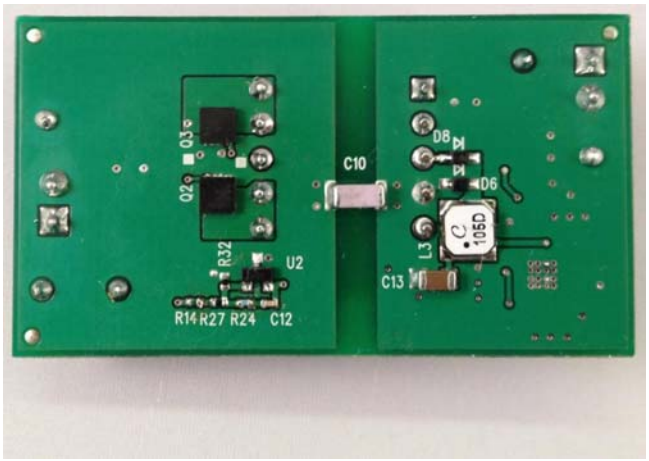
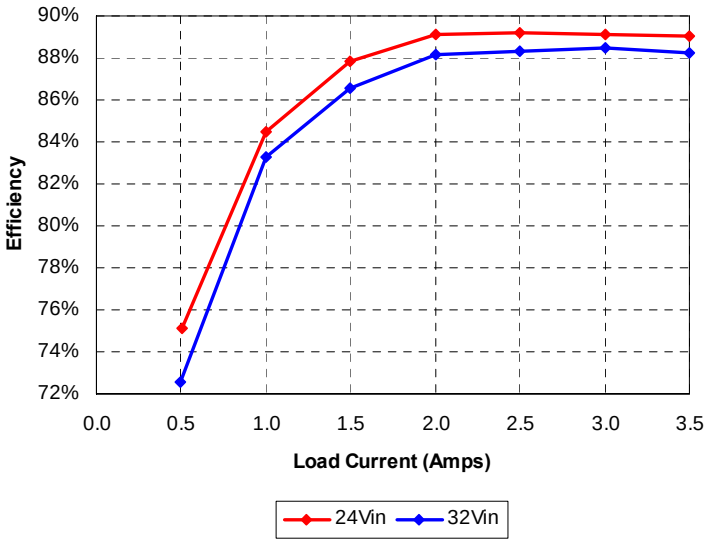
1 Photo

The photographs below show the top and bottom views of the PMP7357 Rev B demo board. The circuit is built on a PMP7357 Rev A PWB.





2 Efficiency



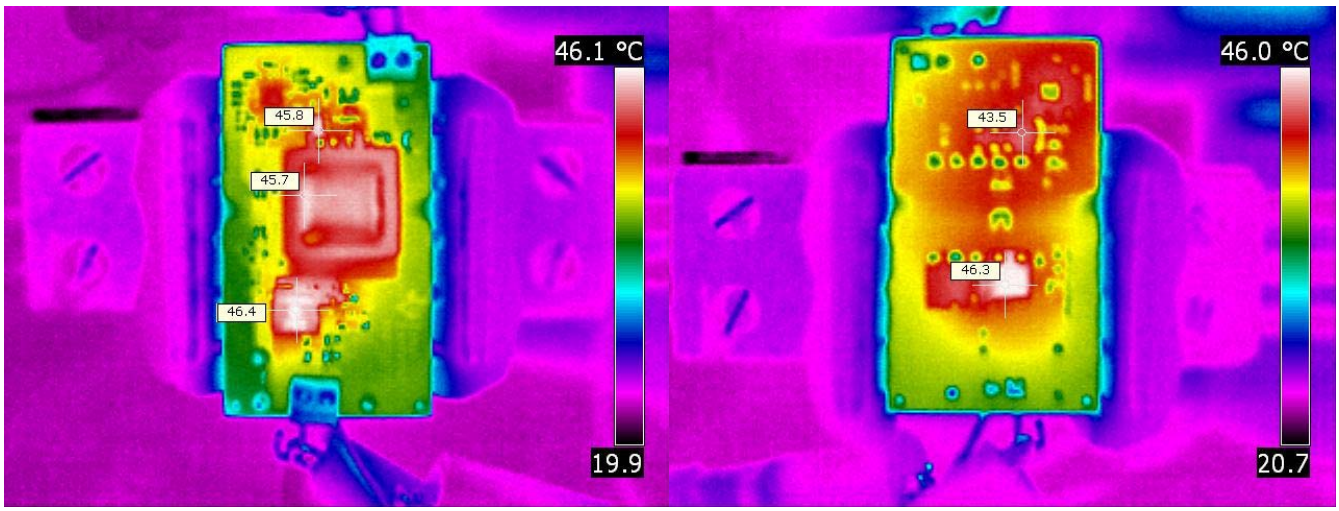
Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	3.303	32.0	0.019	0.00	0.608	0.0%
0.499	3.303	32.0	0.071	1.65	0.624	72.5%
1.001	3.302	32.0	0.124	3.31	0.663	83.3%
1.502	3.302	32.0	0.179	4.96	0.768	86.6%
2.000	3.302	32.0	0.234	6.60	0.884	88.2%
2.500	3.302	32.0	0.292	8.26	1.089	88.3%
3.002	3.302	32.0	0.350	9.91	1.287	88.5%
3.500	3.301	32.0	0.409	11.55	1.535	88.3%

Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	3.303	24.0	0.022	0.00	0.528	0.0%
0.502	3.303	24.0	0.092	1.66	0.550	75.1%
1.001	3.303	24.0	0.163	3.31	0.606	84.5%
1.501	3.302	24.0	0.235	4.96	0.684	87.9%
2.002	3.302	24.0	0.309	6.61	0.805	89.1%
2.502	3.302	24.0	0.386	8.26	1.002	89.2%
3.000	3.302	24.0	0.463	9.91	1.206	89.1%
3.501	3.302	24.0	0.541	11.56	1.424	89.0%

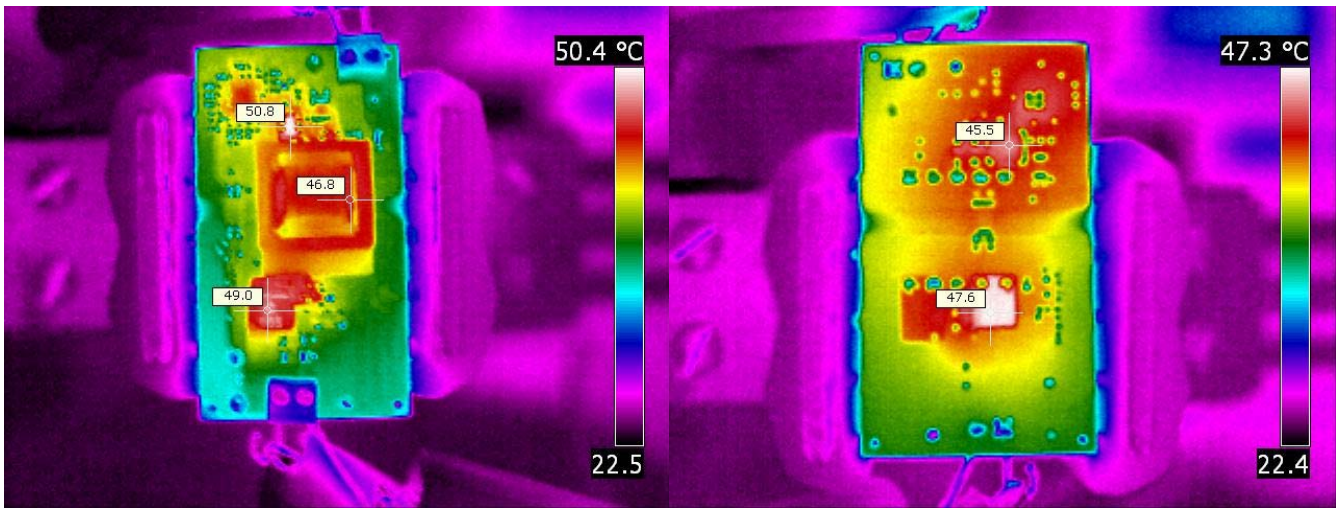
3 Thermal Images

The thermal images below show a top view (left) and bottom view (right) of the board. The ambient temperature was 25C with no forced air flow. The output was loaded with 3.5A.

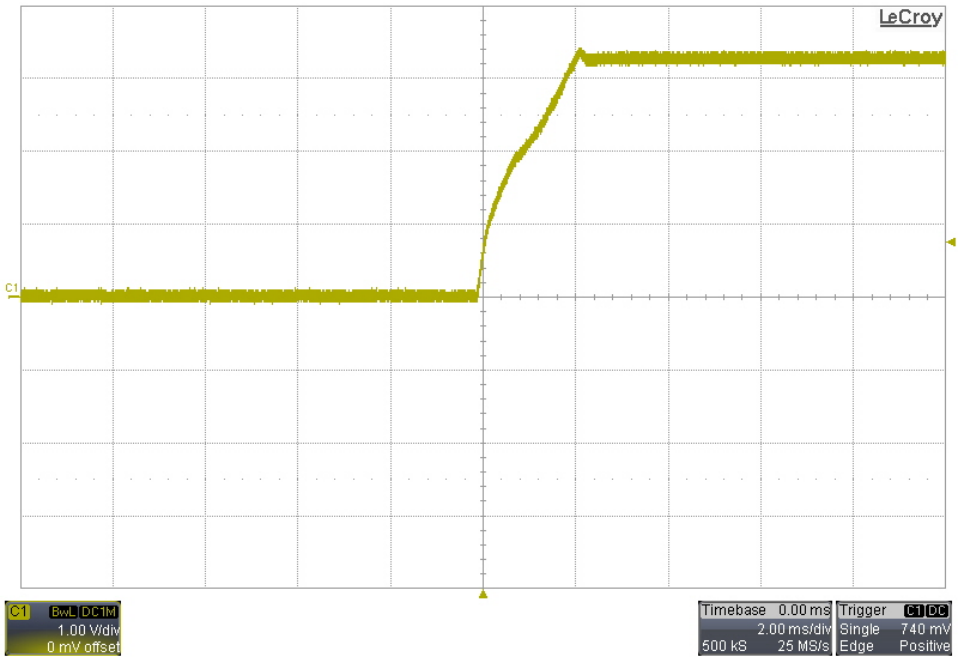
3.1 24V Input



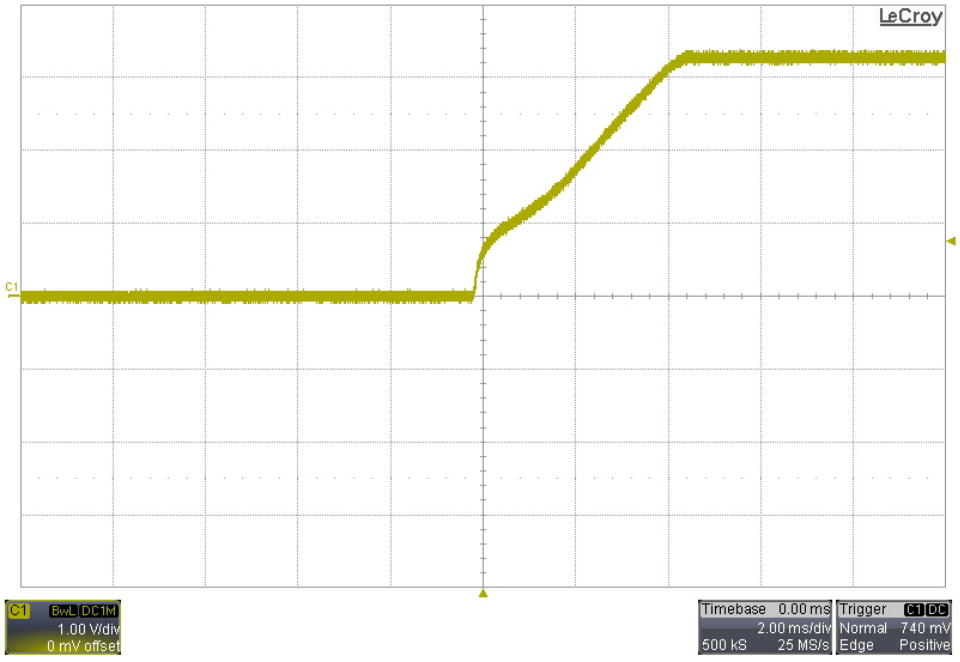
3.2 32V Input



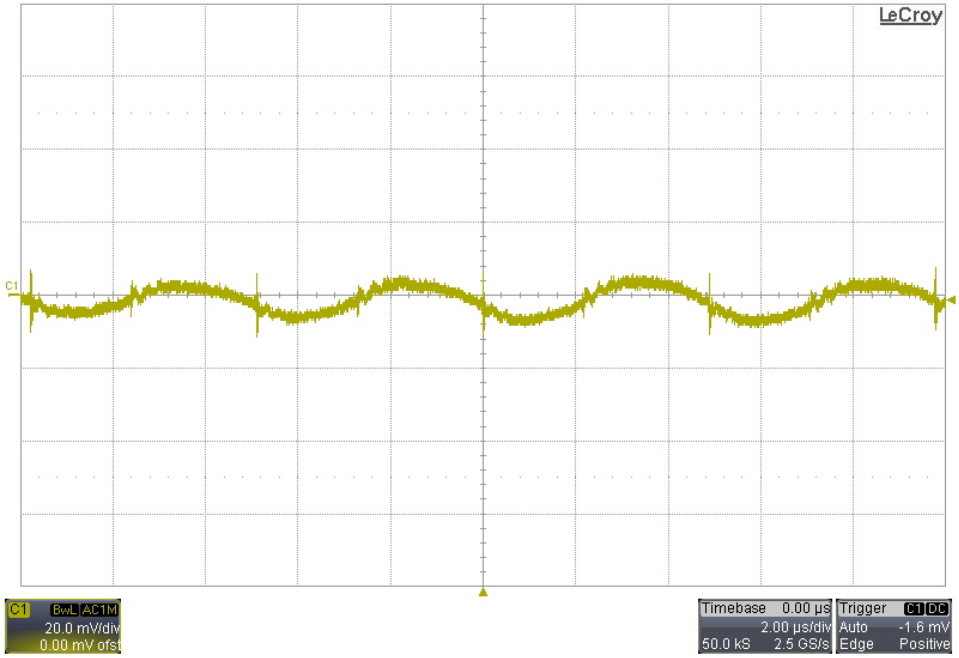
4 Startup – 32V Input – 0A Load



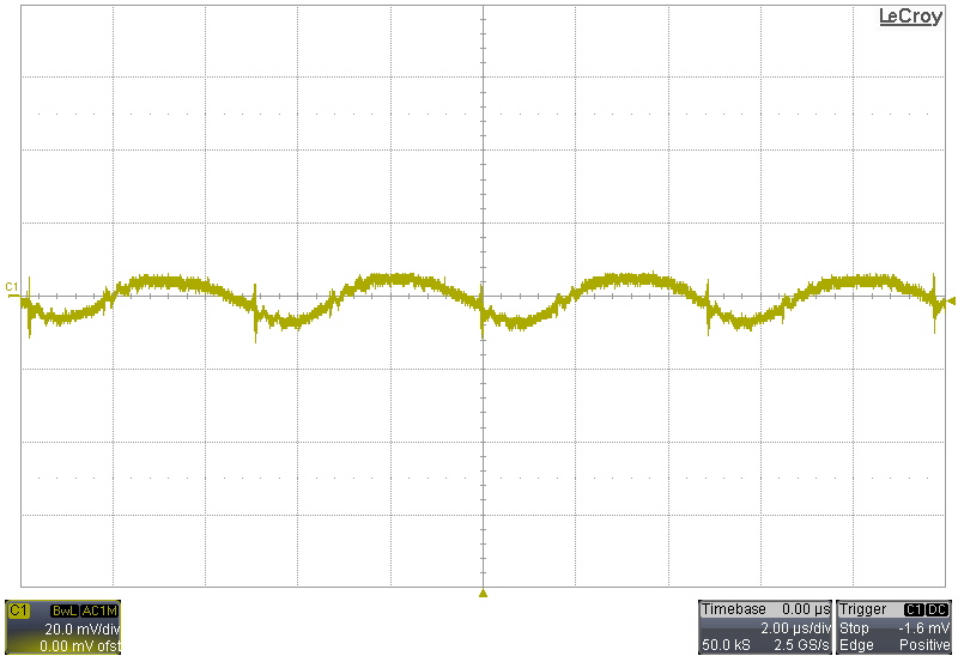
5 Startup – 32V Input - 1Ω Load



6 Output Ripple Voltage – 24V Input – 3.5A Load



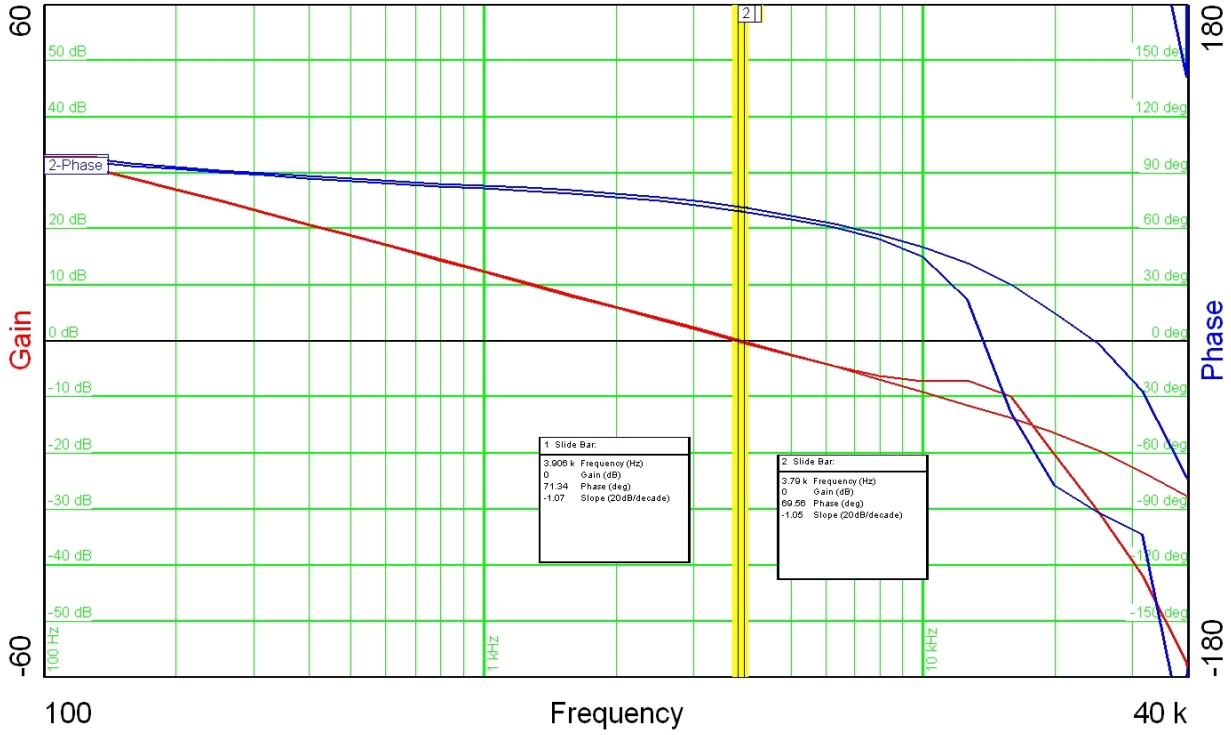
7 Output Ripple Voltage – 32V Input – 3.5A Load



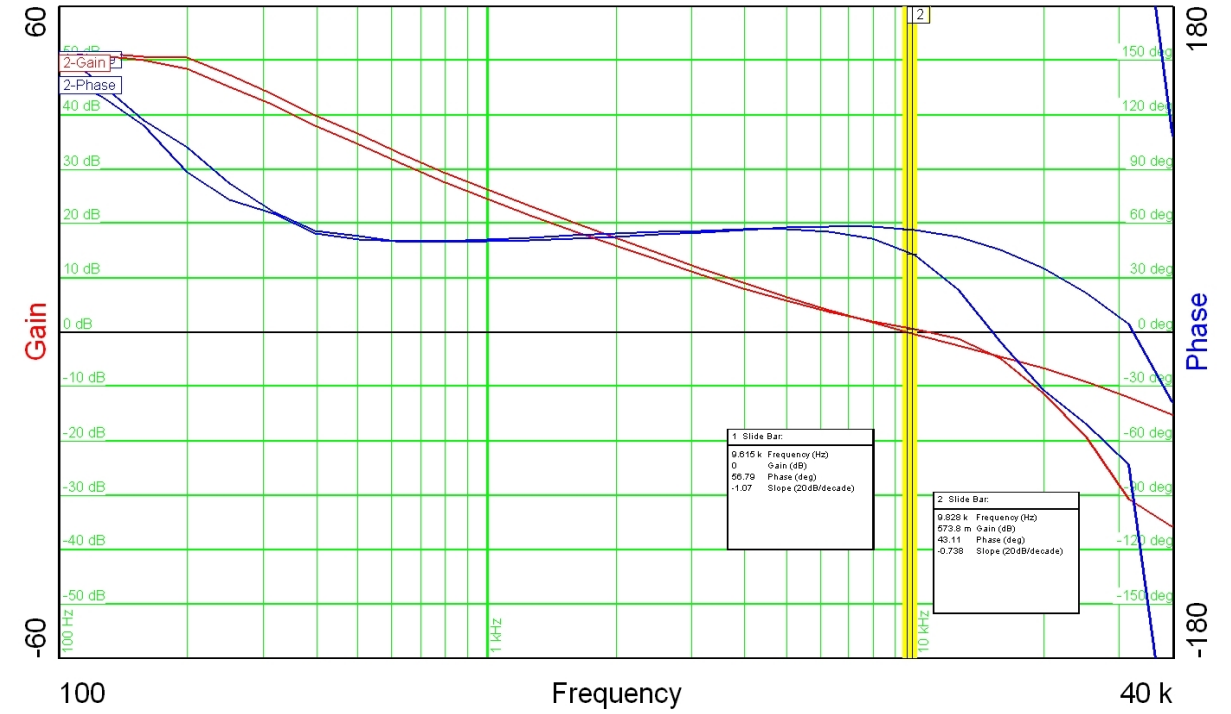
8 Frequency Response

For the gain/phase plot #1, the input was set to 32V. For the gain/phase plot #2, the input was set to 17V. The output was loaded with 3.5A.

8.1 Loop Broken At R14



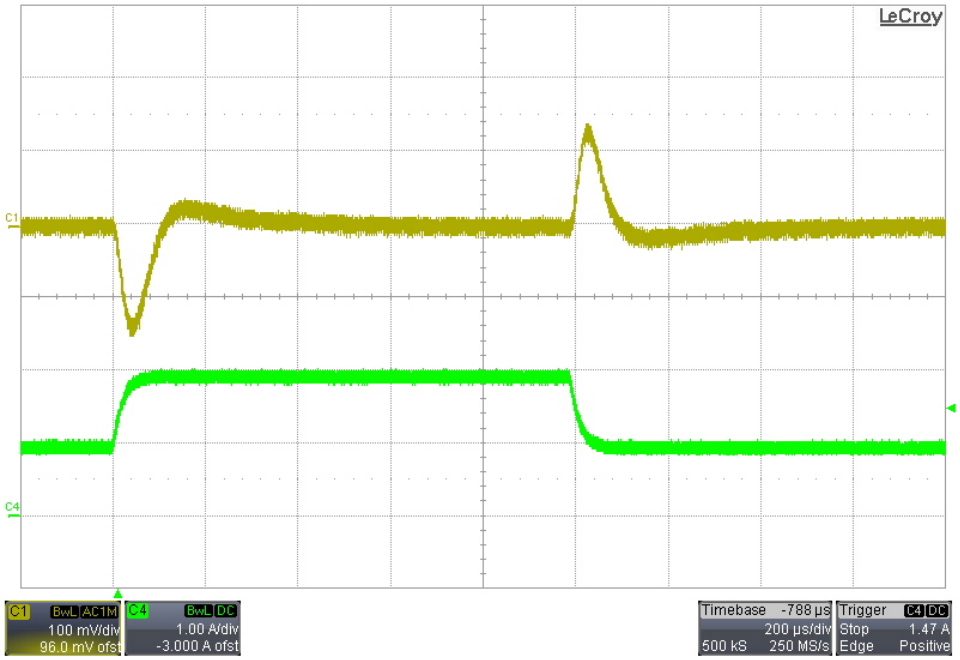
8.2 Loop Broken At R26



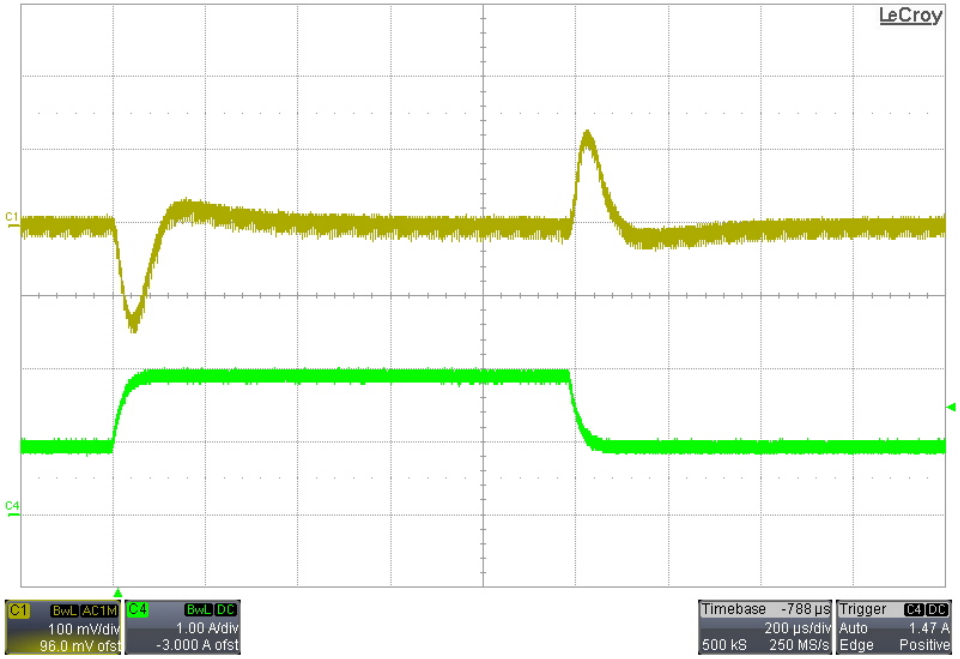
9 Load Transients

The response to a load step from 1A to 2A is shown in the images below. Channel 1: Vout (ac coupled); Channel 4: Iout

9.1 24V Input



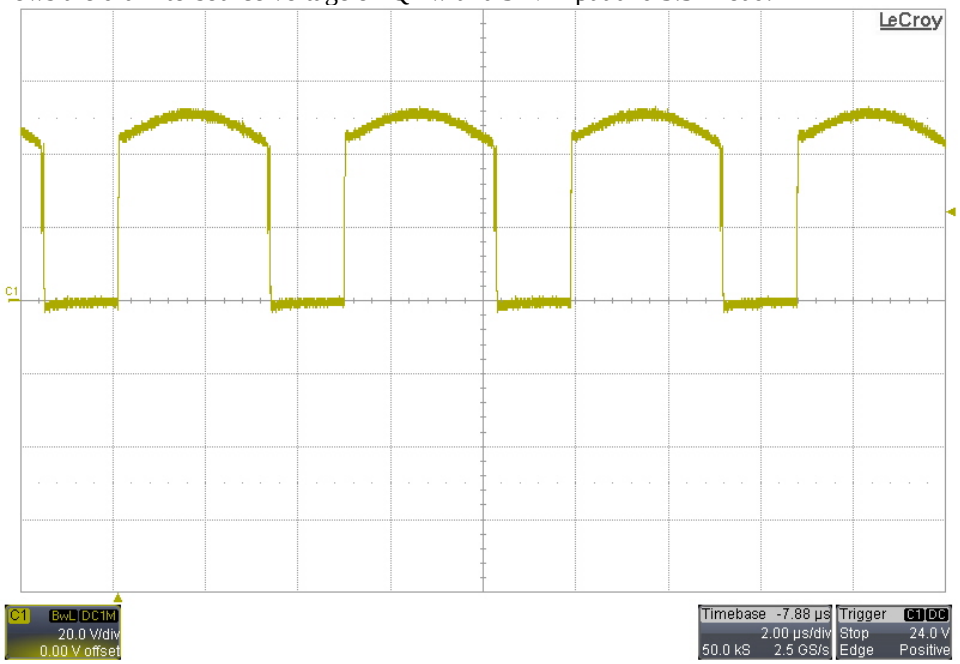
9.2 32V Input



10 Switching Waveforms

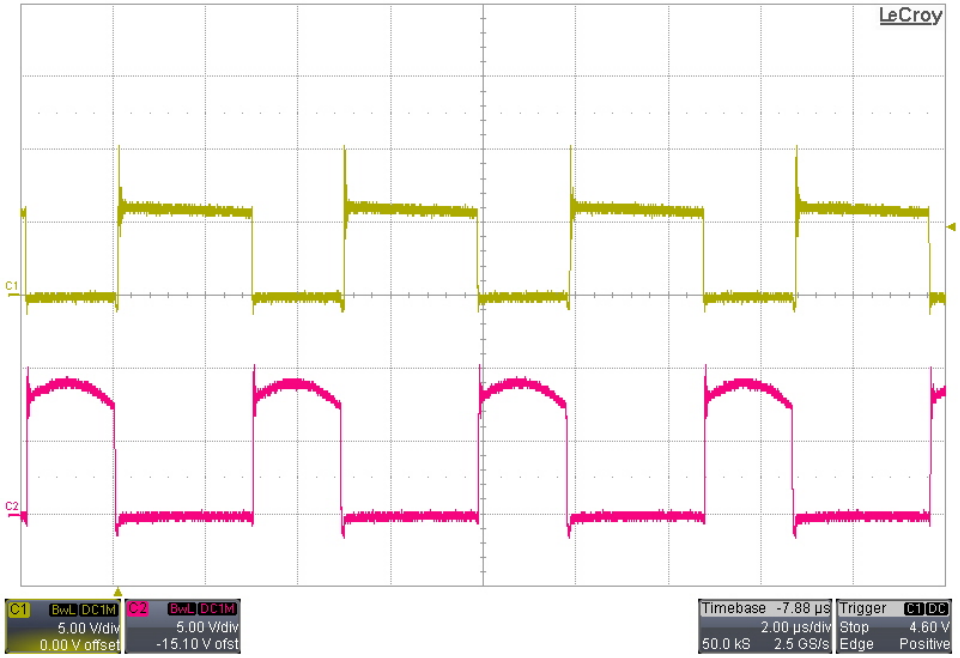
10.1 Primary FET

The image below shows the drain-to-source voltage on Q1 with a 32V input and 3.5A load.



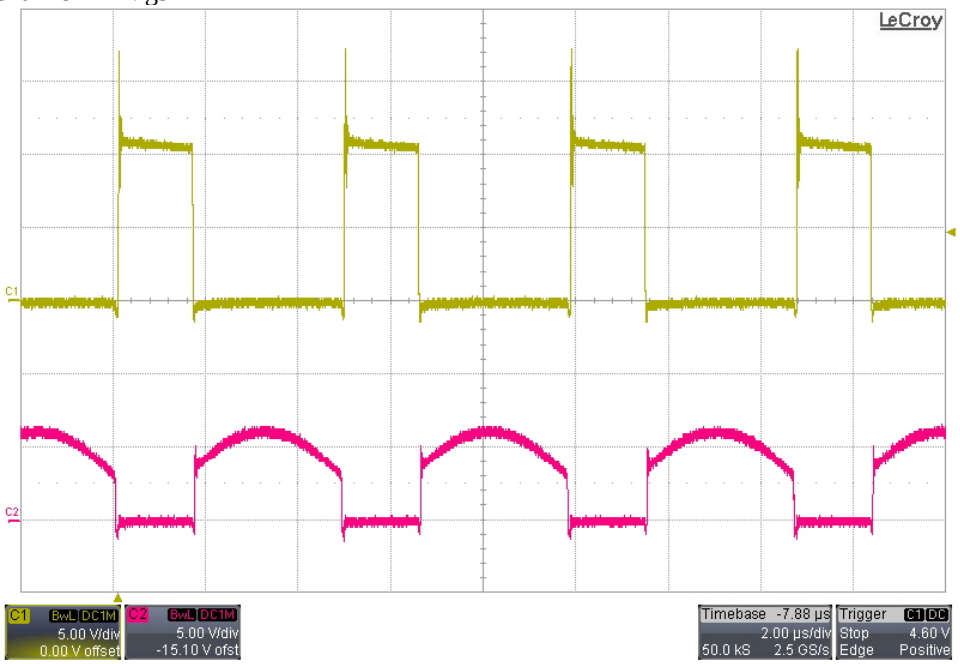
10.2 Q2 Synchronous FET – 17V Input – 3.5A Load

Channel 1 – Vds; Channel 2 - Vgs



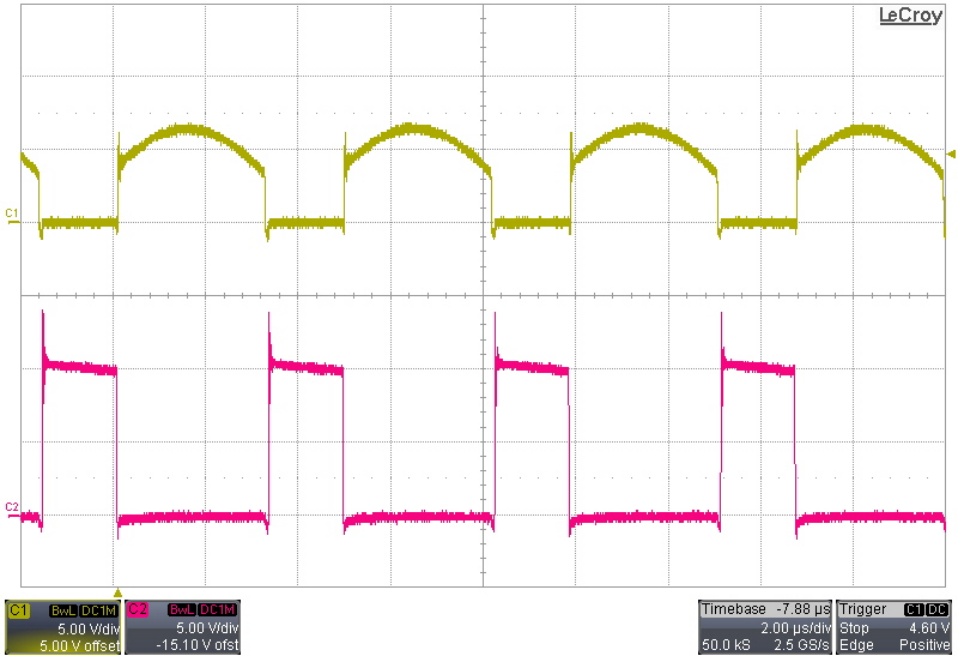
10.3 Q2 Synchronous FET – 32V Input – 3.5A Load

Channel 1 – Vds; Channel 2 – Vgs



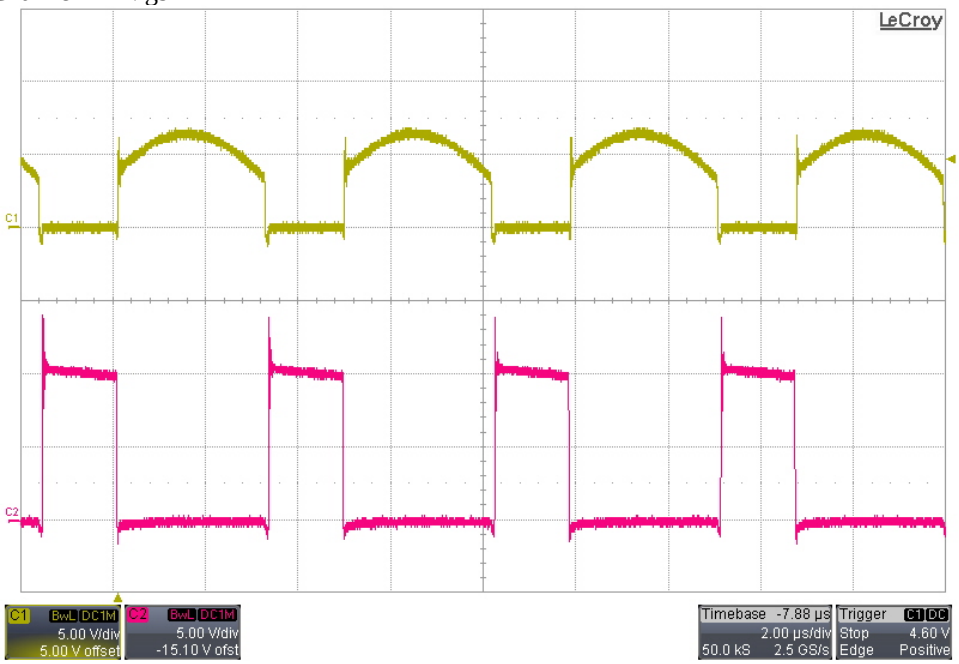
10.4 Q3 Synchronous FET – 17V Input – 3.5A Load

Channel 1 – Vds; Channel 2 – Vgs



10.5 Q3 Synchronous FET – 32V Input – 3.5A Load

Channel 1 – Vds; Channel 2 – Vgs



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