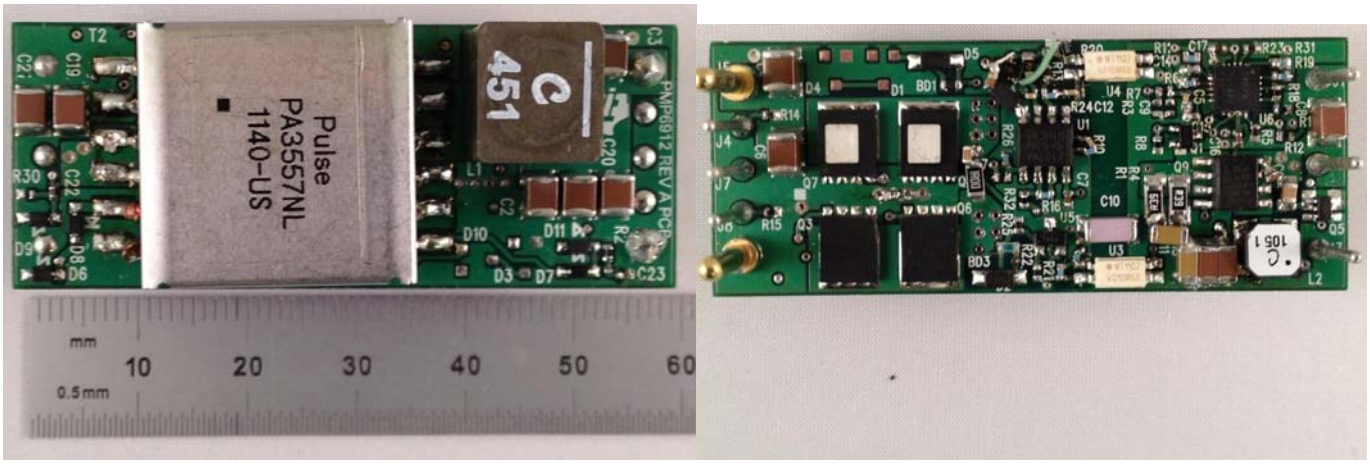
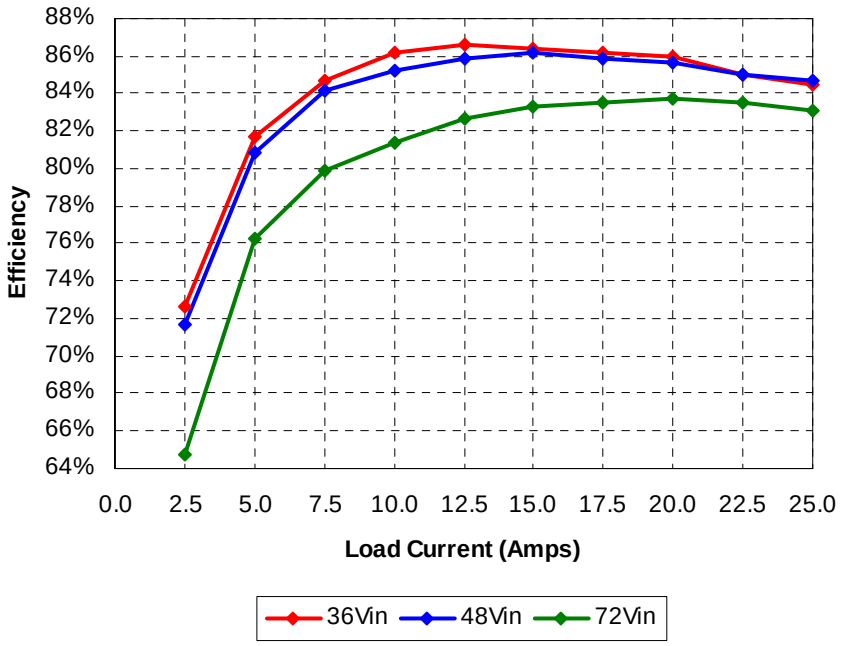
1 Photo

The photographs below show the top and bottom views of the PMP6912 Rev B demo board. The circuit is built on a PMP6912 Rev A PWB.



2 Efficiency



PMP6912 Rev B Test Results

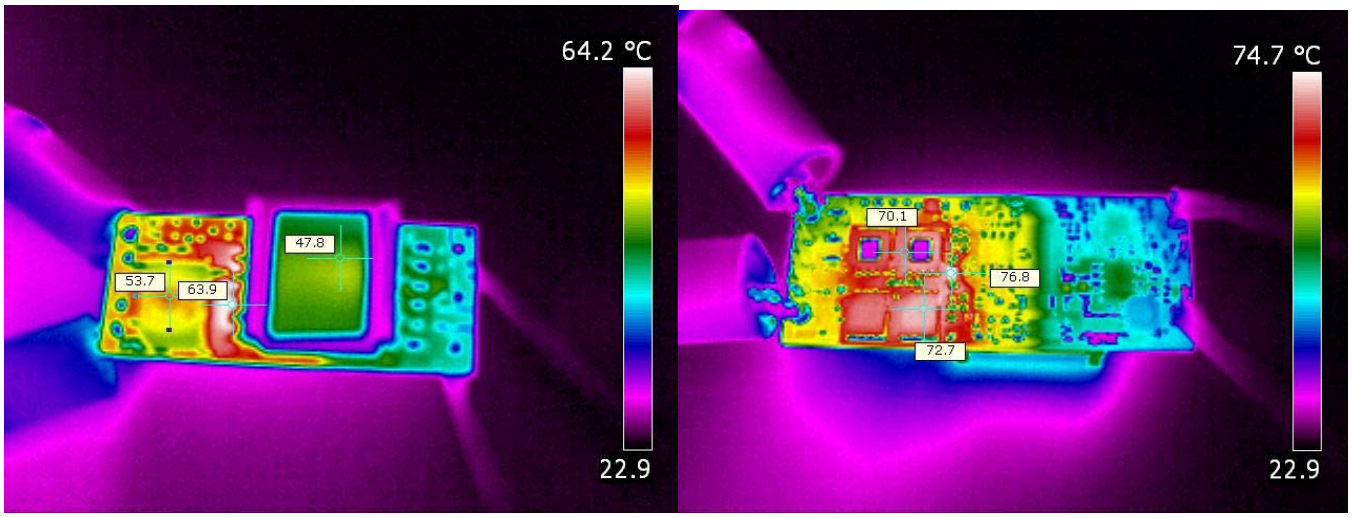
Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	1.194	36.0	0.028	0.00	1.008	0.0%
2.497	1.194	36.0	0.114	2.98	1.123	72.6%
5.002	1.194	36.0	0.203	5.97	1.336	81.7%
7.50	1.195	36.0	0.294	8.96	1.622	84.7%
10.00	1.195	36.0	0.385	11.95	1.910	86.2%
12.50	1.195	36.0	0.479	14.94	2.307	86.6%
15.00	1.195	36.0	0.576	17.93	2.811	86.4%
17.50	1.195	36.0	0.674	20.91	3.352	86.2%
20.0	1.194	36.0	0.772	23.88	3.912	85.9%
22.5	1.194	36.0	0.878	26.87	4.743	85.0%
25.0	1.194	36.0	0.981	29.85	5.466	84.5%

Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	1.196	48.0	0.022	0.00	1.056	0.0%
2.504	1.195	48.0	0.087	2.99	1.184	71.7%
4.999	1.195	48.0	0.154	5.97	1.418	80.8%
7.50	1.195	48.0	0.222	8.96	1.694	84.1%
10.00	1.195	48.0	0.292	11.95	2.066	85.3%
12.50	1.194	48.0	0.362	14.93	2.451	85.9%
15.00	1.194	48.0	0.433	17.91	2.874	86.2%
17.50	1.194	48.0	0.507	20.90	3.441	85.9%
20.0	1.194	48.0	0.581	23.88	4.008	85.6%
22.5	1.194	48.0	0.658	26.87	4.719	85.1%
25.0	1.195	48.0	0.735	29.88	5.405	84.7%

Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	1.196	72.0	0.020	0.00	1.440	0.0%
2.495	1.196	72.0	0.064	2.98	1.624	64.8%
5.002	1.196	72.0	0.109	5.98	1.866	76.2%
7.50	1.196	72.0	0.156	8.97	2.262	79.9%
10.00	1.195	72.0	0.204	11.95	2.738	81.4%
12.50	1.195	72.0	0.251	14.94	3.135	82.7%
15.00	1.195	72.0	0.299	17.93	3.603	83.3%
17.51	1.195	72.0	0.348	20.92	4.132	83.5%
20.0	1.194	72.0	0.396	23.88	4.632	83.8%
22.5	1.194	72.0	0.447	26.87	5.319	83.5%
25.0	1.194	72.0	0.499	29.85	6.078	83.1%

3 Thermal Images

The thermal images below show a top view (left) and bottom view (right) of the board. The ambient temperature was 25C with 100LFM of forced air flow. The input was 48VDC, and the output was loaded with 25A.

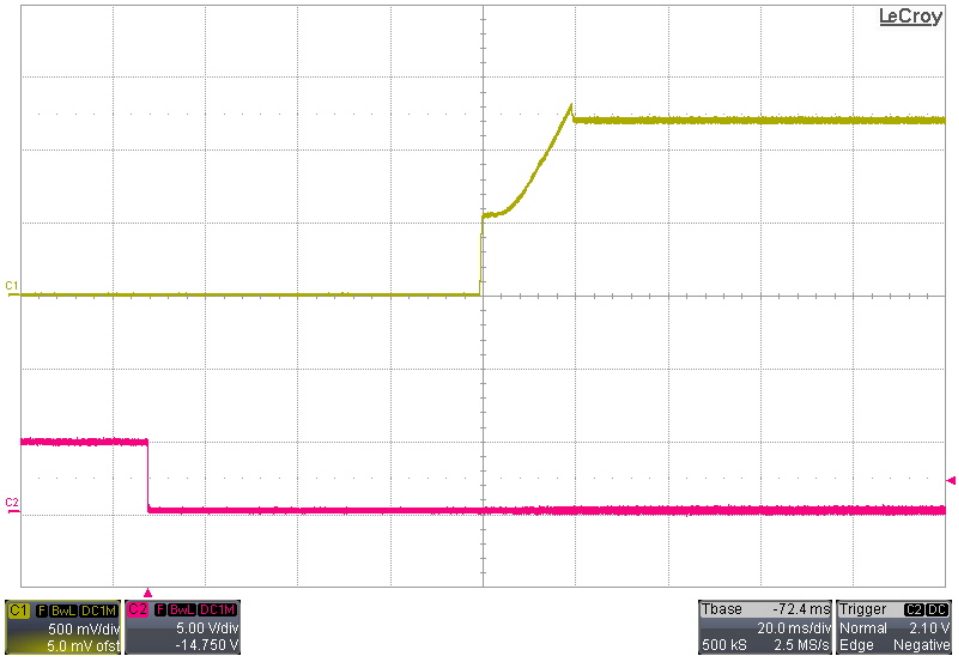


4 Startup

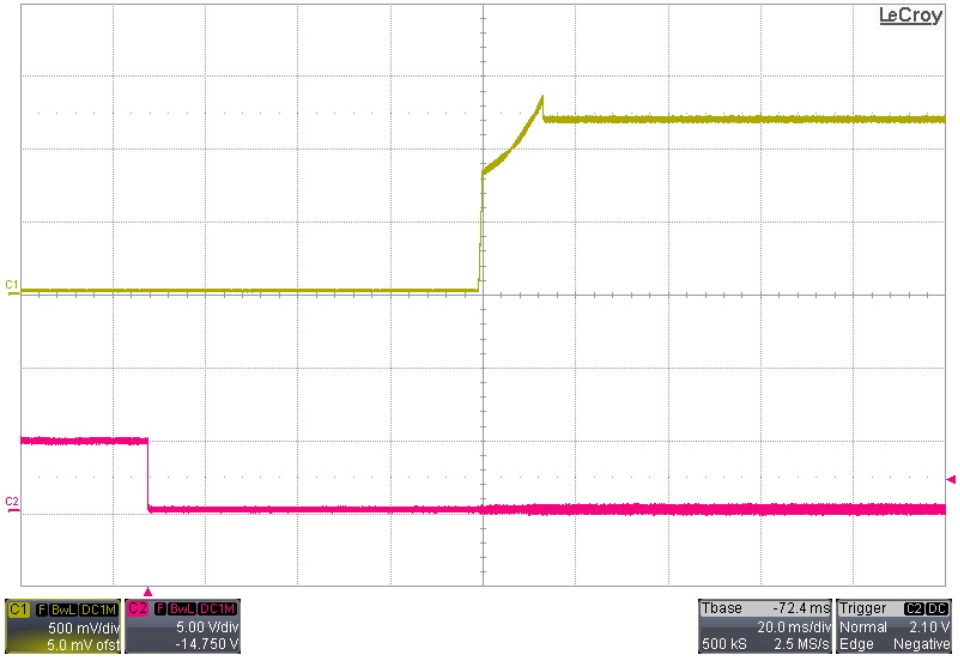
The output voltage at startup is shown in the images below. Channel 1 shows the output voltage. Channel 2 shows the enable signal voltage.

4.1 No External Capacitance

4.1.1 36V Input – No Load



4.1.2 72V Input – No Load



4.2 6800uF External Capacitance

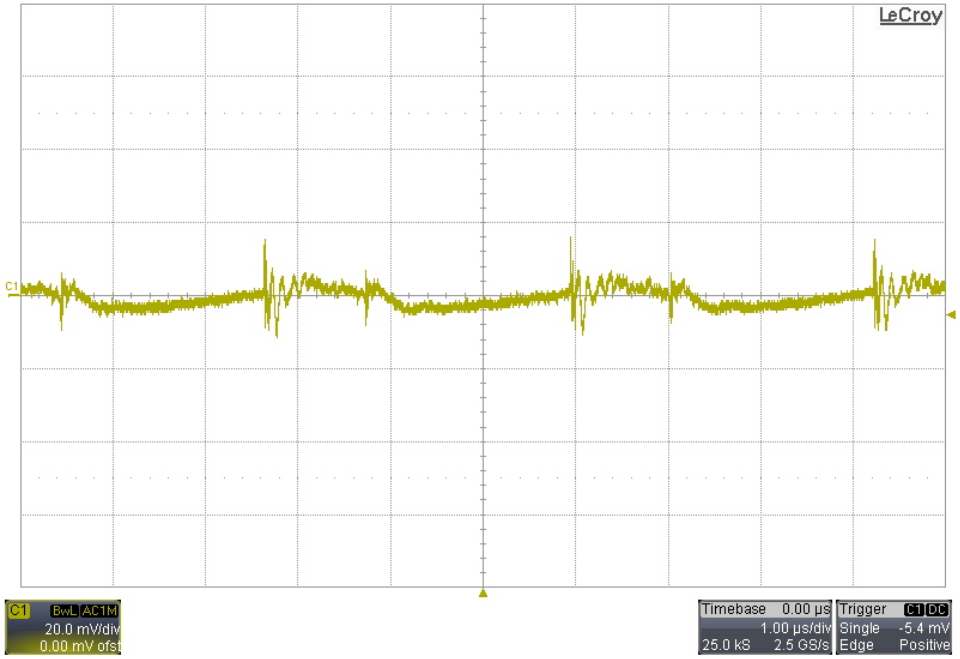
4.2.1 36V Input – No Load

4.2.2 72V Input – No Load

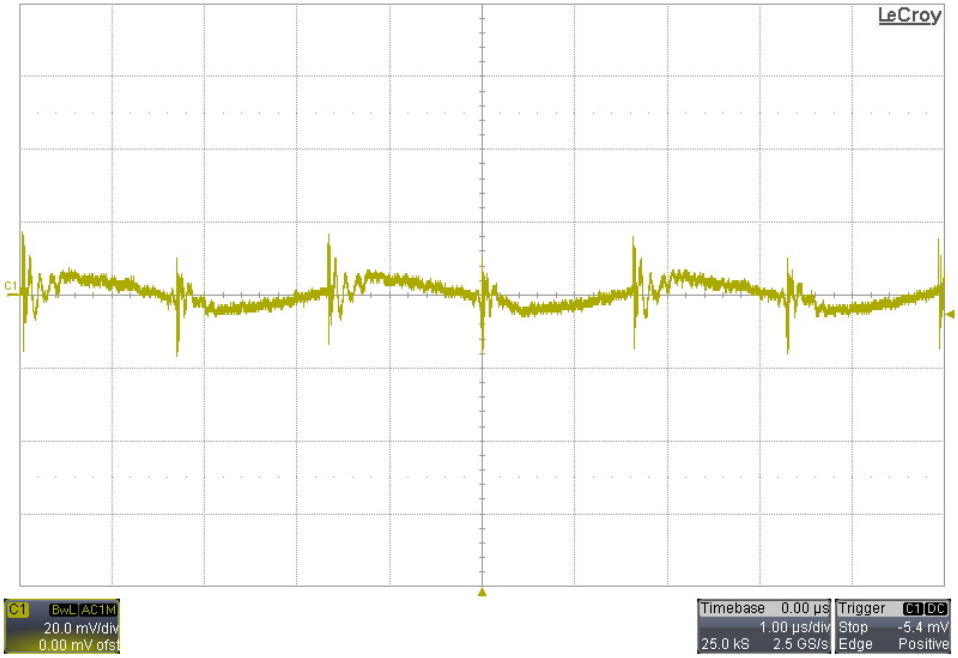
5 Output Ripple Voltage

The output ripple voltage is shown in the plots below. The output was loaded with 25A.

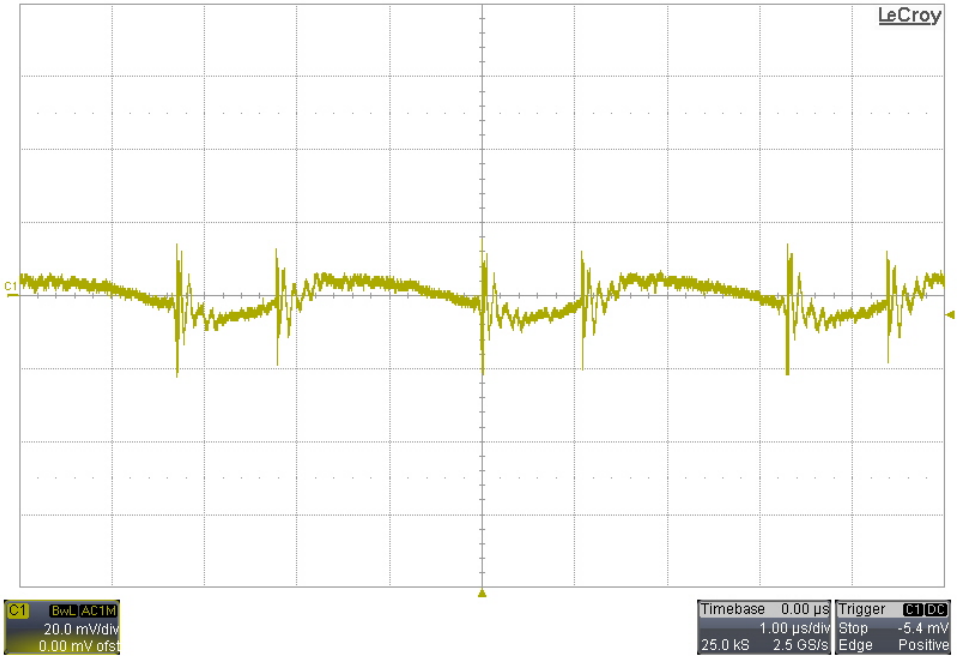
5.1 36V Input



5.2 48V Input



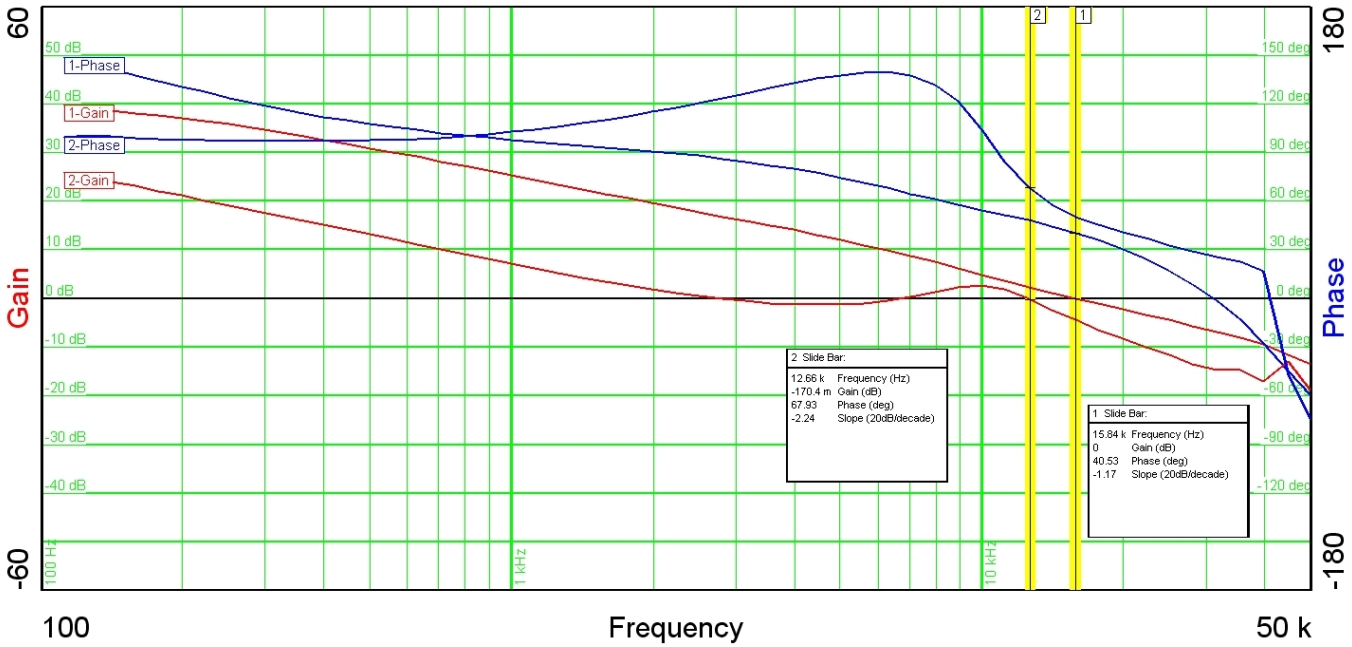
5.3 72V Input



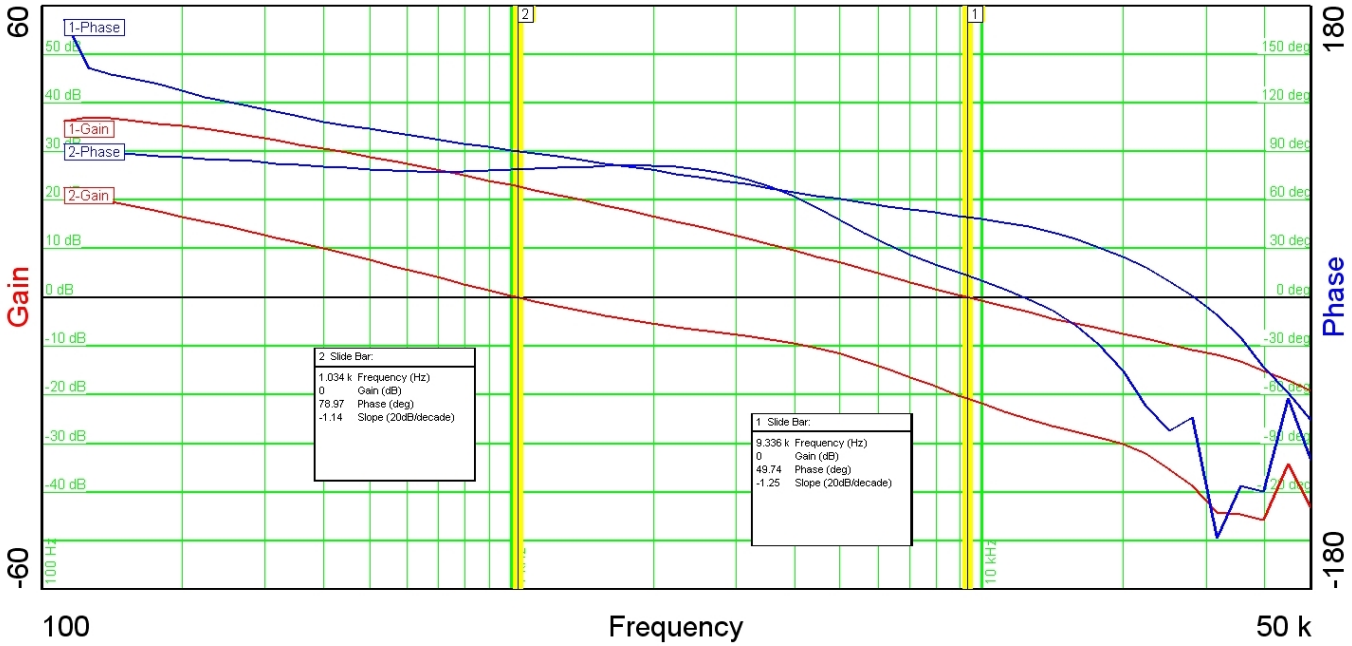
6 Frequency Response

The frequency response of the feedback loop is shown below. For the gain/phase plot #1, the input was set to 72V. For the gain/phase plot #2, the input was set to 36V.

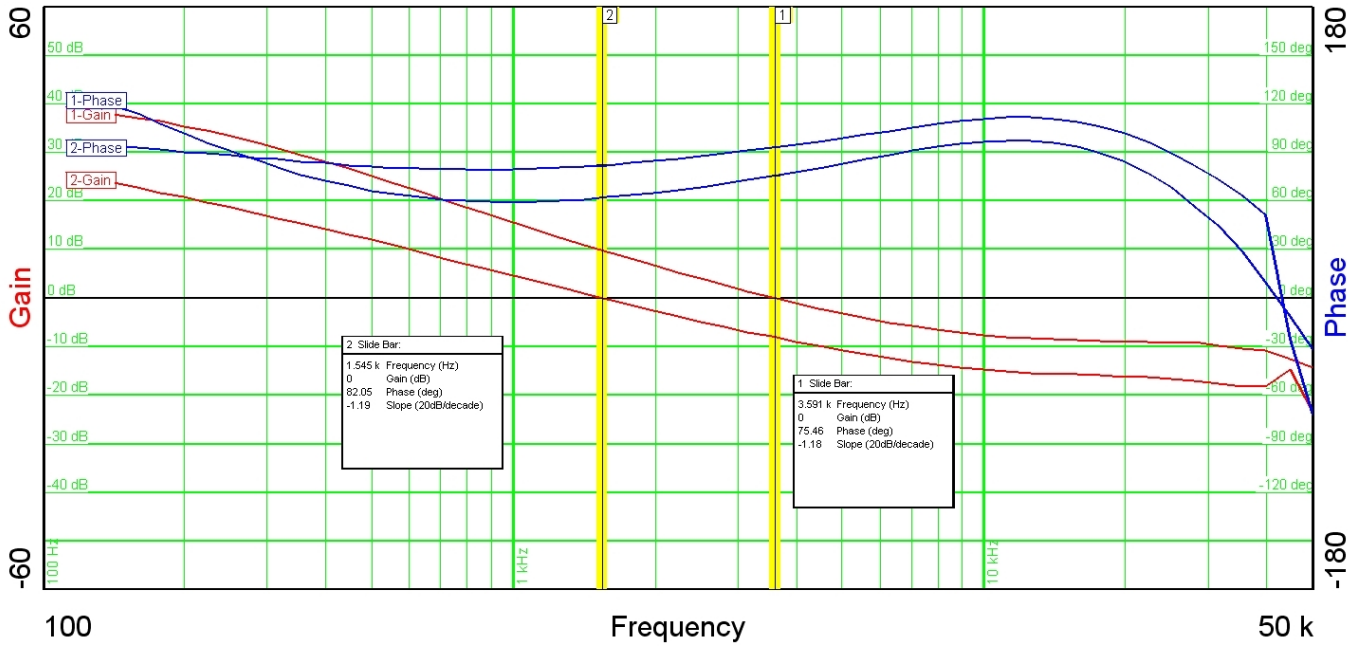
6.1 No External Capacitance, 0A Load



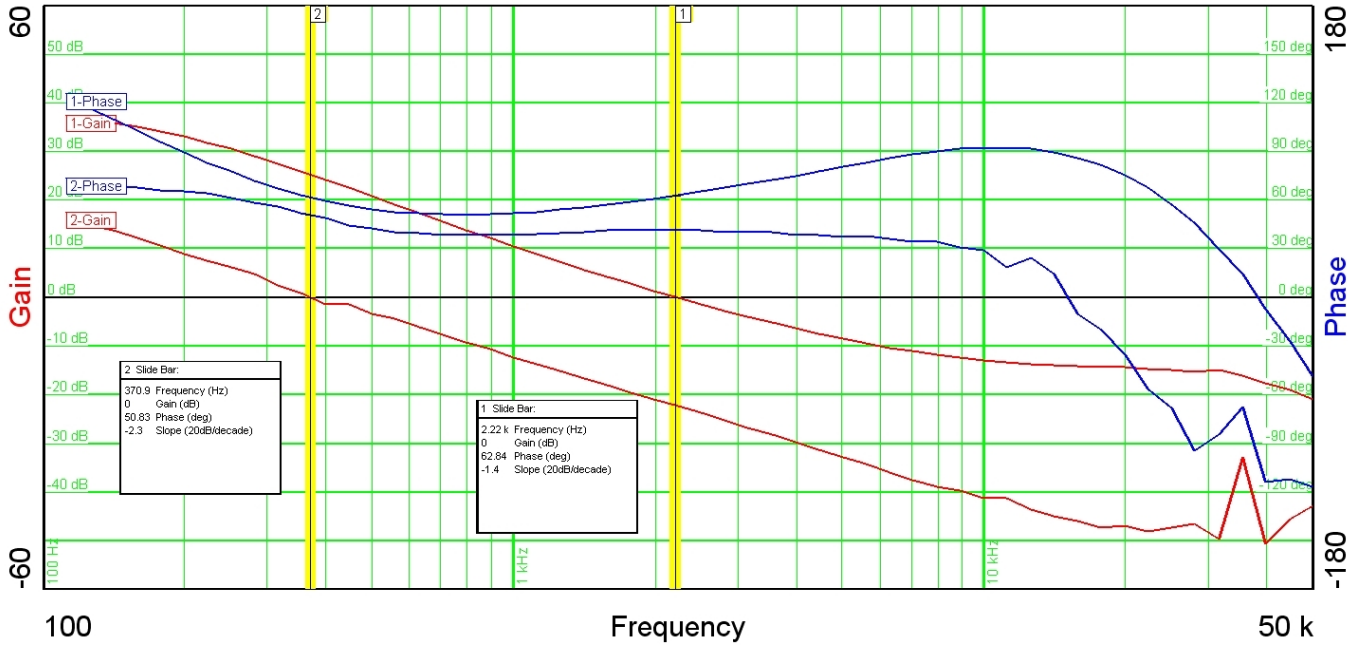
6.2 No External Capacitance, 25A Load



6.3 6800uF External Capacitance, 0A Load



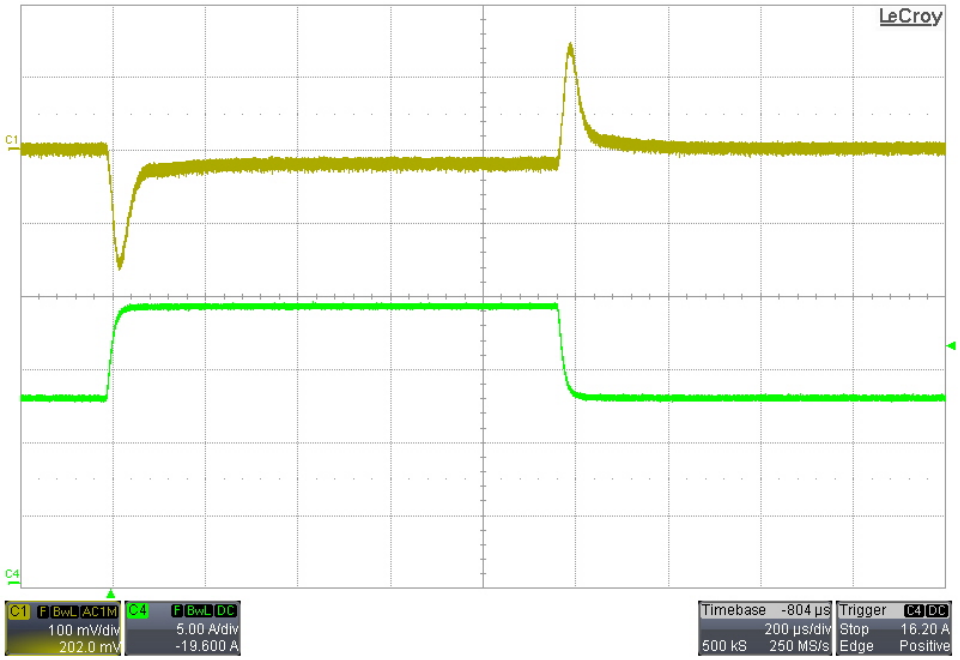
6.4 6800uF External Capacitance, 25A Load



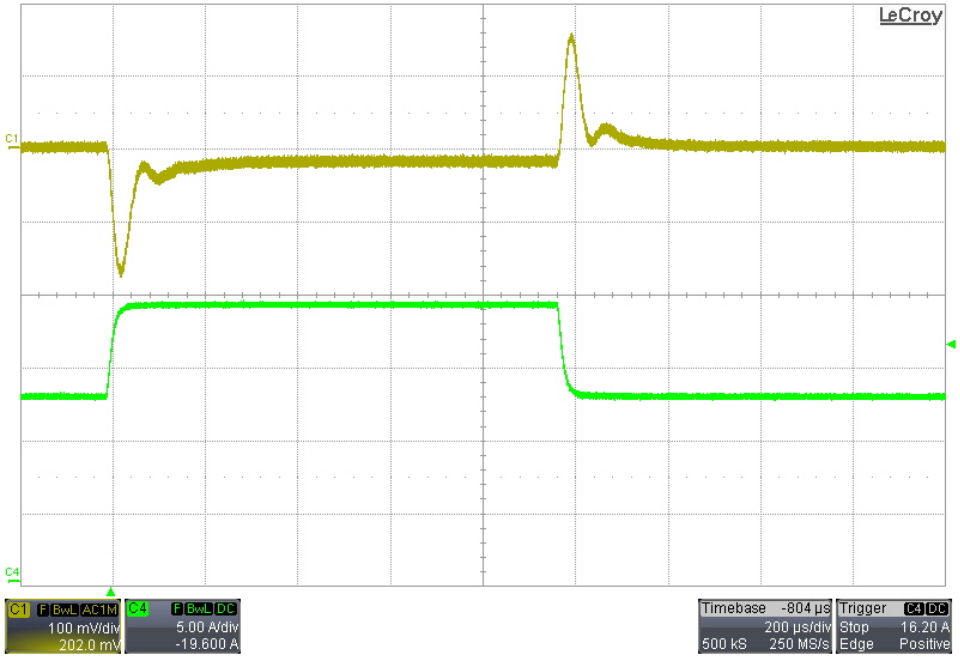
7 Load Transients

The response to a load step from 12.5A to 18.75A is shown in the images below. Channel 1: Vout (ac coupled); Channel 4: Iout

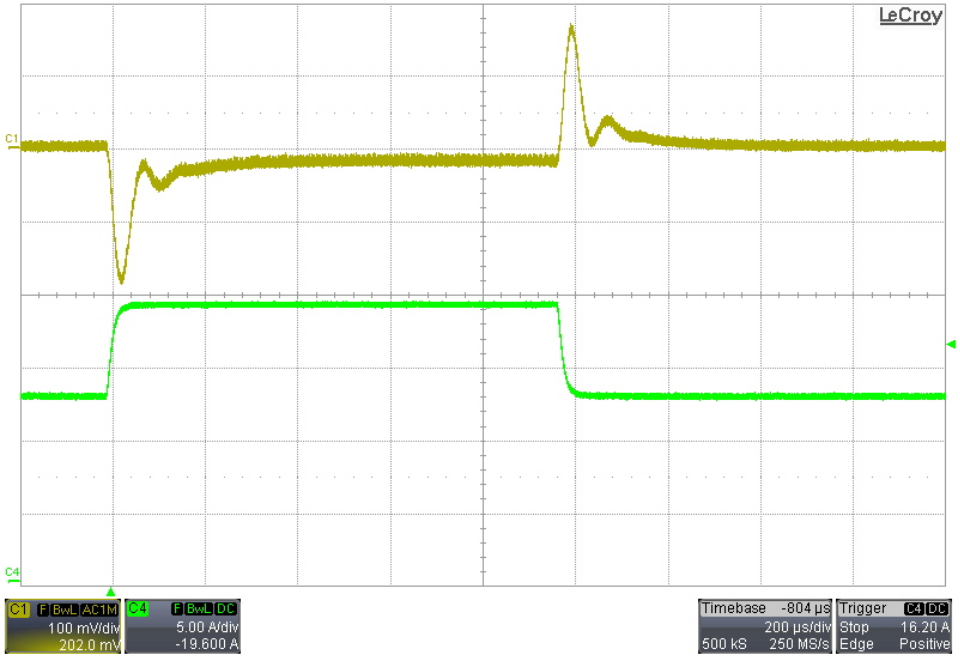
7.1 36V Input – No External Capacitance



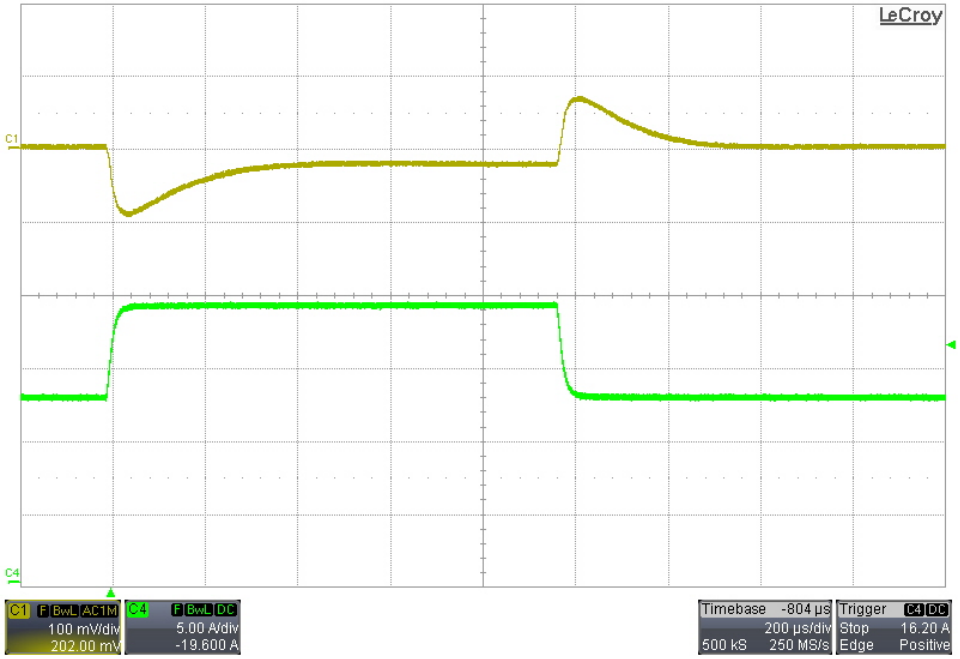
7.2 48V Input – No External Capacitance



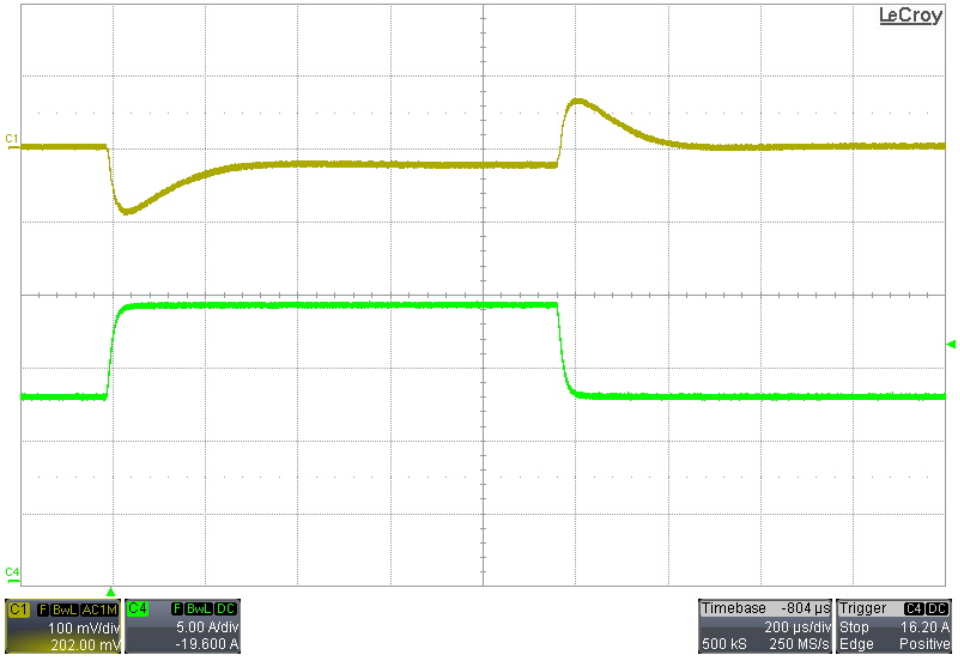
7.3 72V Input – No External Capacitance



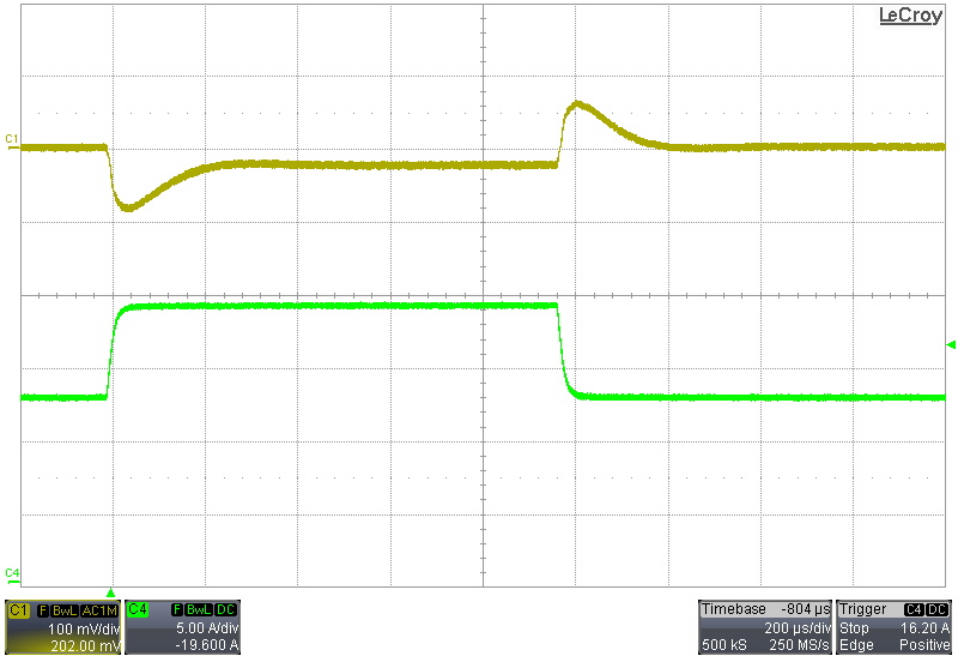
7.4 36V Input – 6800uF External Capacitance



7.5 48V Input – 6800uF External Capacitance



7.6 72V Input – 6800uF External Capacitance



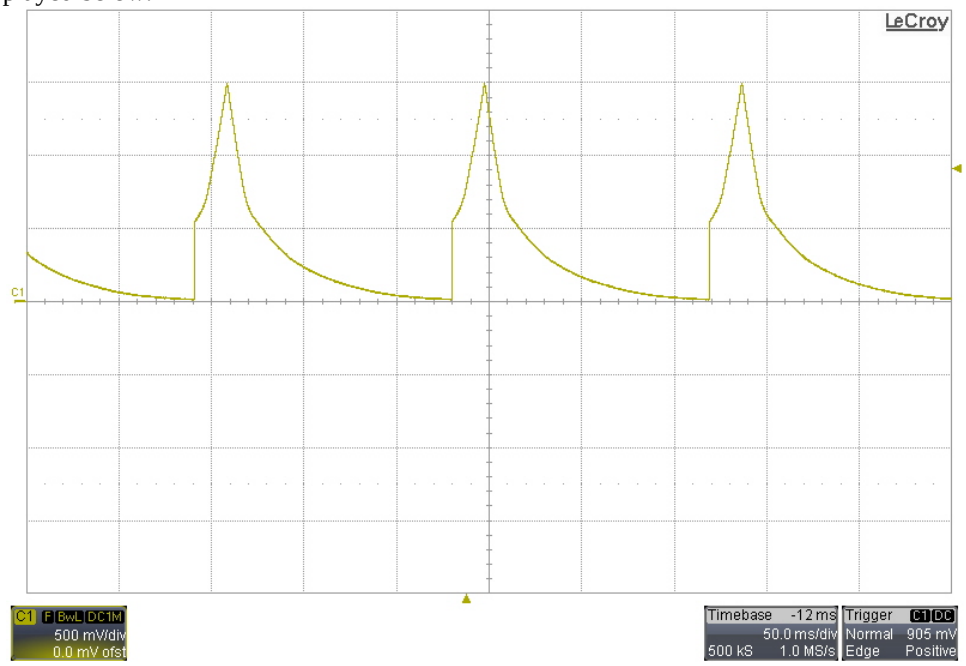
8 Input Under-Voltage Lock-Out

The turn-on and turn-off input voltages were measured and recorded below.

Turn-On	35.3 V
Turn-Off	33.5 V

9 Output Over-Voltage

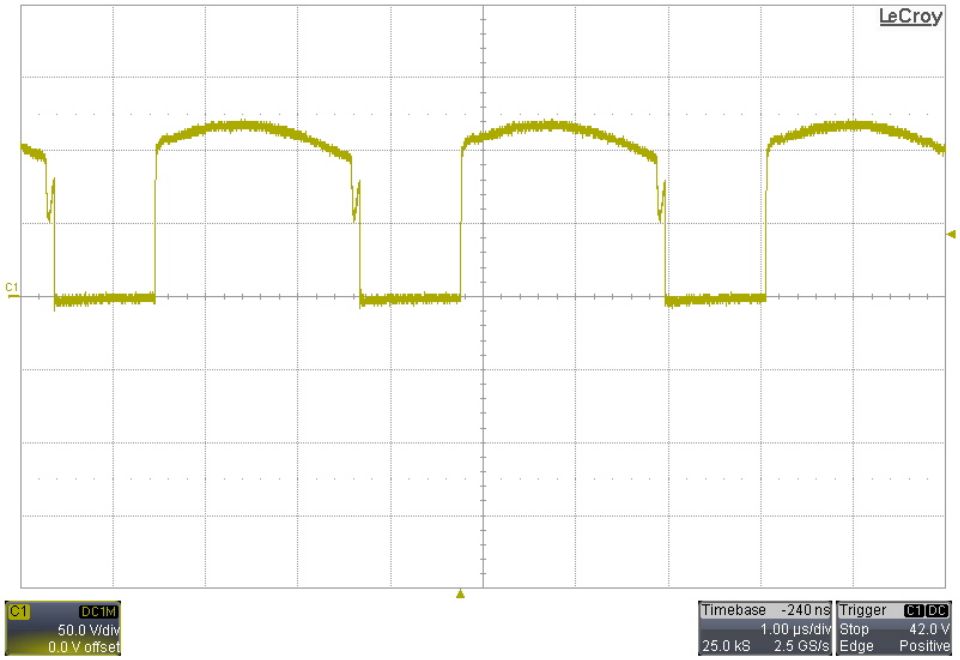
An output over-voltage was induced by shorting the +Remote Sense pin (J4) to ground. The output voltage waveform was captured and is displayed below.



10 Switching Waveforms

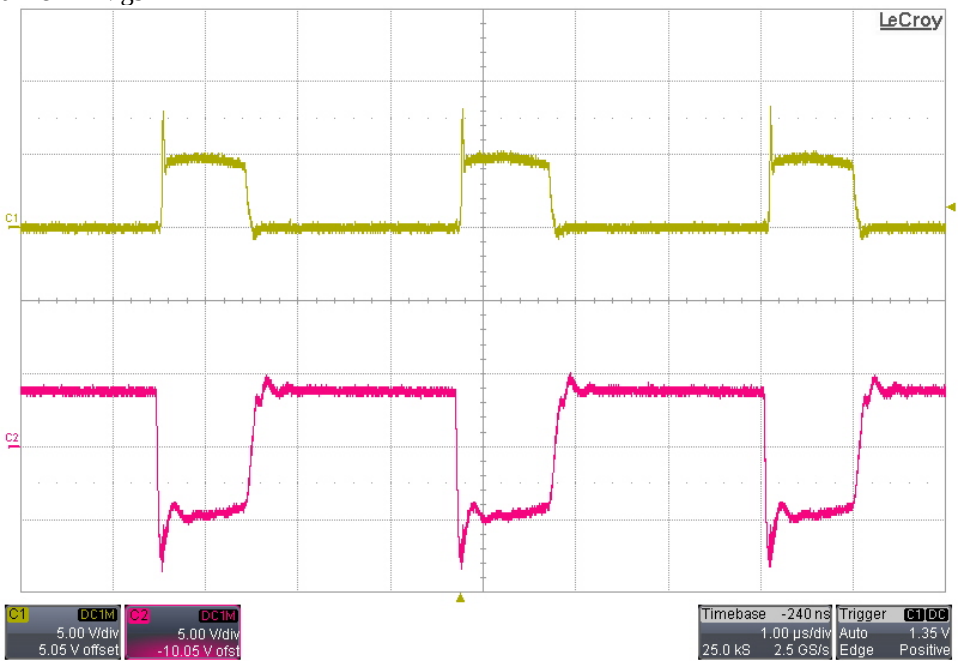
For the images below show the output was loaded with 25A.

10.1 Primary FET (Q9) Vds – 72V Input



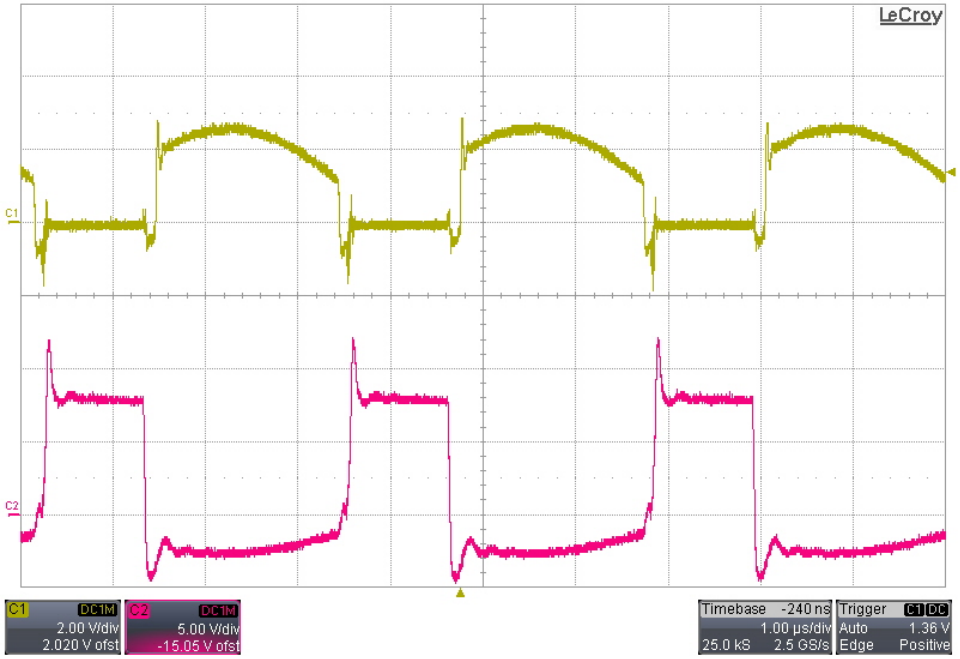
10.2 Q3 & Q6 Synchronous FETs – 36V Input

Channel – Vds; Channel 2 - Vgs



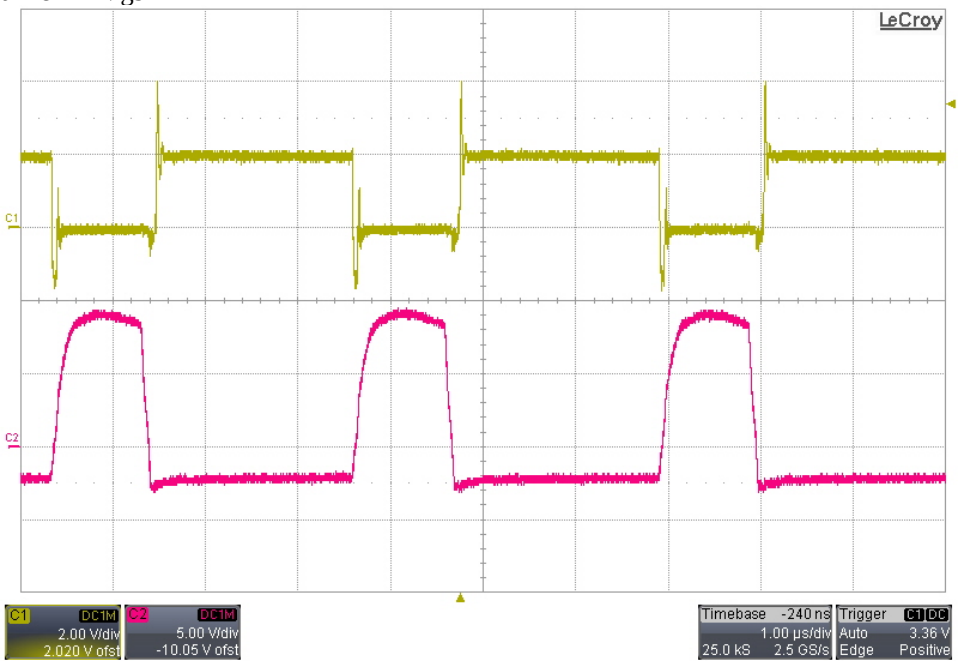
10.3 Q3 & Q6 Synchronous FETs – 72V Input

Channel – Vds; Channel 2 - Vgs



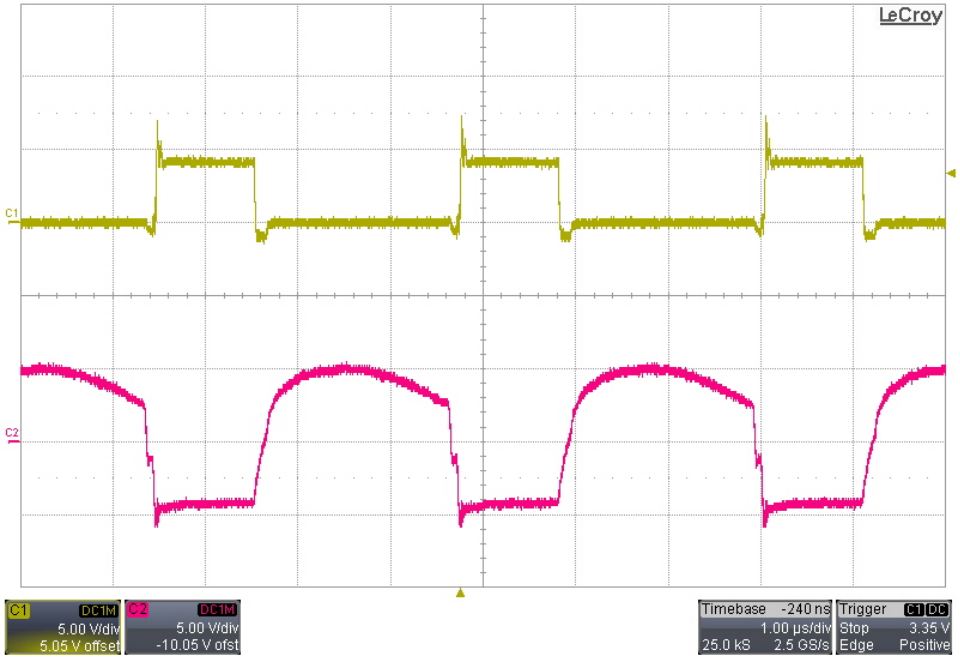
10.4 Q7 & Q8 Synchronous FETs – 36V Input

Channel – Vds; Channel 2 - Vgs



10.5 Q7 & Q8 Synchronous FETs – 72V Input

Channel – Vds; Channel 2 - Vgs



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