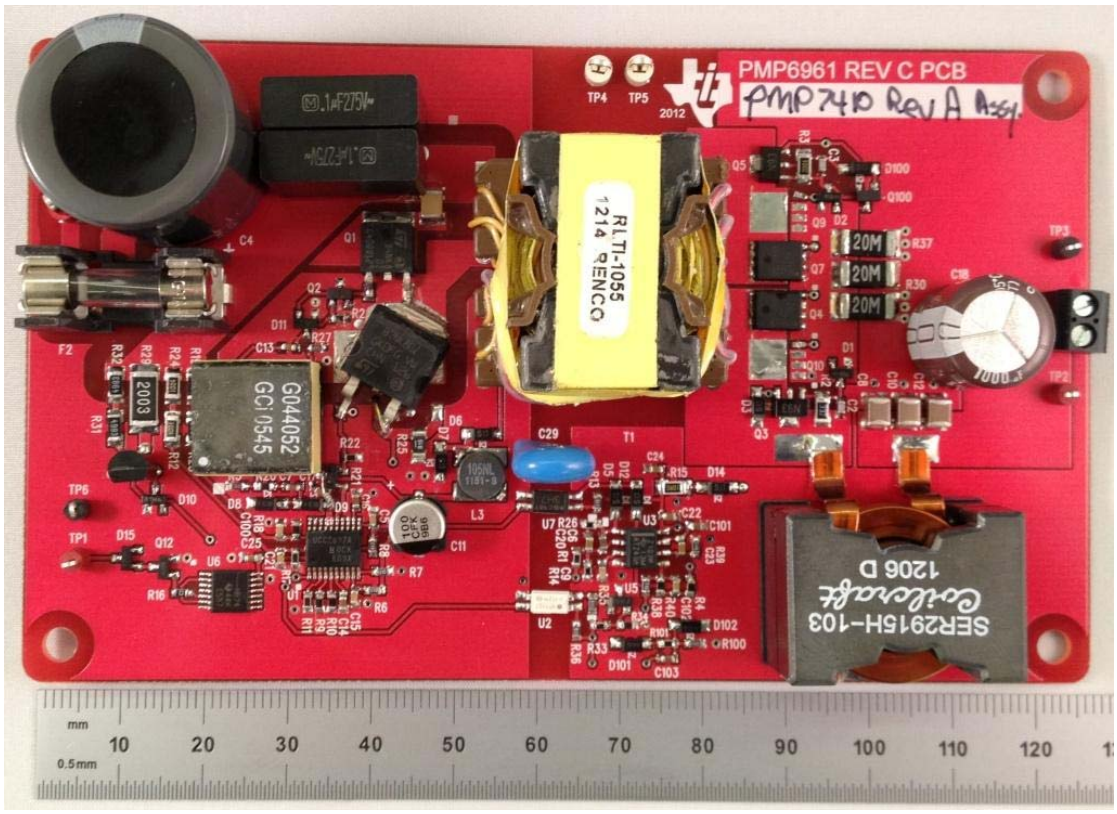
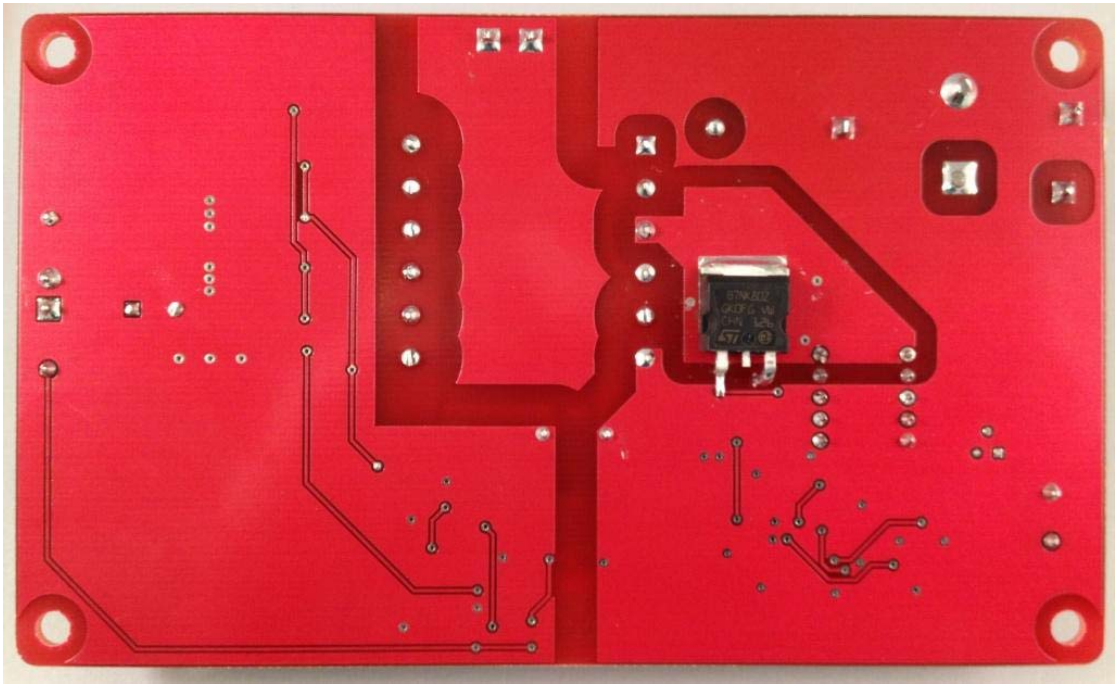
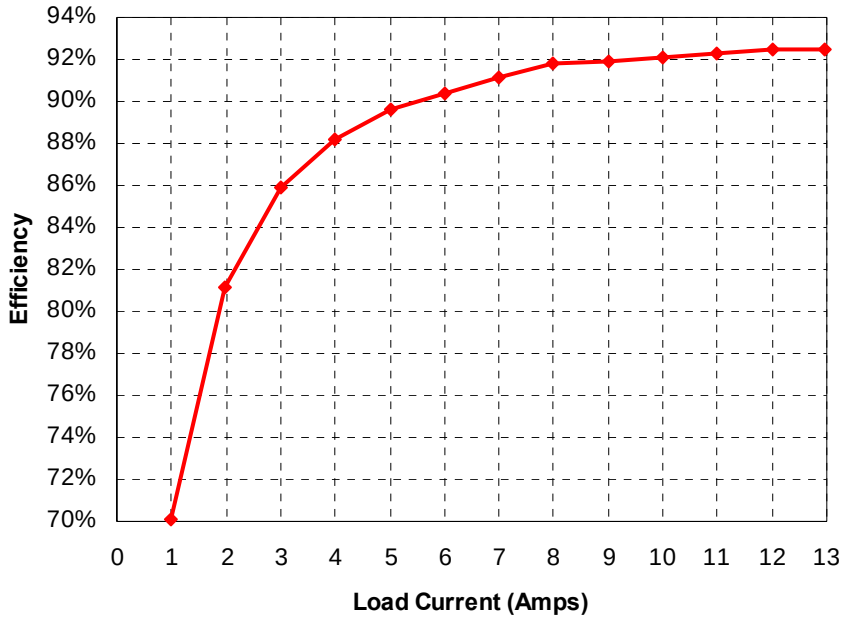
1 Photo

The photographs below show top and bottom views of the PMP7410 Rev A assembly. This circuit was built on a PMP6961 Rev C PCB.





2 Efficiency



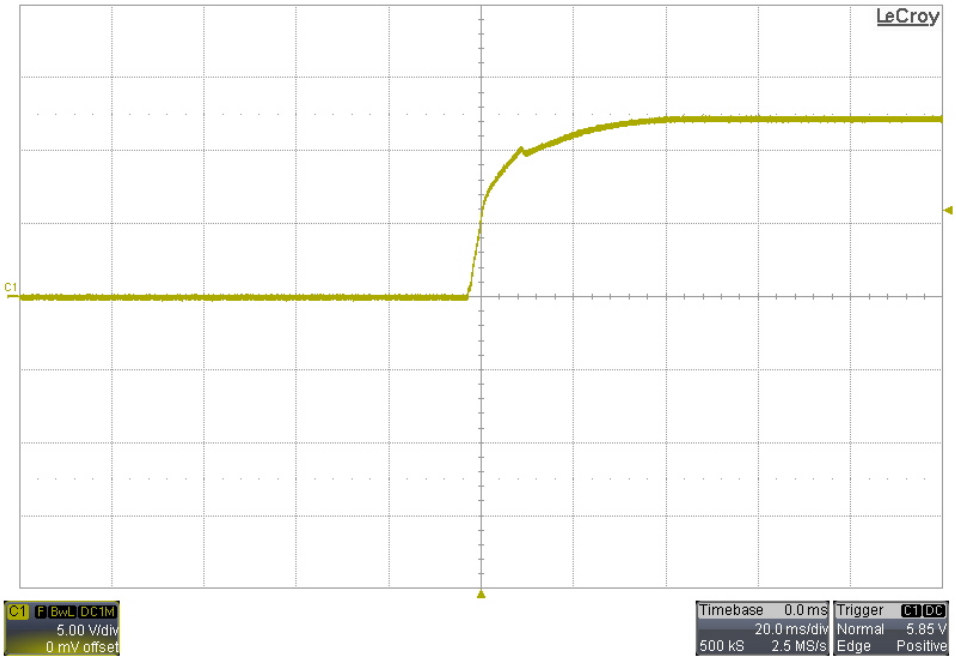
Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	12.09	353.6	0.015	0.00	5.304	0.0%
1.005	12.09	353.6	0.049	12.15	5.176	70.1%
1.994	12.09	353.6	0.084	24.11	5.595	81.2%
2.990	12.09	353.6	0.119	36.15	5.929	85.9%
3.999	12.09	353.6	0.155	48.35	6.460	88.2%
5.006	12.09	353.6	0.191	60.52	7.015	89.6%
5.998	12.09	353.6	0.227	72.52	7.751	90.3%
7.010	12.09	353.6	0.263	84.75	8.246	91.1%
8.000	12.09	353.5	0.298	96.72	8.623	91.8%
9.000	12.09	353.5	0.335	108.81	9.613	91.9%
9.990	12.09	353.5	0.371	120.78	10.369	92.1%
10.980	12.09	353.5	0.407	132.75	11.126	92.3%
12.000	12.09	353.5	0.444	145.08	11.874	92.4%
12.950	12.09	353.5	0.479	156.57	12.761	92.5%

3 Thermal Image

The ambient temperature was 25ºC with 150lfm of air flow. The input was 350VDC, and the output was loaded with 13A.

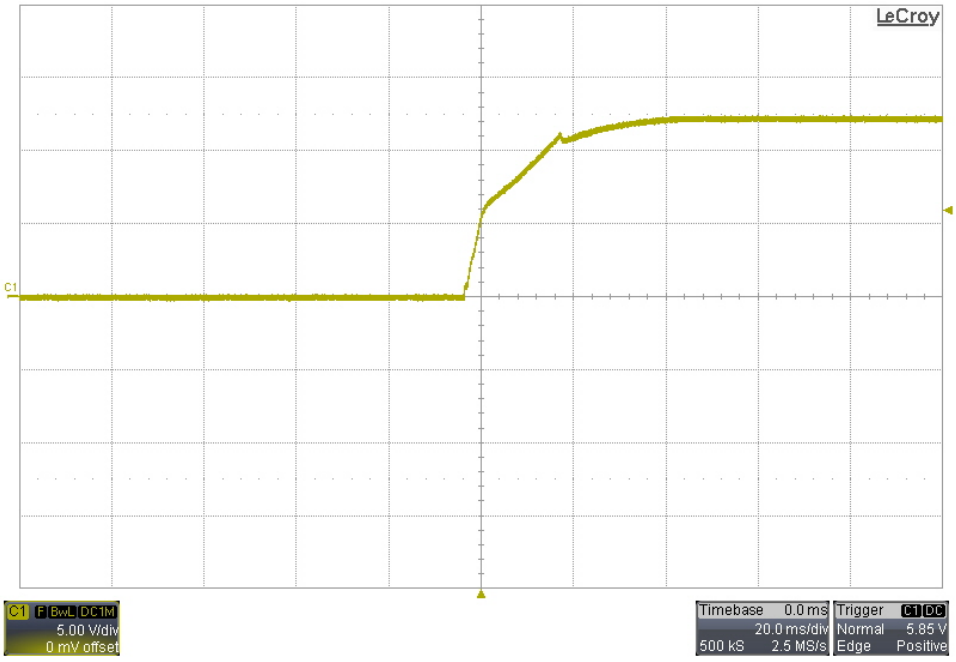
4 Startup – No Load

The input was 350VDC.



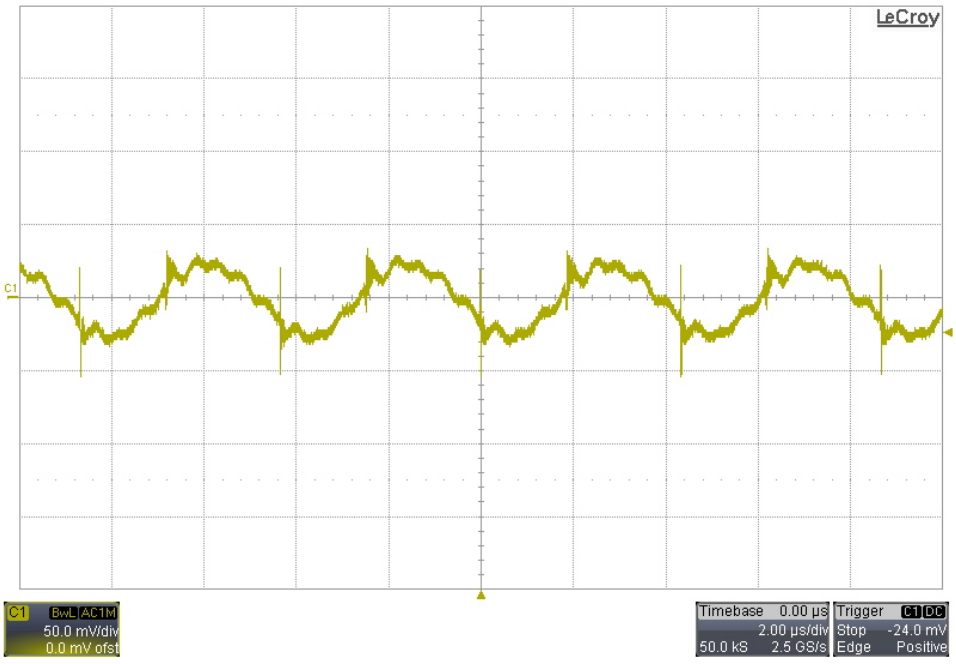
5 Startup – 4Ω Load

The input was 350VDC.



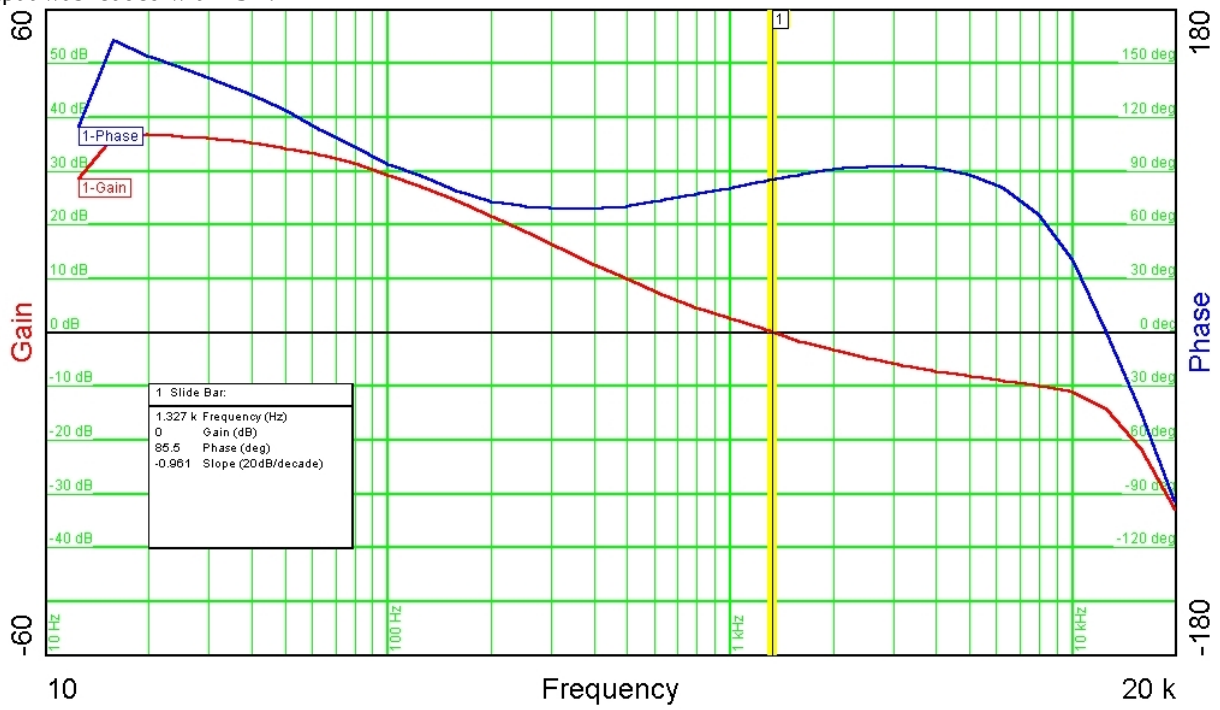
6 Output Ripple Voltage

The output ripple voltage during full load (13A) operation is shown in the plot below. The input was 350VDC.



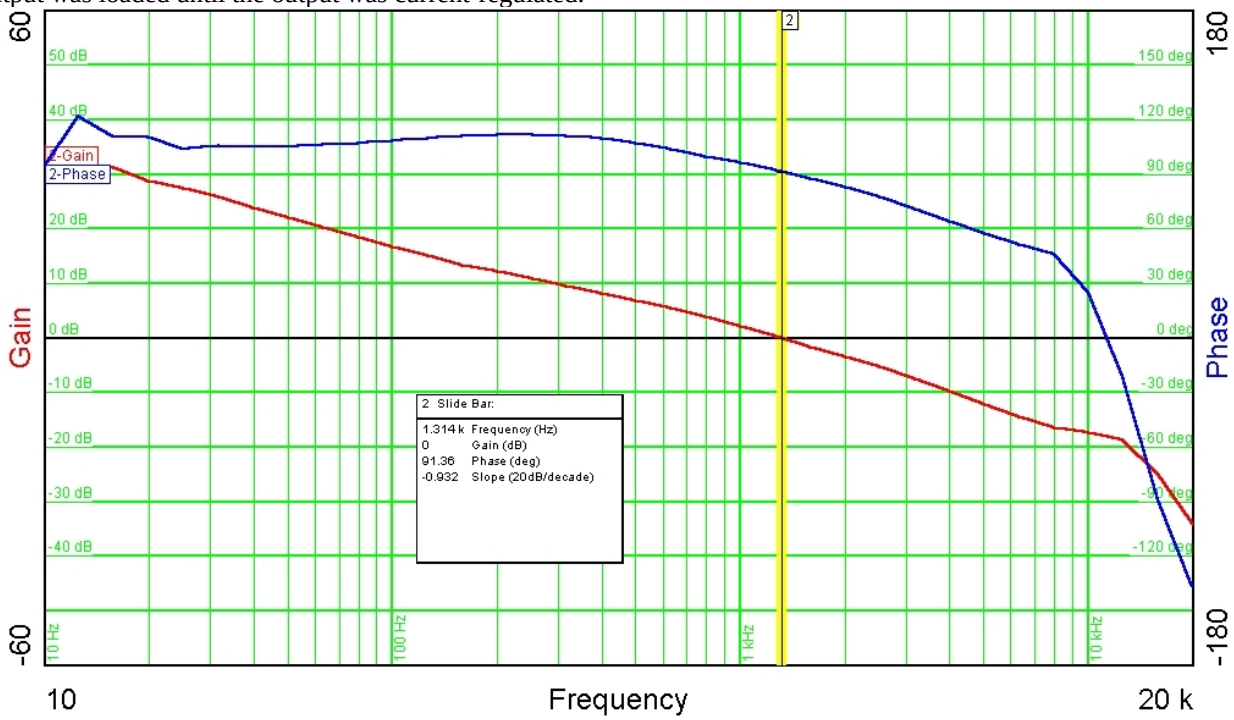
7 Voltage Loop Response

The frequency response of the voltage feedback loop is shown in the image below. The input was 350VDC and the output was loaded with 13A.



8 Current Loop Response

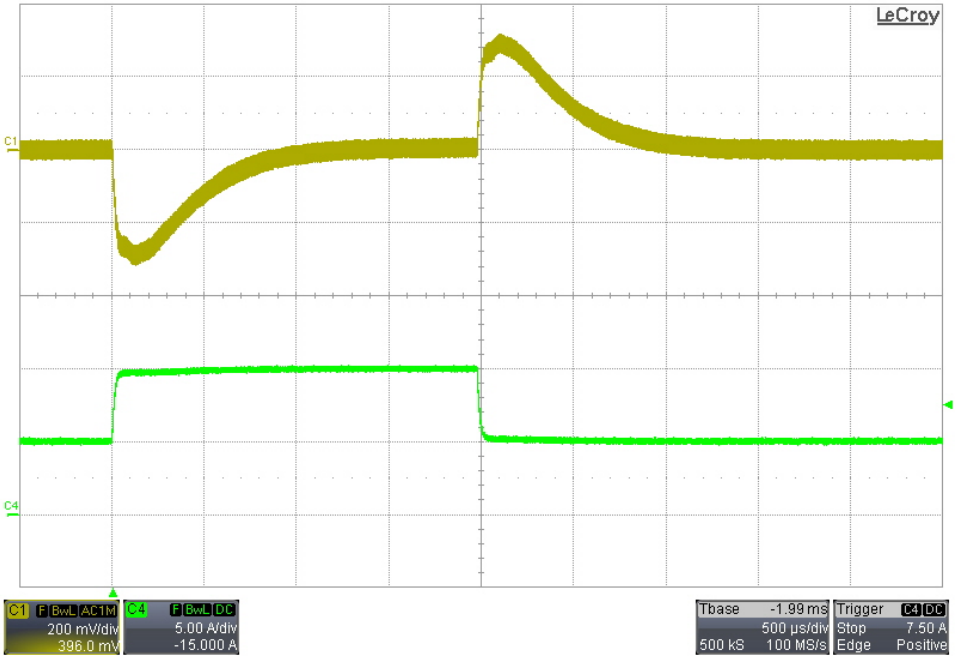
The frequency response of the over current feedback loop is shown in the image below. The input was 350VDC and the output was loaded until the output was current-regulated.



9 Load Transients

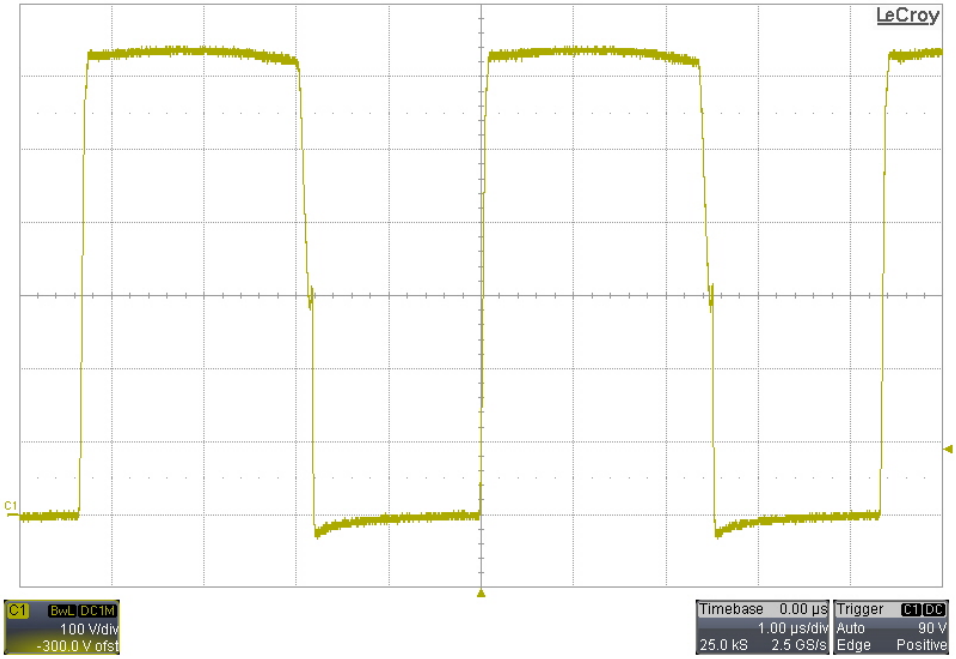
The image below shows the response to a 5A to 10A load transient. The input voltage was set to 350VDC.

Channel 1: Vout (ac coupled) 200mV/div Channel 4: Iout 5A/div



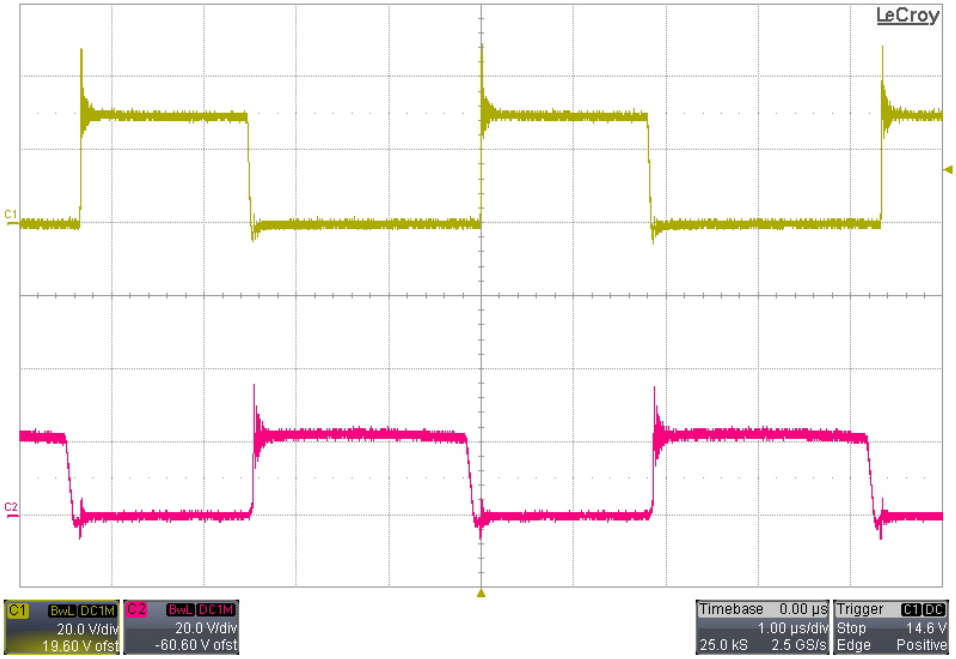
10 Switching Waveforms – Primary Side

The image below shows the switching voltage waveform on the drain of the primary FETs (Q6 and Q11). The load was 13A and the input was set to 350VDC.



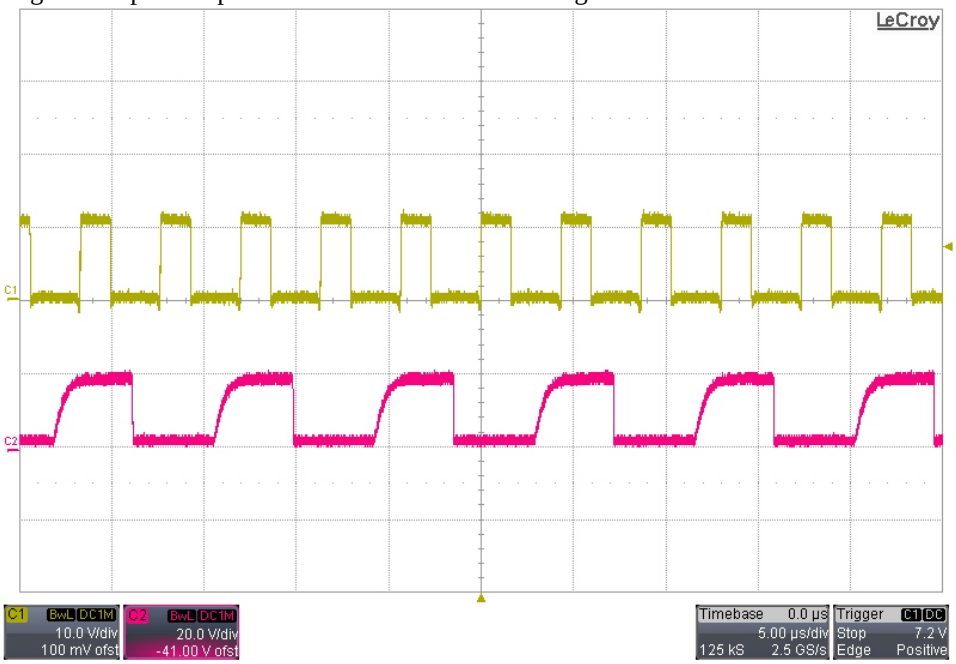
11 Switching Waveforms – Secondary Side

The image below shows the switching voltage waveform on the drains of the secondary FETs. The load was 13A and the input was set to 350VDC. Channel 1 shows the drain-to-source voltage on Q 4. Channel 2 shows the drain-to-source voltage on Q7.



12 Synchronization Output

Channel 1 shows the voltage on the gate of the primary FETs (Q6 and Q11). Channel 2 shows the sync output (TP1). The sync output signal was pulled up to an external 20V source through a 30k resistor.



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