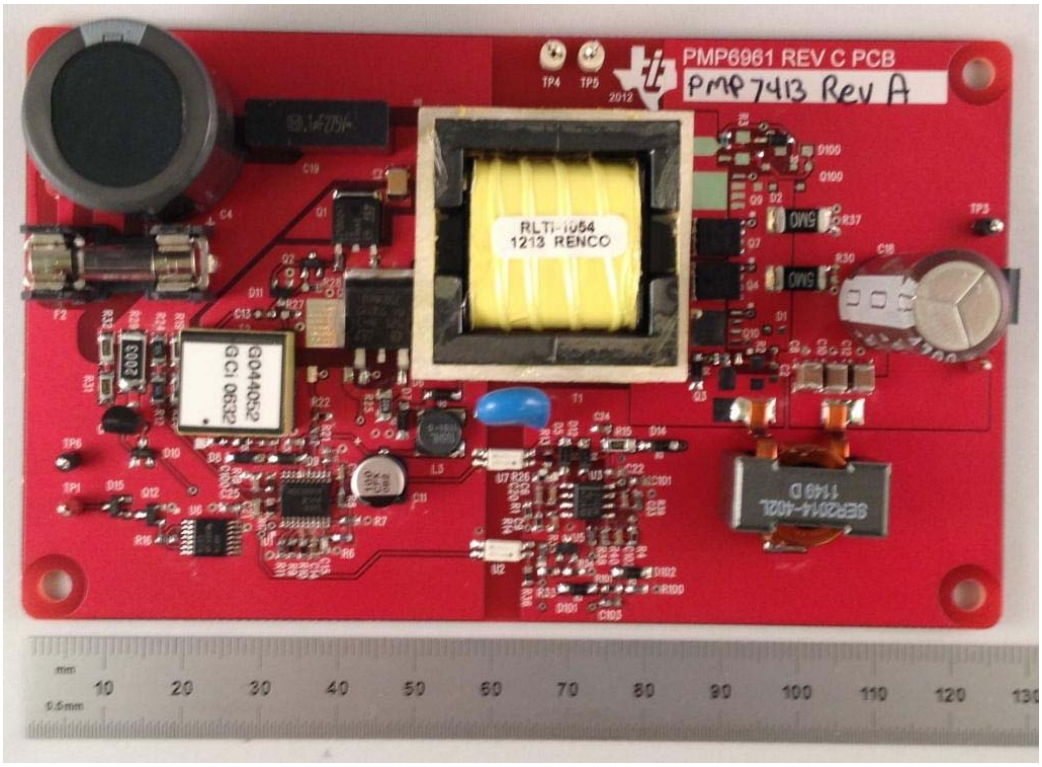
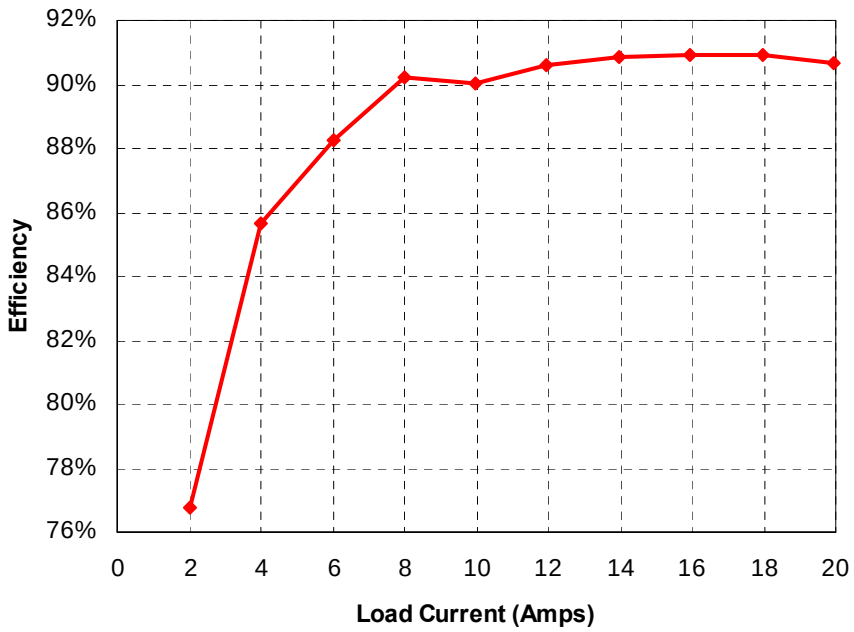
PMP7413 Rev A Test Results

1 Photo

The photograph below shows the PMP7413 Rev A assembly. This circuit was built on a PMP6961 Rev C PCB.



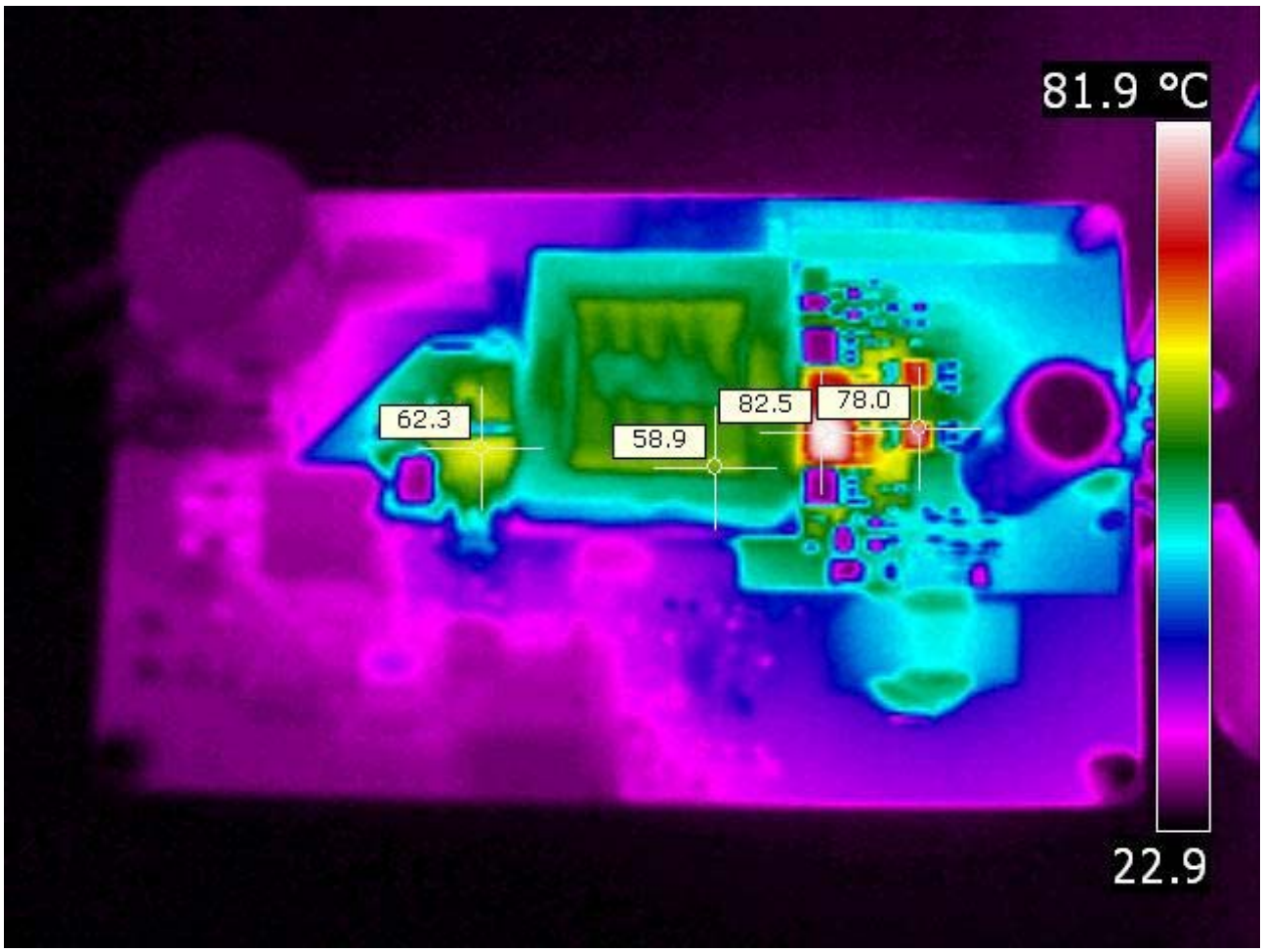
2 Efficiency



Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	5.00	354.6	0.008	0.00	2.837	0.0%
2.015	5.00	354.6	0.037	10.08	3.045	76.8%
4.009	5.00	354.6	0.066	20.05	3.359	85.6%
6.007	5.00	354.6	0.096	30.04	4.007	88.2%
8.00	5.00	354.6	0.125	40.00	4.325	90.2%
9.96	5.00	354.6	0.156	49.80	5.518	90.0%
11.95	5.00	354.6	0.186	59.75	6.206	90.6%
13.95	5.00	353.7	0.217	69.75	7.003	90.9%
15.95	5.00	353.7	0.248	79.75	7.968	90.9%
17.95	5.00	353.8	0.279	89.75	8.960	90.9%
19.95	5.00	353.7	0.311	99.75	10.251	90.7%

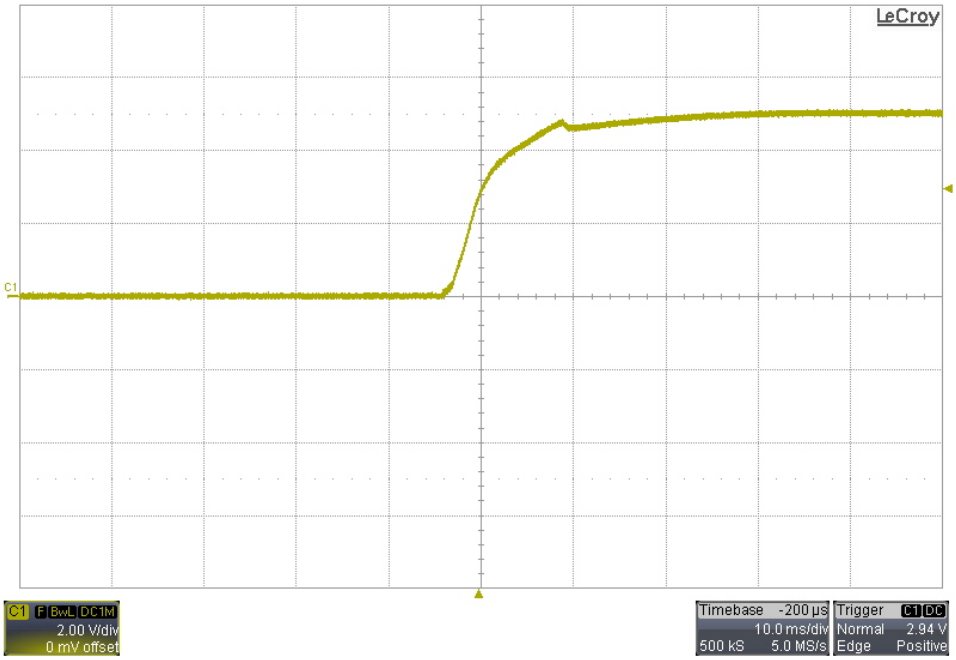
3 Thermal Image

The ambient temperature was 25ºC with 100lfm of air flow. The input was 350VDC, and the output was loaded with 20A.



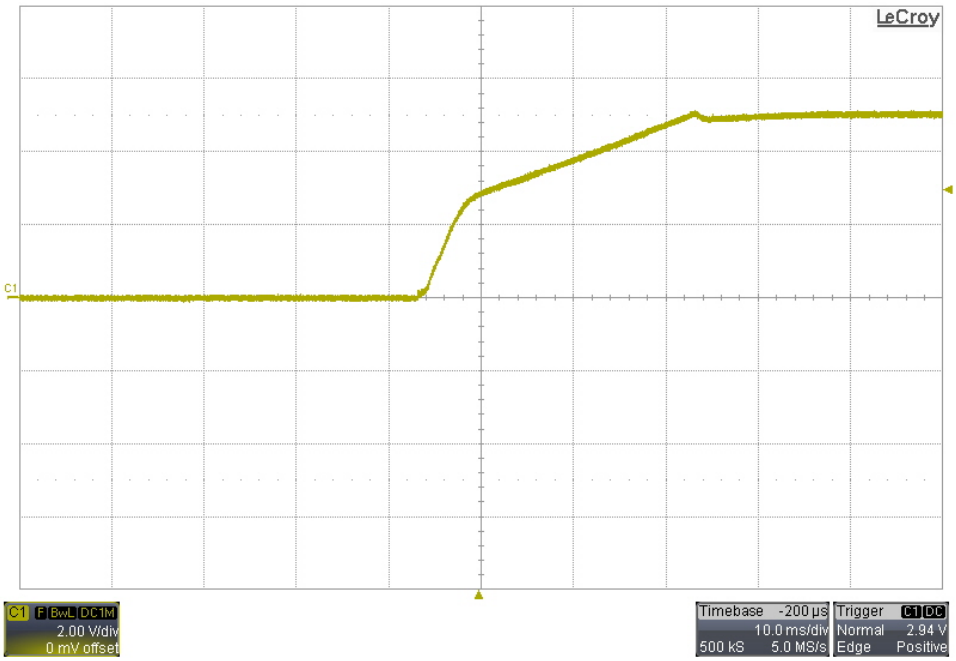
4 Startup – No Load

The input was 350VDC.



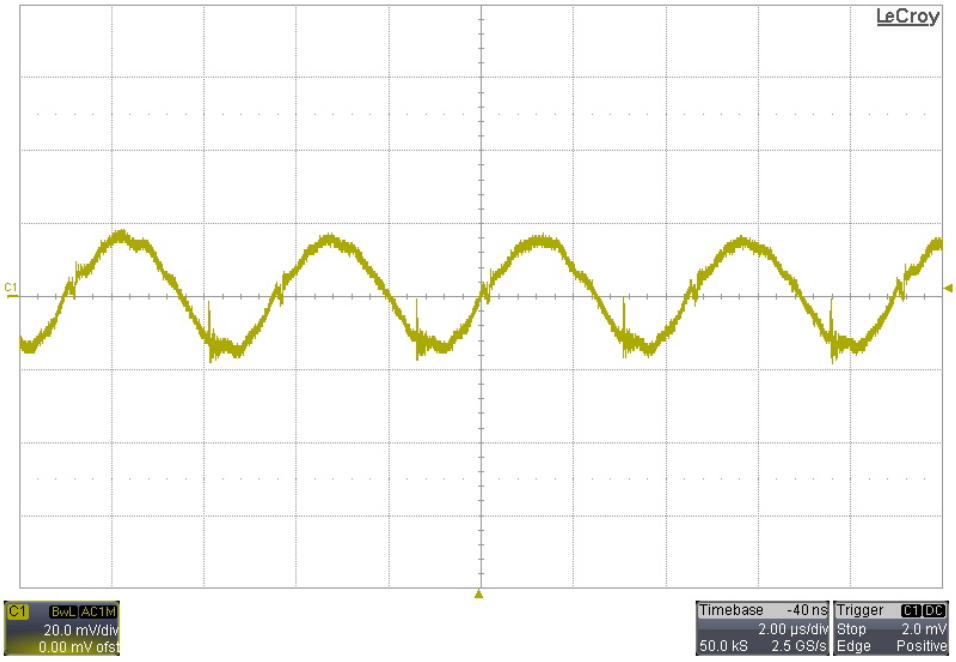
5 Startup – 0.5Ω Load

The input was 350VDC.



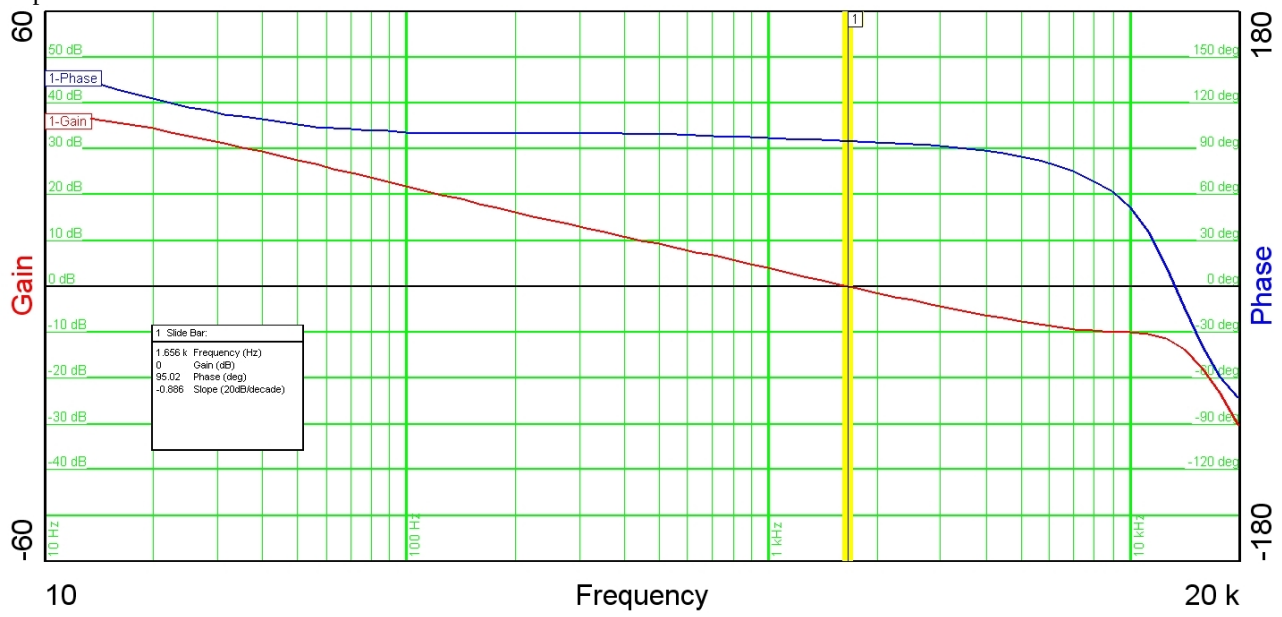
6 Output Ripple Voltage

The output ripple voltage during full load (20A) operation is shown in the plot below. The input was 350VDC.



7 Voltage Loop Response

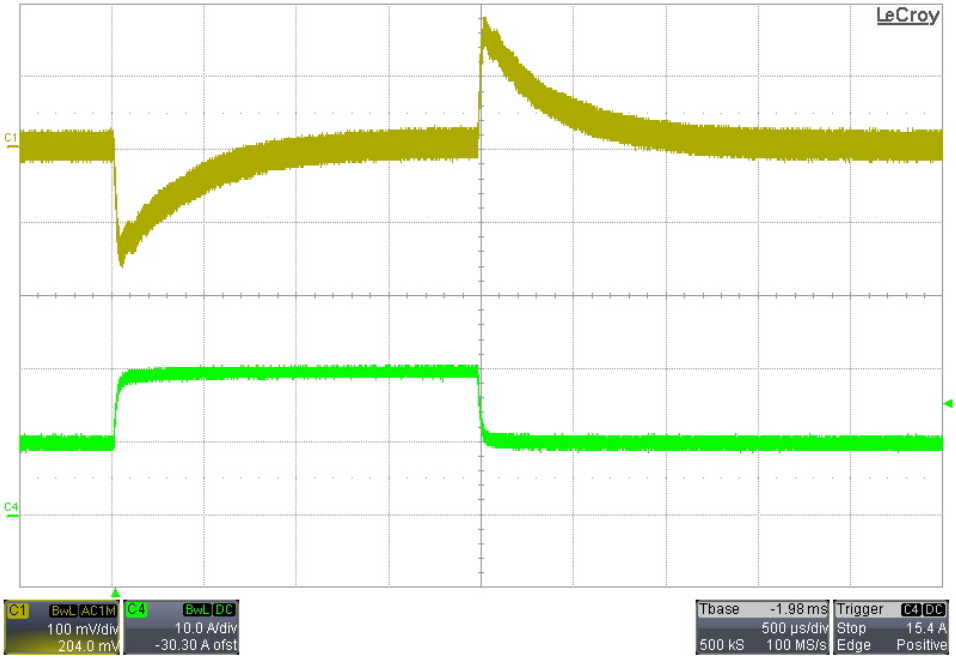
The frequency response of the voltage feedback loop is shown in the image below. The input was 350VDC and the output was loaded with 20A.



8 Load Transients

The image below shows the response to a 10A to 20A load transient. The input voltage was set to 350VDC.

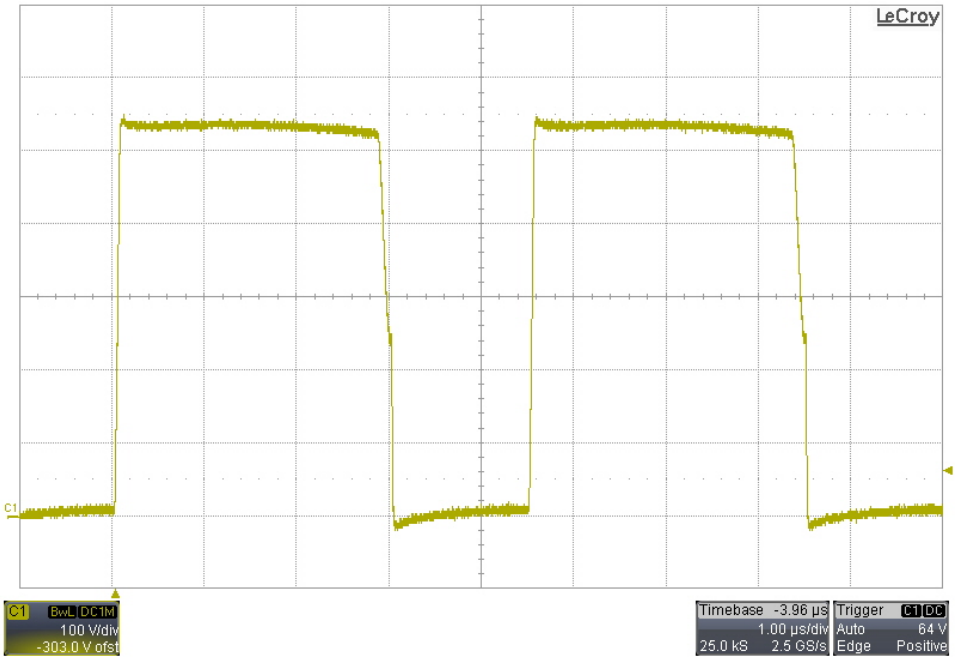
Channel 1: Vout (ac coupled) 100mV/div Channel 4: Iout 10A/div



9 Switching Waveforms

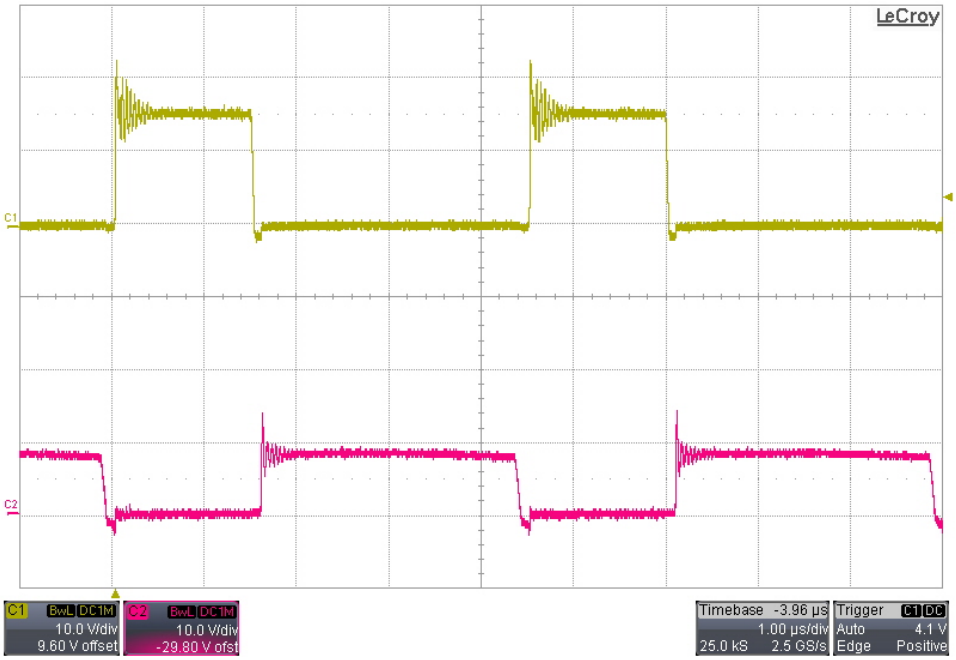
9.1 Primary FET Drain Voltage

The image below shows the drain voltage on the primary MOSFET (Q6). The load was 20A and the input was set to 350VDC.



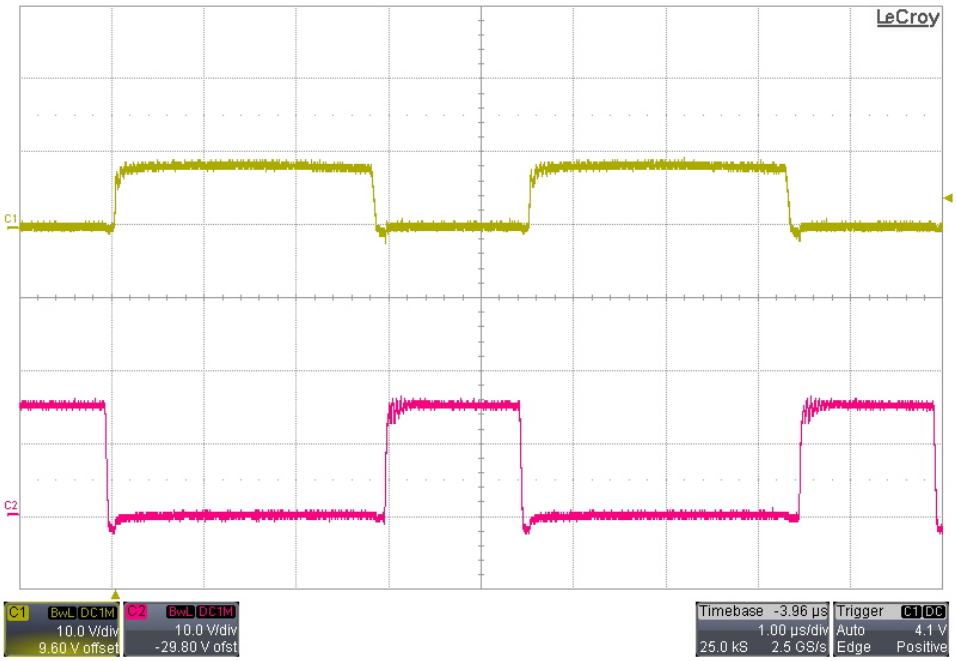
9.2 Synchronous Rectifier Drain Voltages

Channel 1 shows the drain voltage on Q4. Channel 2 shows the drain voltage on Q7. The load was 20A and the input was set to 350VDC.



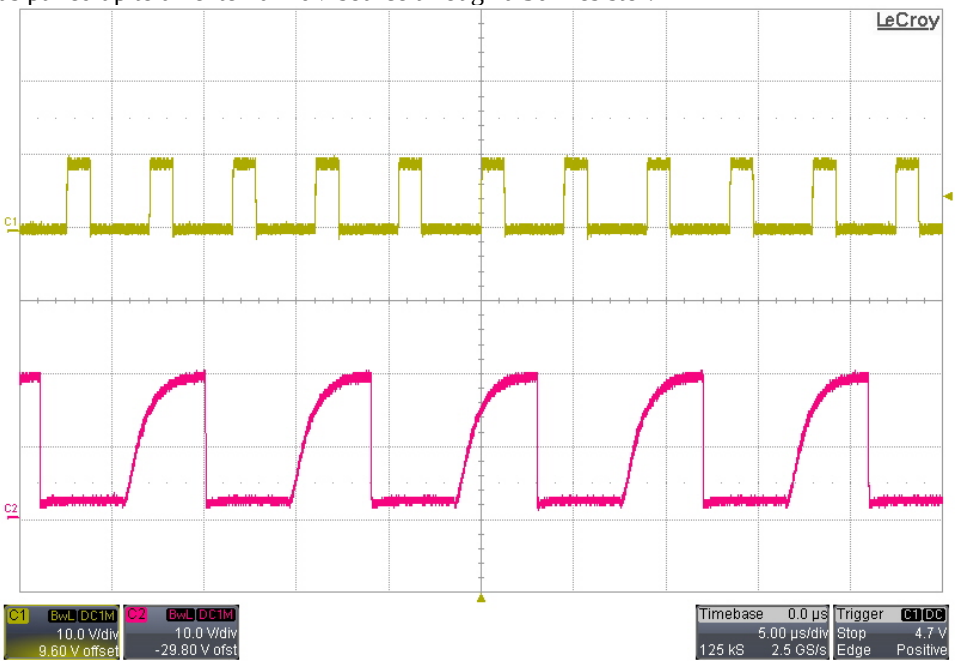
9.3 Synchronous Rectifier Gate Voltages

Channel 1 shows the gate voltage on Q4. Channel 2 shows the gate voltage on Q7. The load was 20A and the input was set to 350VDC.



10 Synchronization Output

Channel 1 shows the voltage on the gate of the main FET (Q6). Channel 2 shows the sync output (TP1). The sync output signal was pulled up to an external 20V source through a 30k resistor.



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