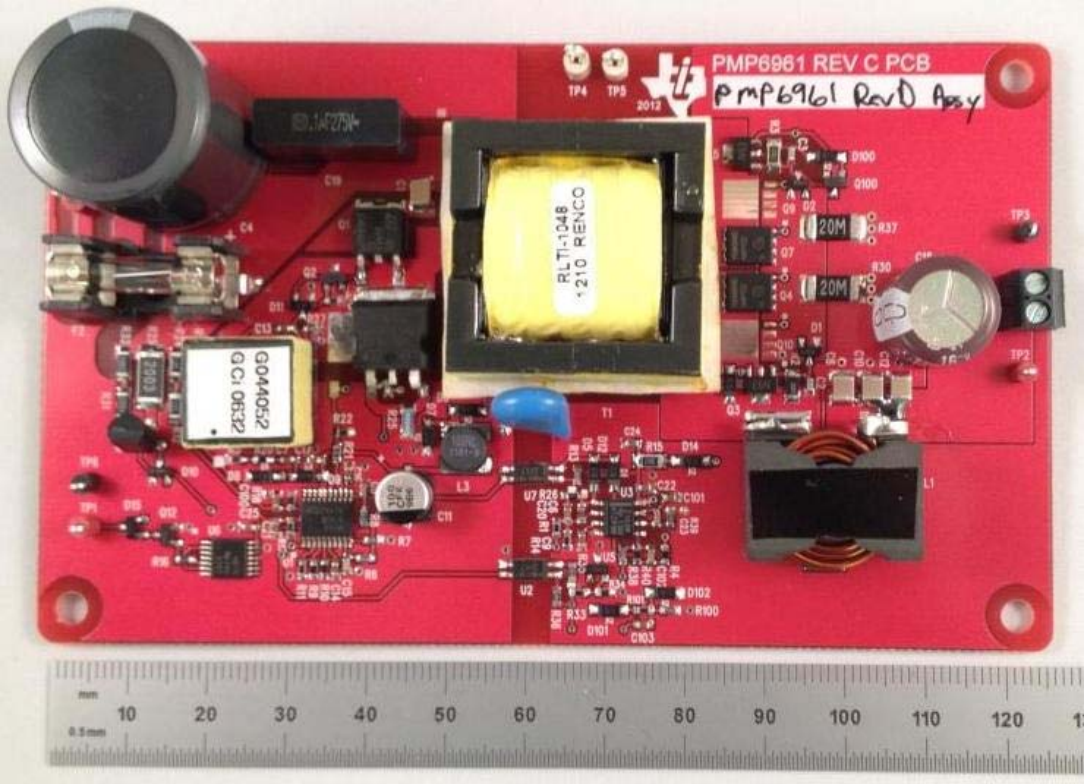
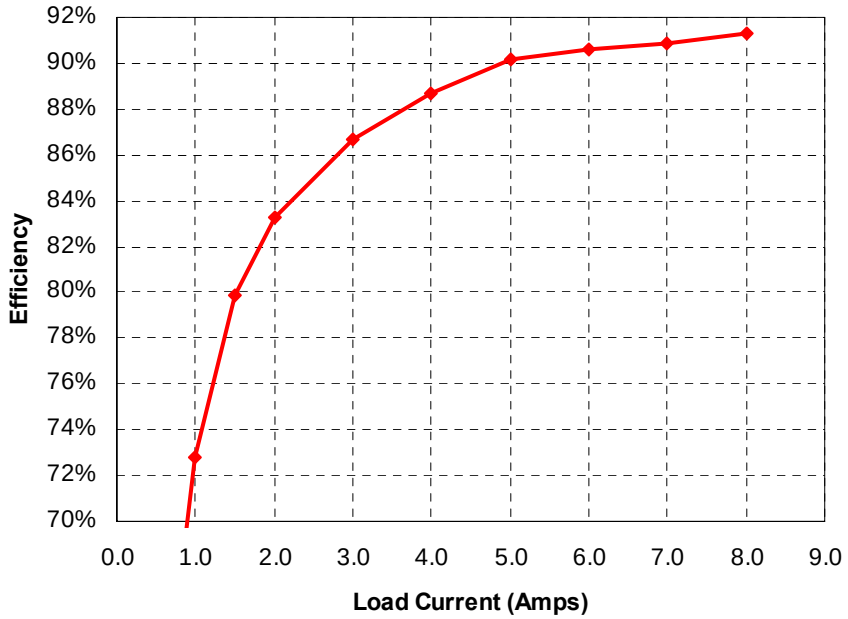
PMP6961 Rev D Test Results

1 Photo

The photograph below shows the PMP6961 Rev D assembly. This circuit was built on a PMP6961 Rev C PCB.



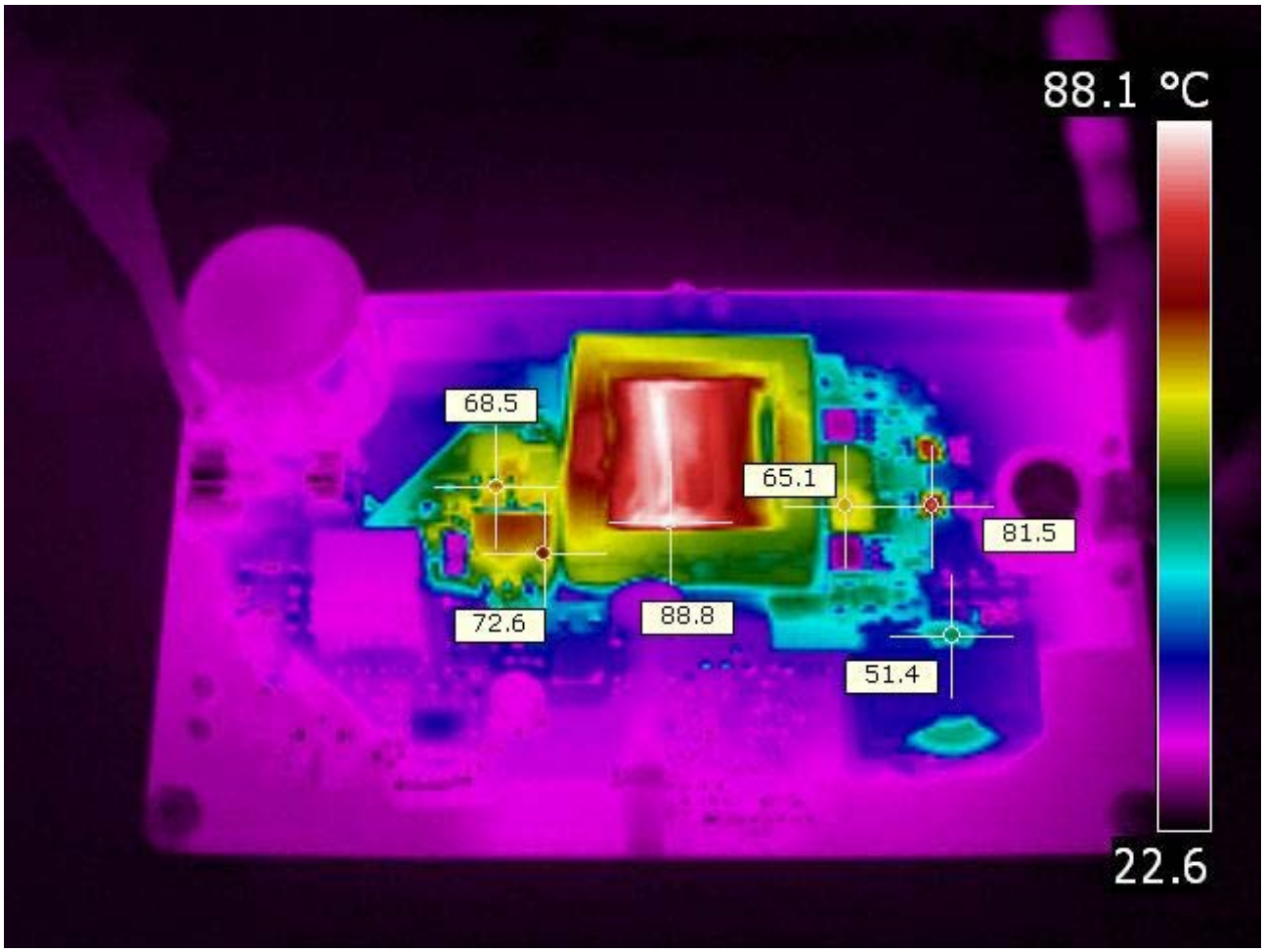
2 Efficiency



Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	12.05	353.2	0.012	0.00	4.238	0.0%
0.494	12.05	353.2	0.029	5.95	4.290	58.1%
1.003	12.05	353.2	0.047	12.09	4.514	72.8%
1.499	12.05	353.2	0.064	18.06	4.542	79.9%
2.001	12.05	353.2	0.082	24.11	4.850	83.3%
2.998	12.05	353.2	0.118	36.13	5.552	86.7%
4.002	12.05	353.2	0.154	48.22	6.169	88.7%
4.997	12.05	353.2	0.189	60.21	6.541	90.2%
6.000	12.05	353.2	0.226	72.30	7.523	90.6%
6.980	12.05	353.2	0.262	84.11	8.429	90.9%
8.000	12.05	353.2	0.299	96.40	9.207	91.3%
8.330	12.05	353.2	0.312	100.38	9.822	91.1%

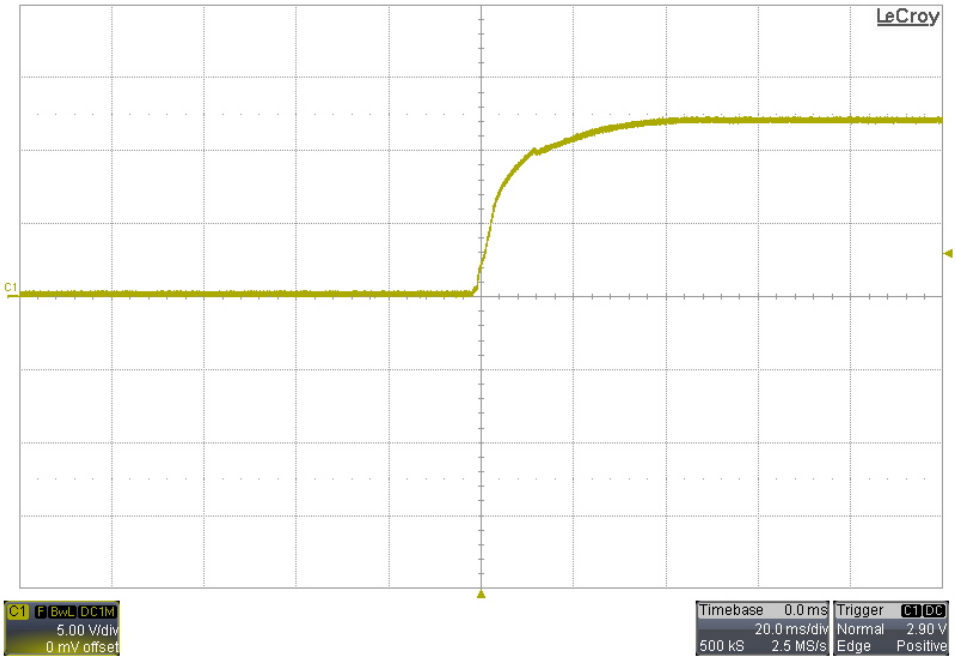
3 Thermal Image

The ambient temperature was 25ºC with 150lfm of air flow. The input was 350VDC, and the output was loaded with 8.3A.



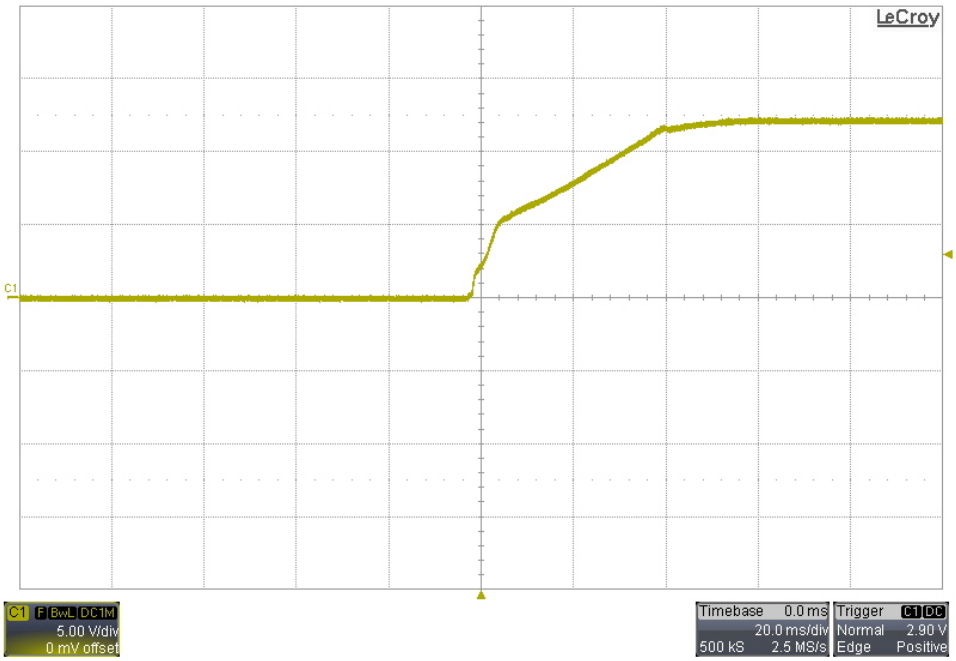
4 Startup – No Load

The input was 350VDC.



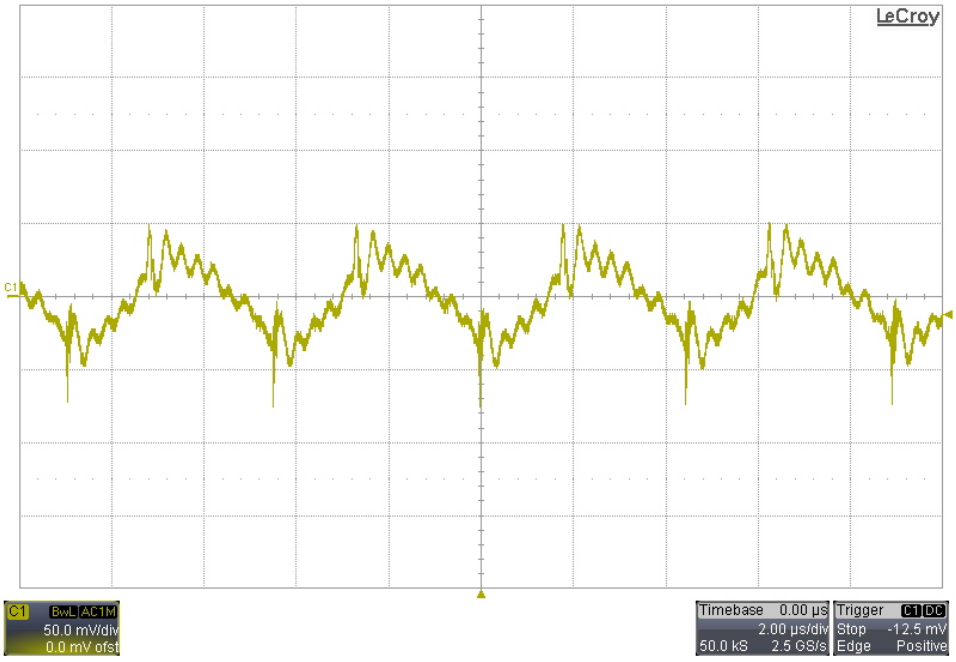
5 Startup – 2Ω Load

The input was 350VDC.



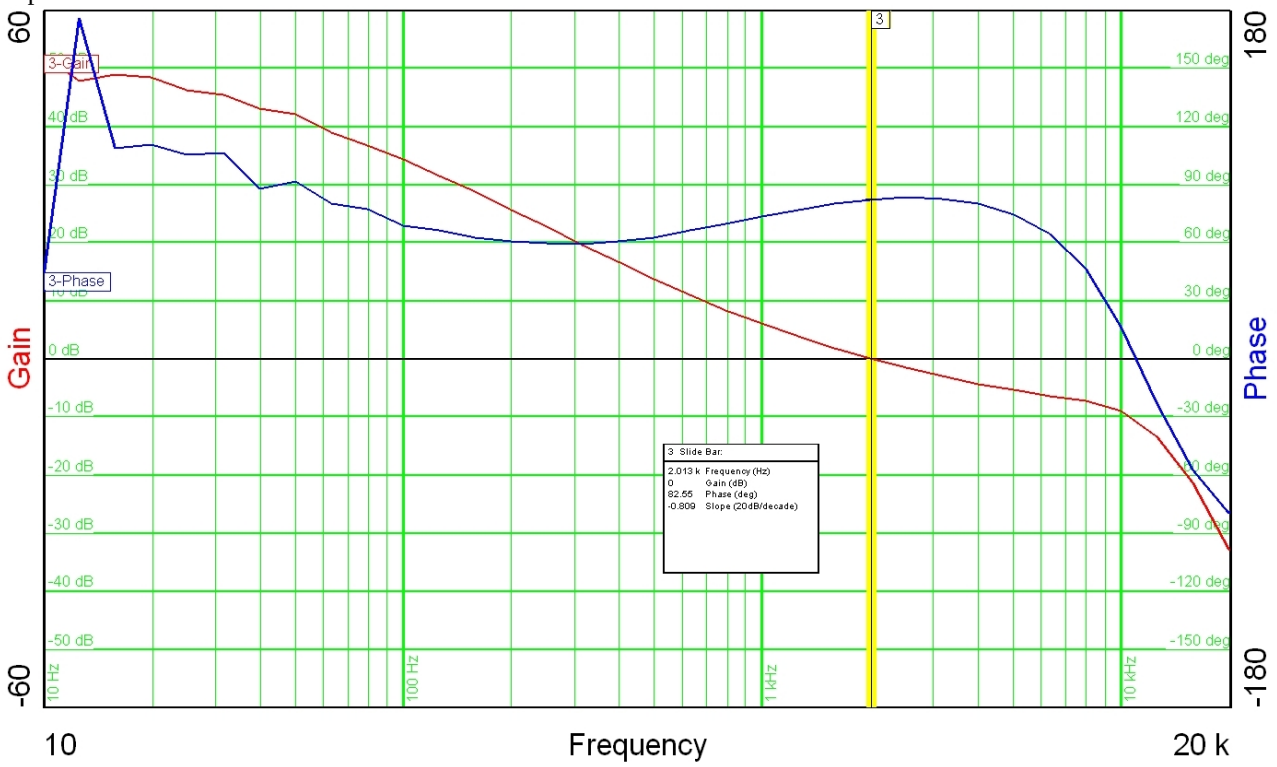
6 Output Ripple Voltage

The output ripple voltage during full load (8.3A) operation is shown in the plot below. The input was 350VDC.



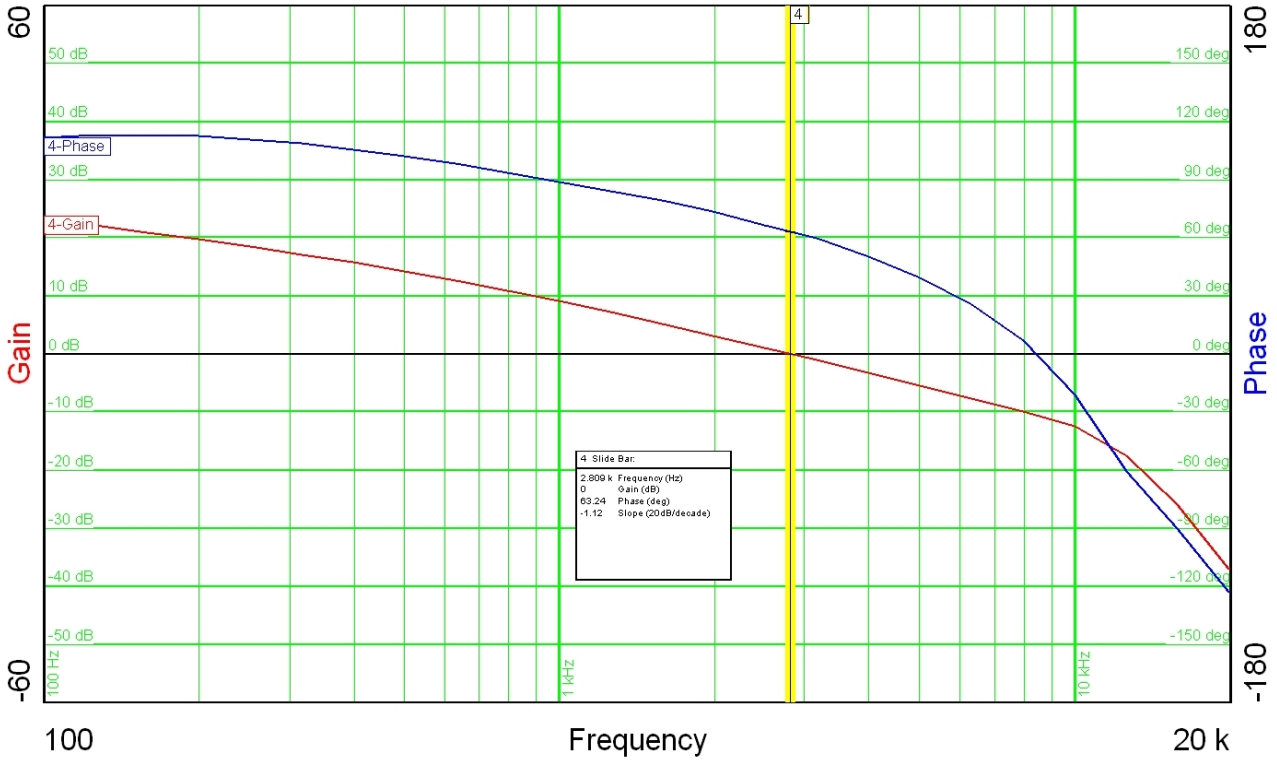
7 Voltage Loop Response

The frequency response of the voltage feedback loop is shown in the image below. The input was 350VDC and the output was loaded with 8.3A.



8 Current Loop Response

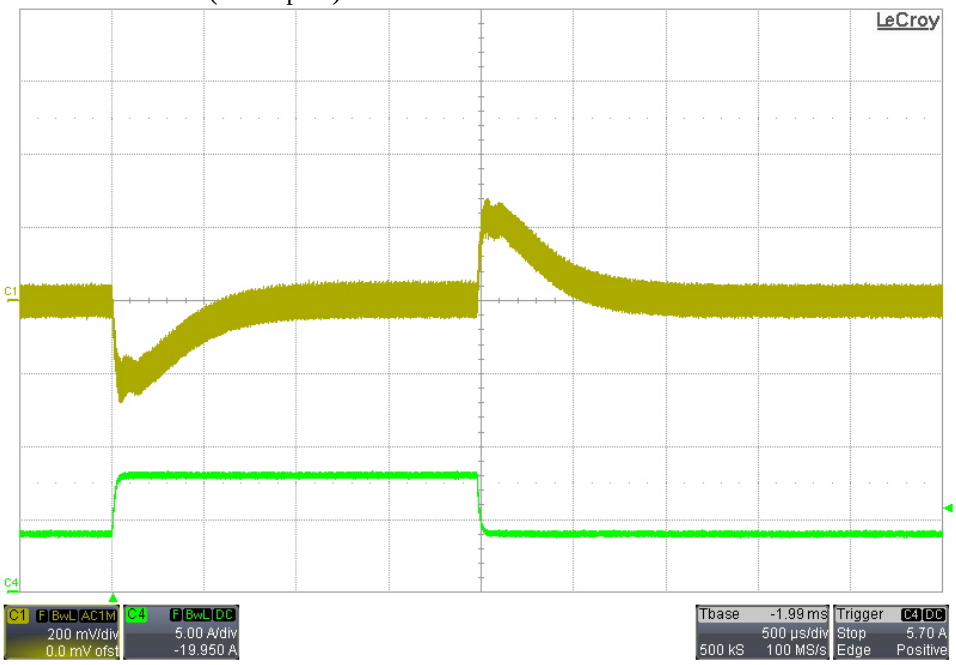
The frequency response of the over current feedback loop is shown in the image below. The input was 350VDC and the output was loaded until the output was current-regulated.



9 Load Transients

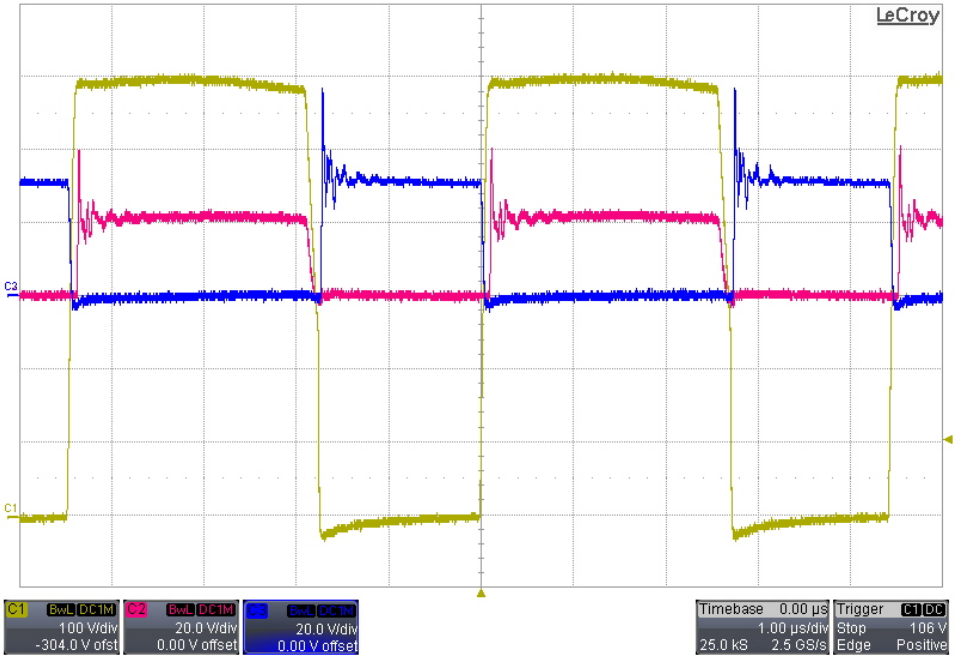
The image below shows the response to a 4A to 8A load transient. The input voltage was set to 350VDC.

Channel 1: Vout (ac coupled) 200mV/div Channel 4: Iout 5A/div



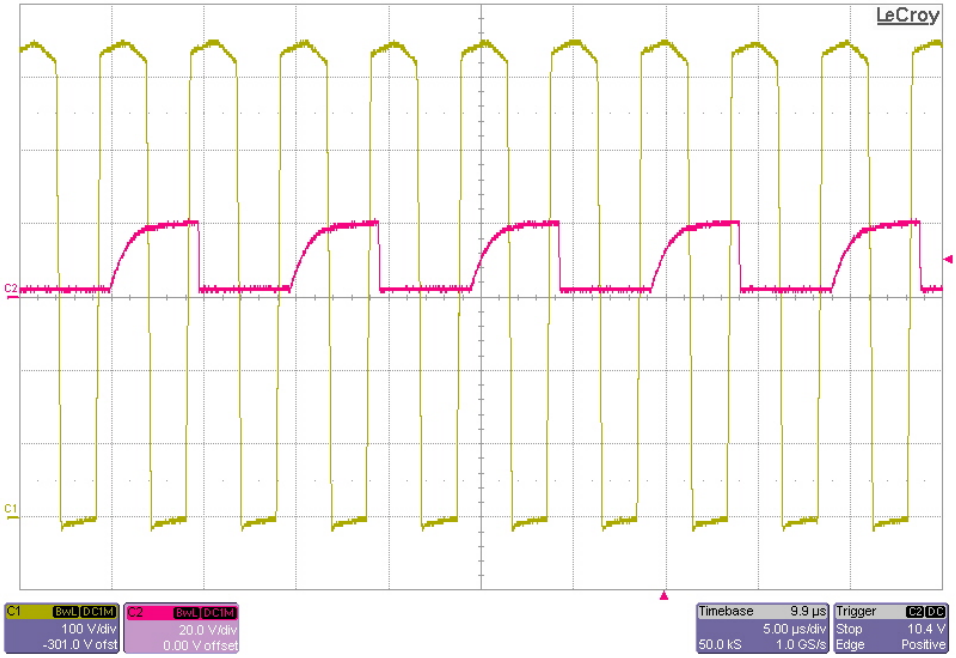
10 Switching Waveforms

The image below shows the switching voltage waveforms. The load was 8.3A and the input was set to 350VDC. The drain-to-source voltage on the primary MOSFET (Q6) is shown on Channel 1. The drain-to-source voltage on the synchronous MOSFET (Q7) is shown on Channel 2. The drain-to-source voltage on the synchronous MOSFET (Q4) is shown on Channel 3.



11 Synchronization Output

Channel 1 shows the voltage on the drain of the main FET (Q6). Channel 2 shows the sync output (TP1). The sync output signal was pulled up to an external 20V source through a 30k resistor.



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