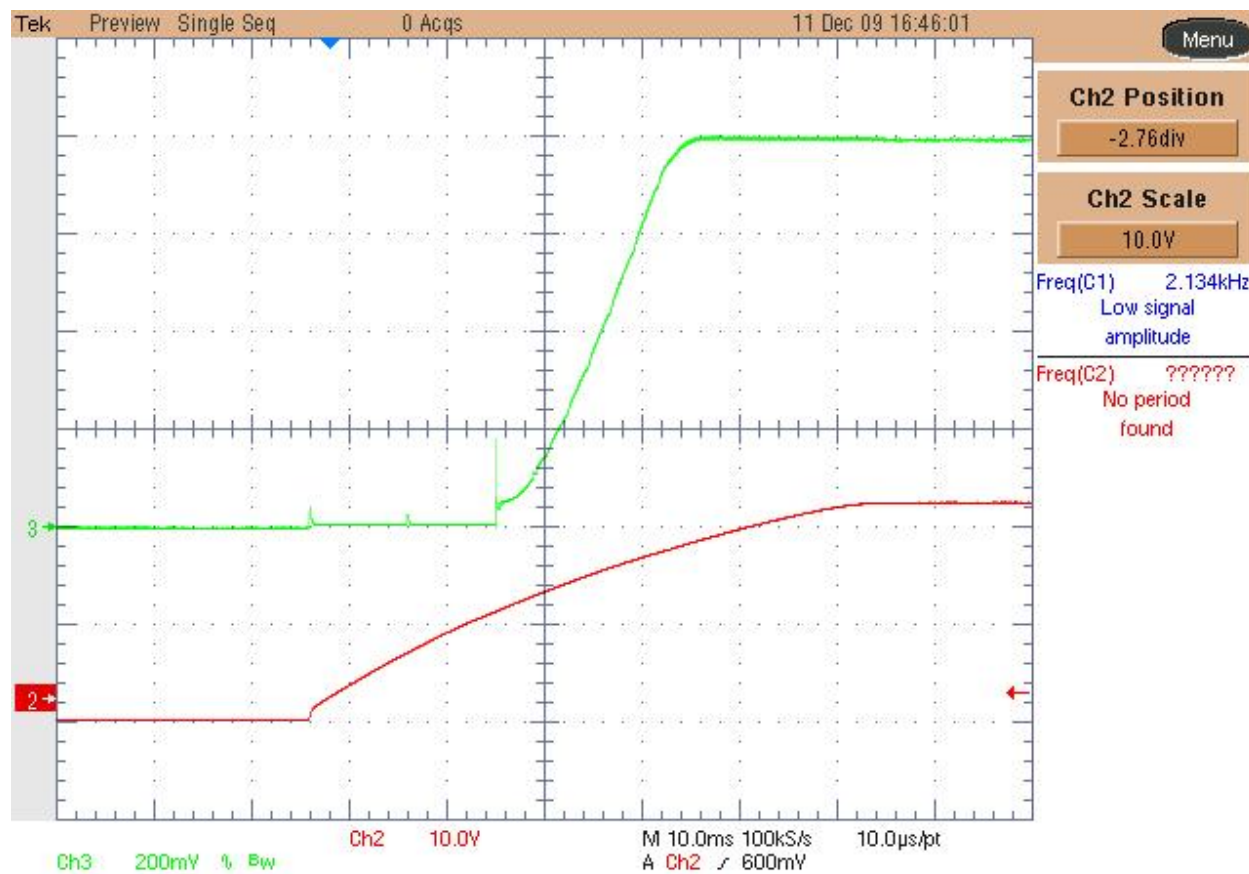


1 Startup

The input current at startup is shown in the image below. Input voltage was set to 22V. The output was loaded with an electronic load set to a constant voltage of 25V (battery load simulation).

Channel 2: Input voltage (10 V/div, 10ms/div).

Channel 3: Input current (200 mA/div).

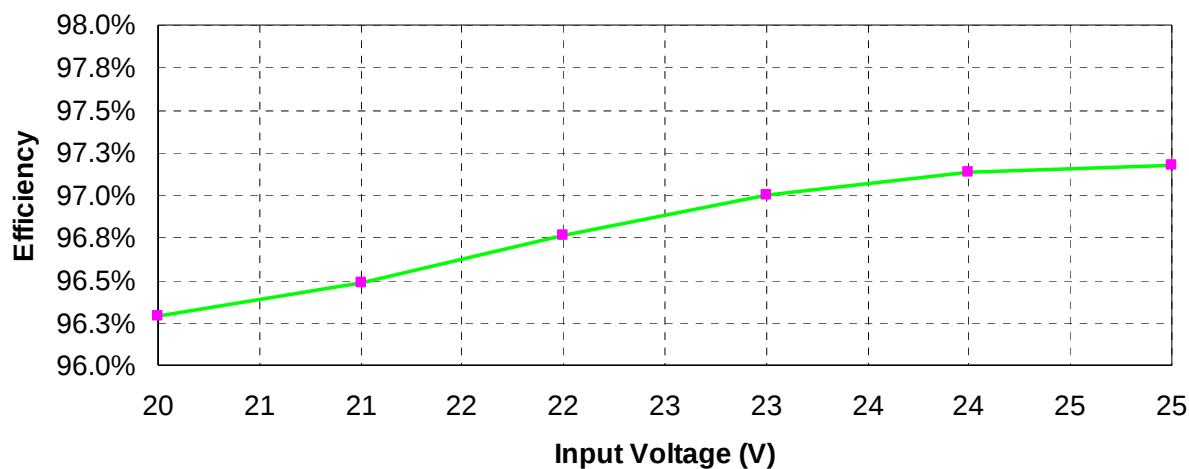


2 Efficiency

The efficiency data is shown in the tables and graph below.

The output load conditions are the same as previously described.

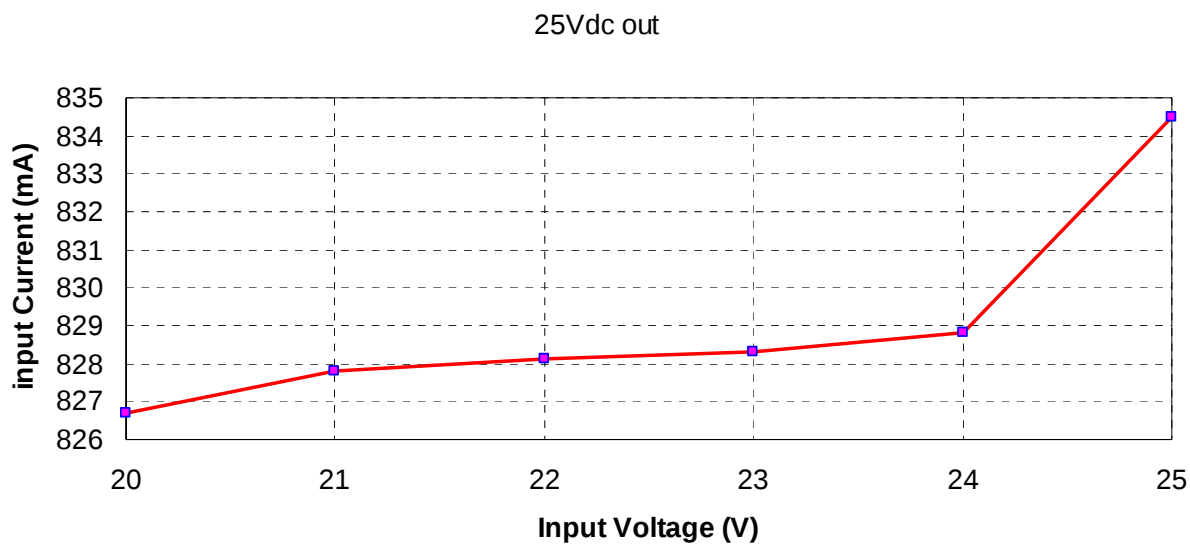
25Vdc out



I _{out} (mA)	V _{out} (V)	P _{out} (W)	I _{in} (mA)	V _{in} (V)	P _{in} (W)	P _{loss} (W)	Eff
634.8	25.08	15.92	826.7	20	16.534	0.613	96.3%
668.8	25.08	16.77	827.8	21	17.38	0.61	96.5%
702.6	25.09	17.63	828.1	22	18.22	0.59	96.8%
736.5	25.09	18.48	828.3	23	19.05	0.57	97.0%
770.1	25.09	19.32	828.8	24	19.89	0.57	97.1%
807.7	25.10	20.27	834.5	25	20.86	0.59	97.2%

3 Input Current Regulation

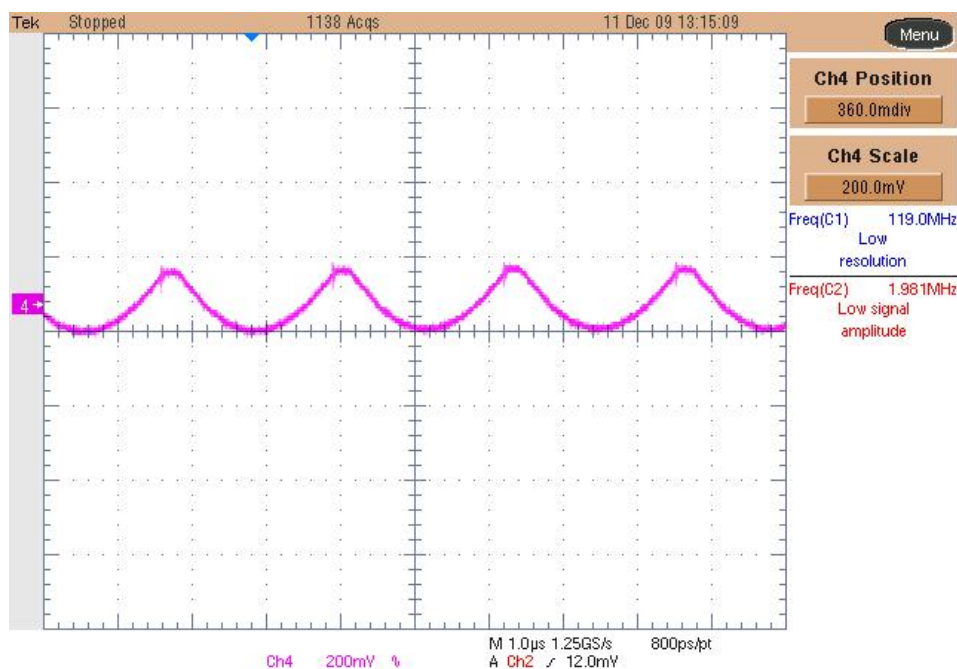
The input current versus input voltage plot is shown below.



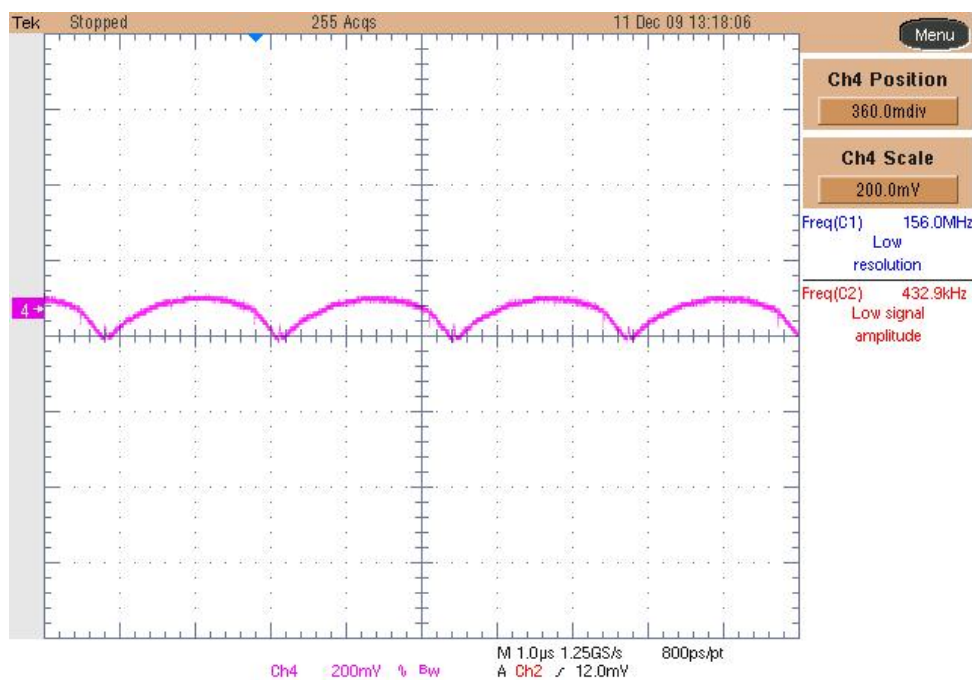
Input and Output Ripple Voltage

The ripple voltage measured at the terminal blocks are shown in the plots below. In order to simulate an input impedance from the cable connections, a 1uH inductor was connected in series at the input and output terminals. The input was set at 22V and the load was set to 25V constant.

Input voltage ripple:



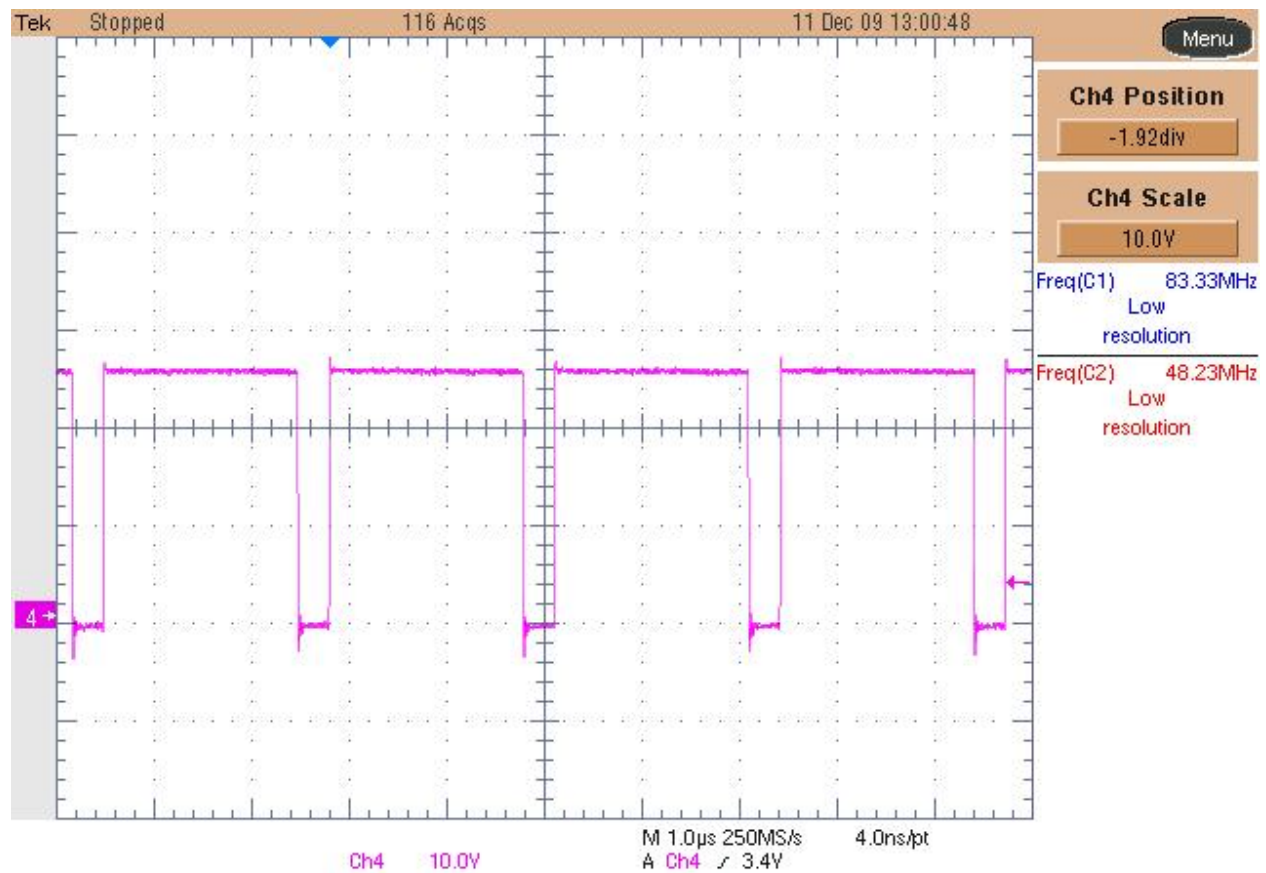
Output voltage ripple:



4 Switch-node

The image below shows the switch-node waveform. The input and output conditions are the same as above.

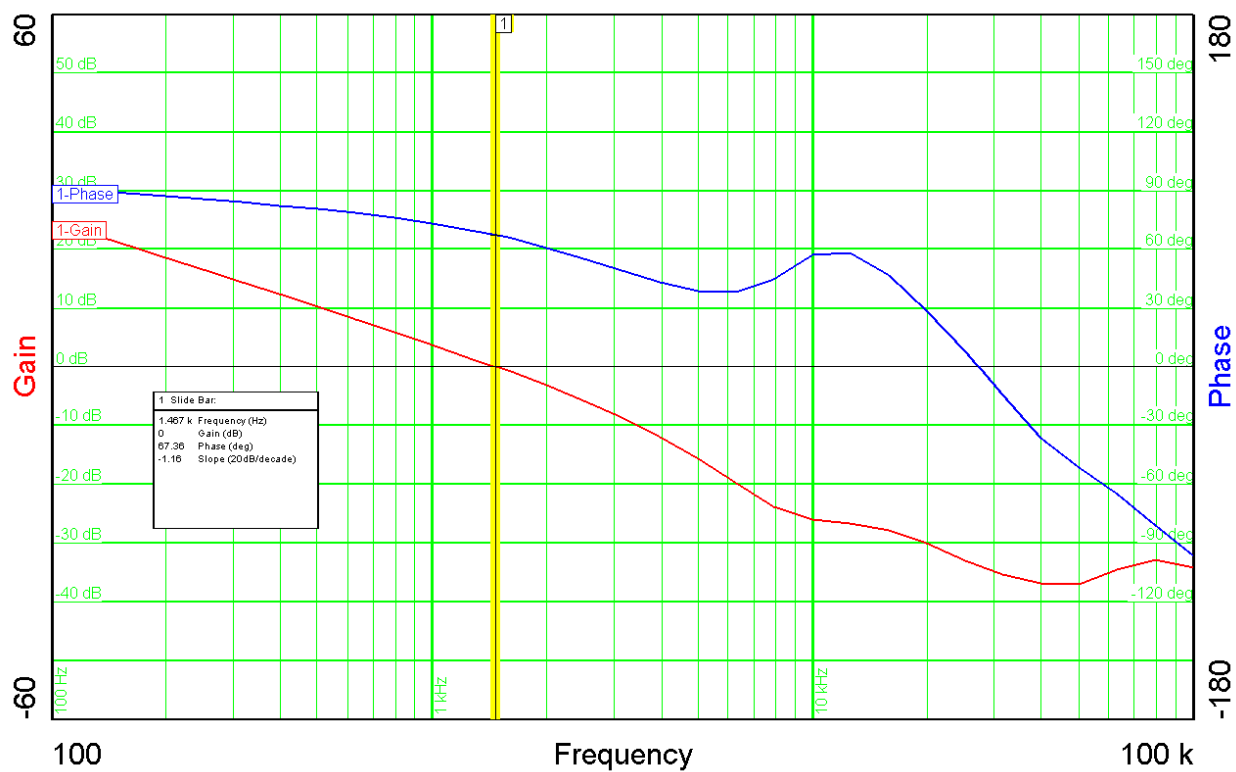
Channel 4: Vds_Q1, 10V/div, 1 μ s/div.

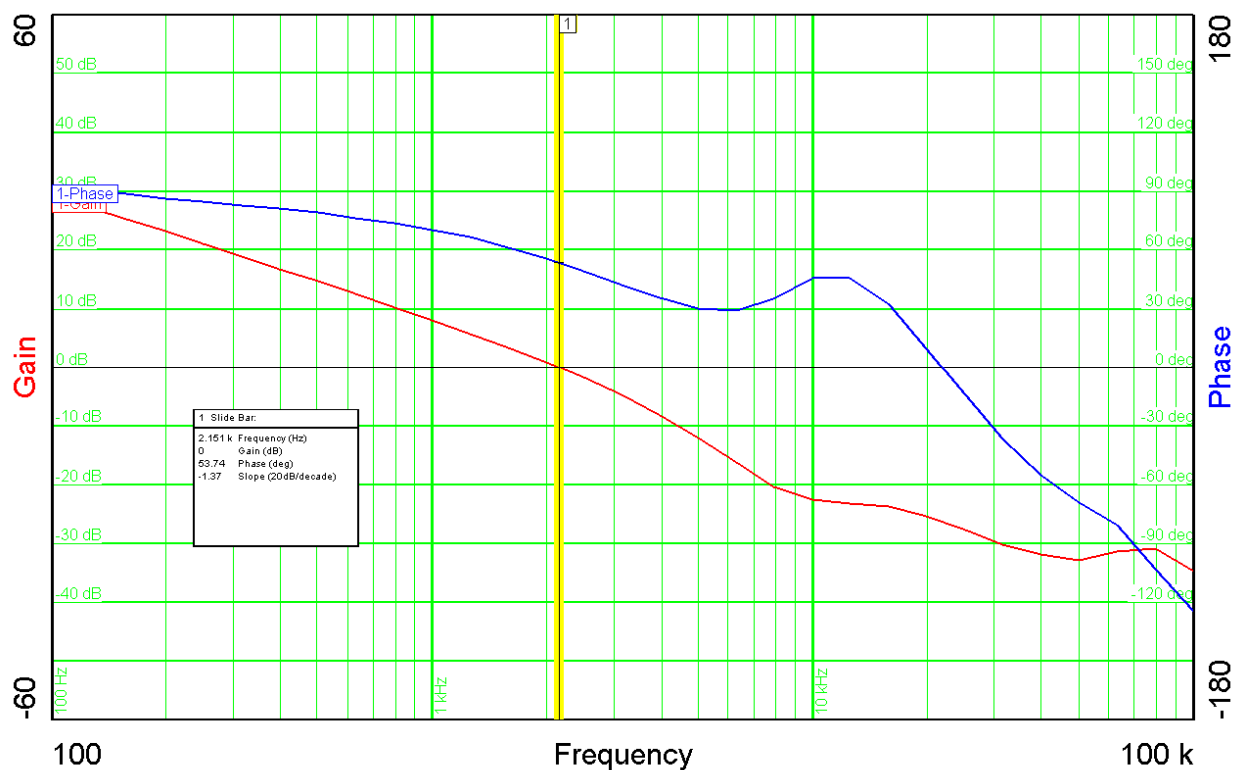
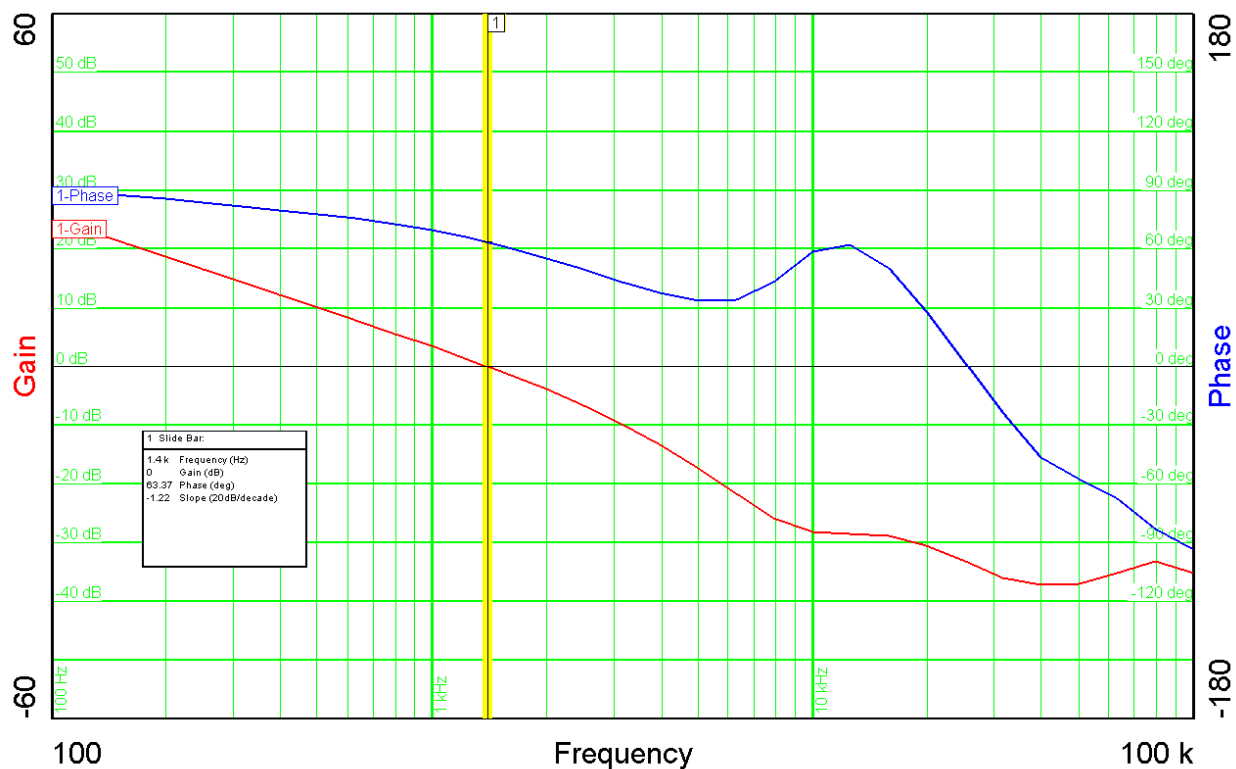


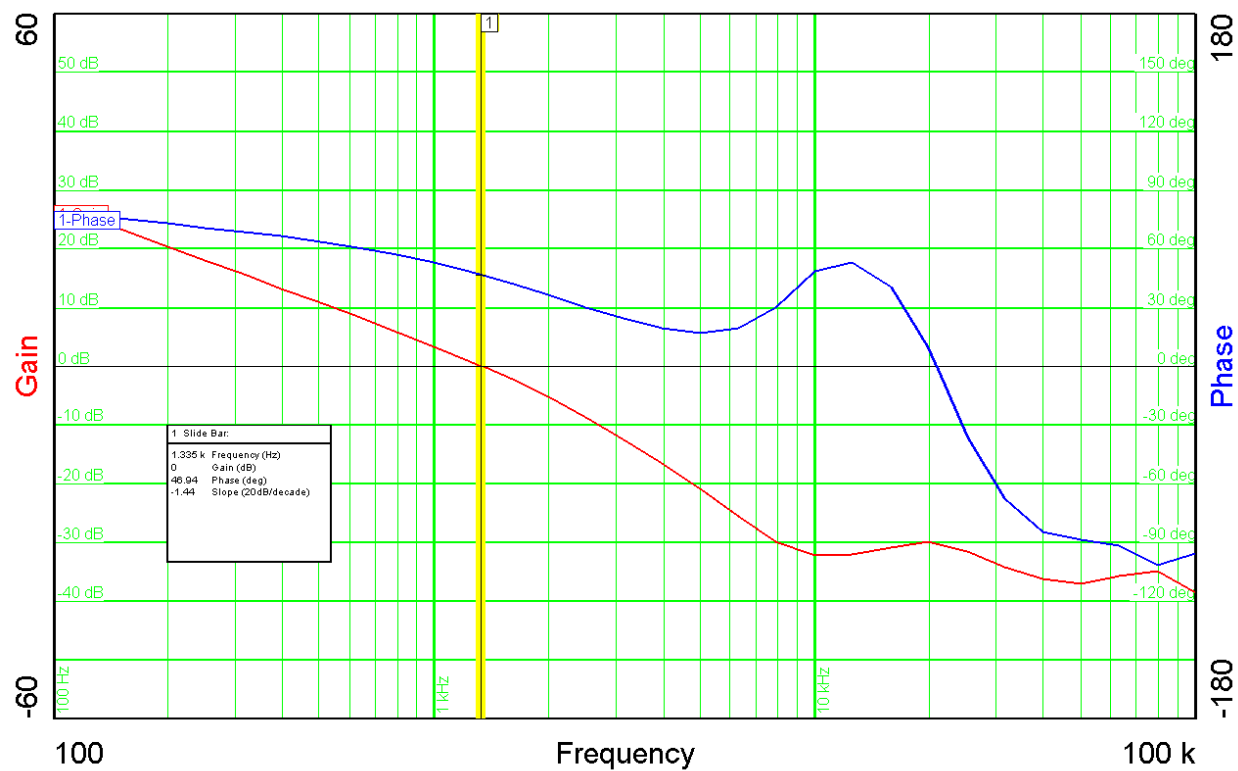
5 Loop Response

The images below show the loop response of the converter measured respectively at 22Vin, 23Vin, 24Vin and 24.5Vin.

Worst case phase margin is 47 deg. and crossover frequency 1.33KHz.







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