Table of Contents: 1.2V output

Notes:

PMP5052 is same as PMP4804 except for a few changes. See the Test Report for PMP4804 for thermal pictures and start up waveform. Operation above 20A on load needs forced air cooling.

Changes:

Stress voltages on the major semiconductors were measured here at full load and at the application input voltage extremes with a 500MHz bandwidth scope and a 500MHz bandwidth 10x probe. See pages 2-4 for waveforms. Only voltage of concern was that on drain of Q9 which exceeded its 25V rating by about 1V at maximum input voltage. The part has avalanche capability, but goal is to avoid avalanche in any steady state situation. A snubber was added across the secondary and this voltage reduced to 24V. See page 4 of this report for the “before” and “after” pictures.

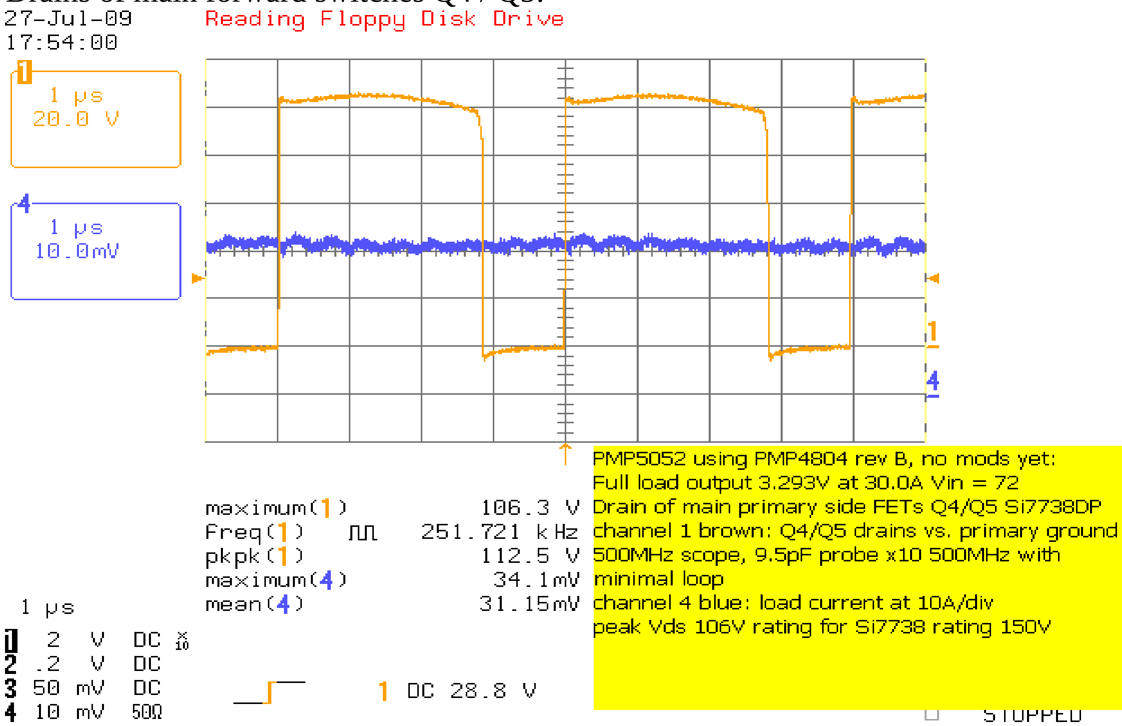
The two large 1000uF output caps were removed and replaced with two 470uF tantalum caps. In the application, the user will have about 500uF minimum cap at the load, mostly in the form of a tantalum cap. Another 470uF cap low ESR cap is needed to allow a load step or load dump of 5A to occur without the output going out of the +/-5% band around 3.3V. Hence, in the actual application one of the 470uF caps will be on the power conversion module and one at the load. The voltage loop gain was adjusted for a bandwidth of 10kHz by increasing R16 and R18 by the UCC2897 from 1k to 1.21k.

The resultant load dump response and Bode plots for the two voltage extremes are shown on pages 7 and 8 of this report. Load dumps are done instead of load steps as they can be made much more abrupt to get the worst case dynamic deviation.

Measured efficiencies in this report are about 0.7% lower than in PMP4804 Test Report. This is most likely due to current shunt variations. A 0.7% combined variation between the shunts and current meters used in the two set ups would explain this difference.

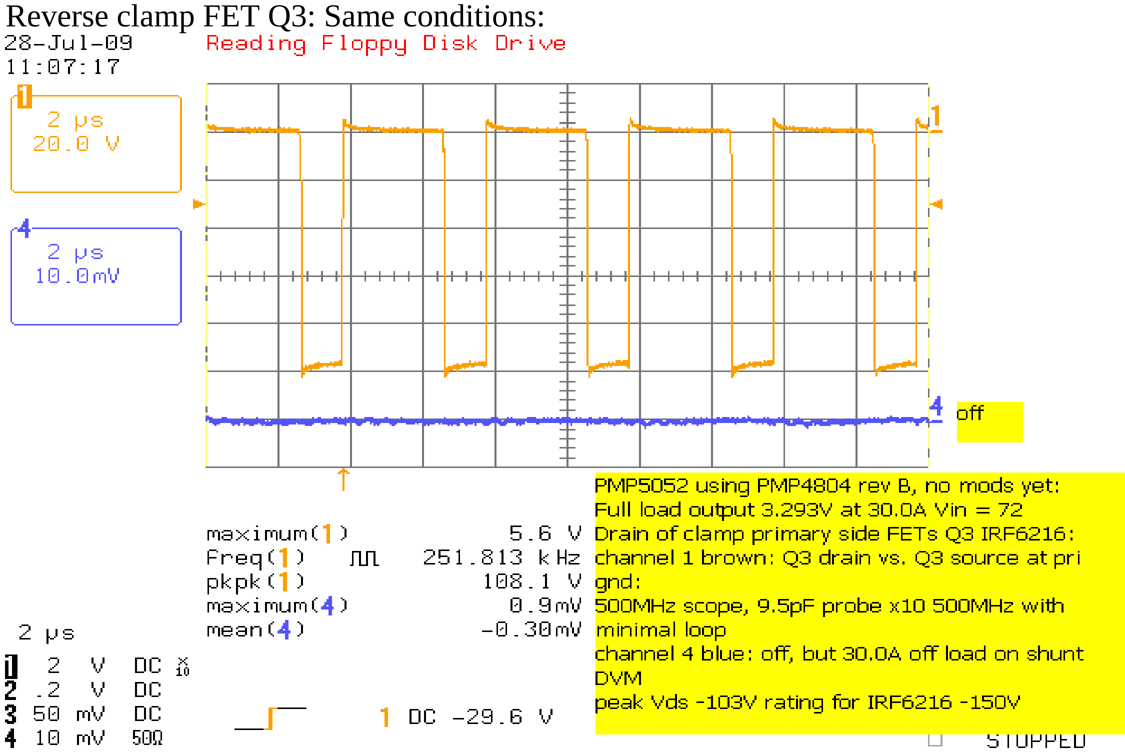
Primary side waveforms: Worst case at 72Vin: Vout: 3.293V at 30.0A

Drains of main forward switches Q4 / Q5:



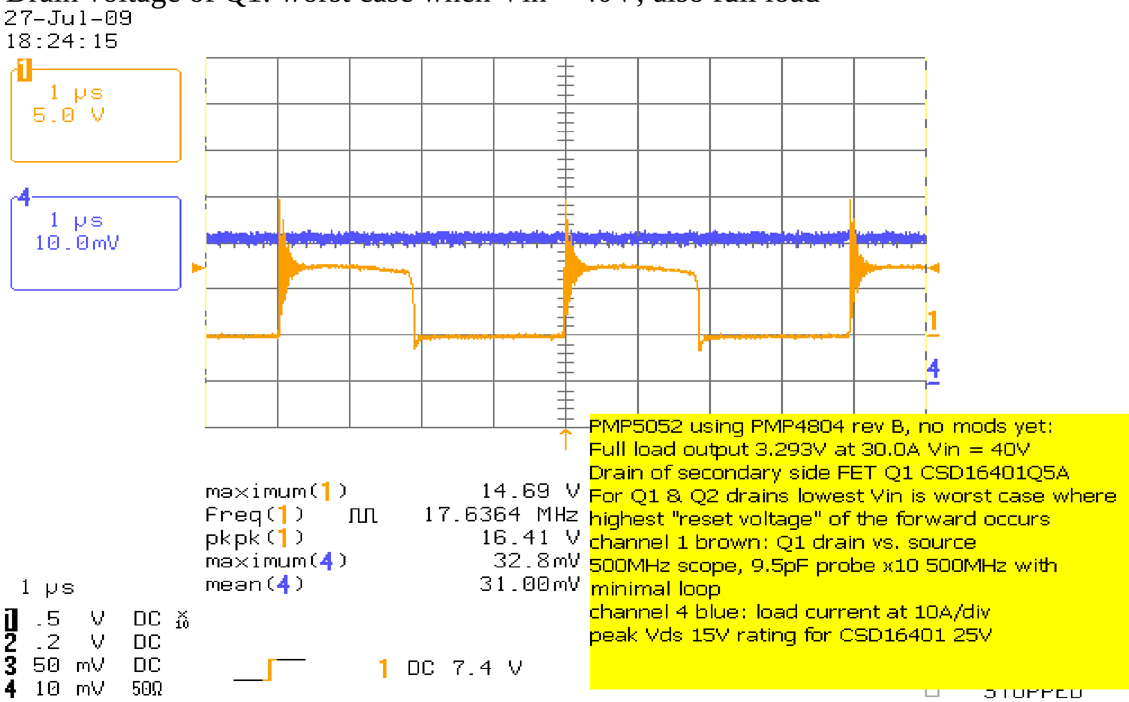
Qq

Reverse clamp FET Q3: Same conditions:

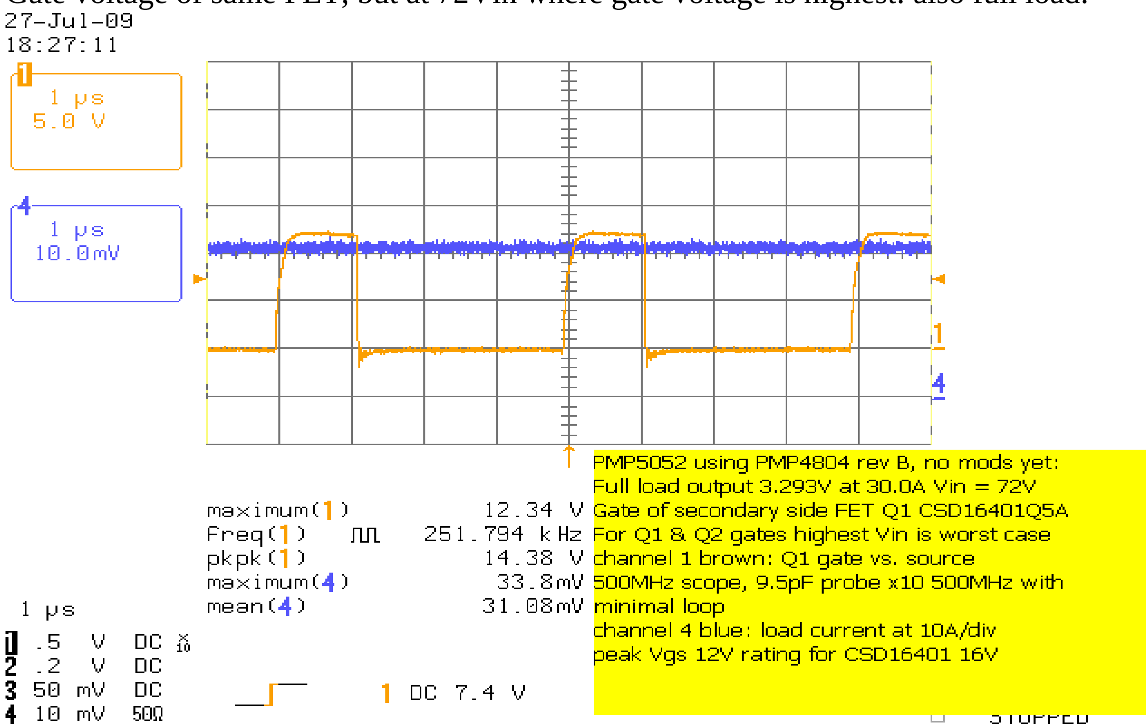


Secondary side: Q1 / Q2 for the forward path:

Drain voltage of Q1: worst case when Vin = 40V; also full load

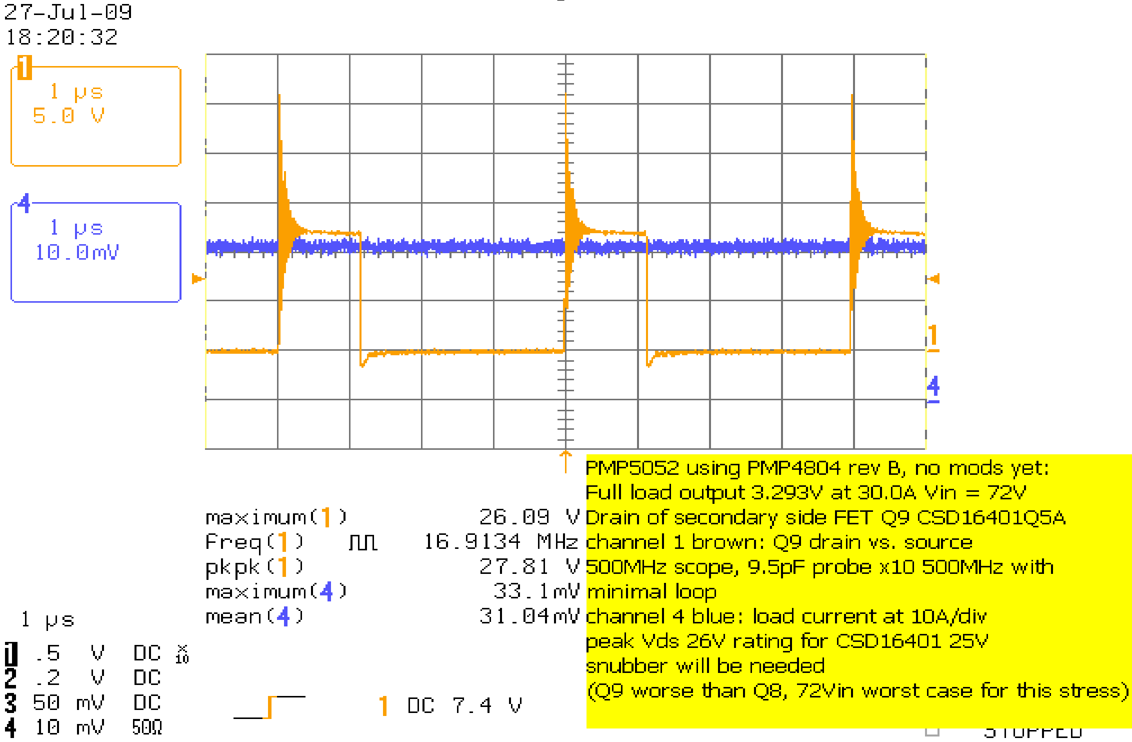


Gate voltage of same FET, but at 72Vin where gate voltage is highest: also full load:

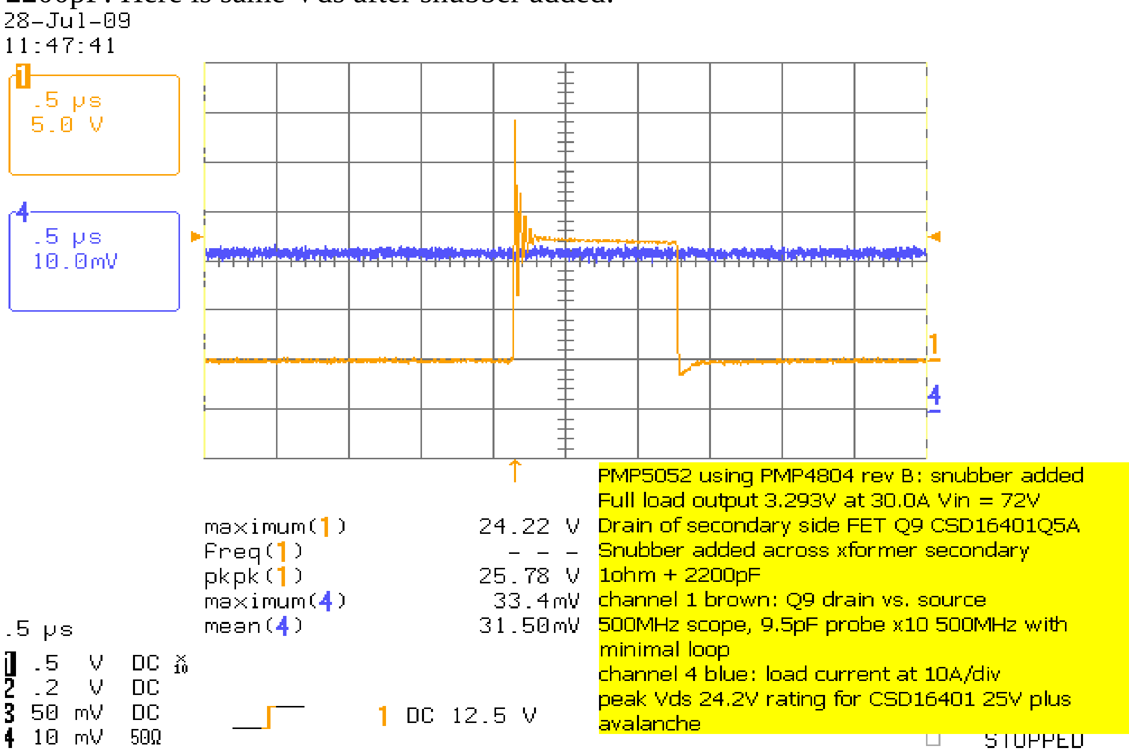


Qq

Now for the clamp Q8 and Q9: Q9 had over 1V higher drain peak than Q8 and is shown here: Worst case is 72Vin: Full load on output:



Vds too high: Need to add snubber across secondary of main transformer: 1ohm + 2200pF: Here is same Vds after snubber added:



Regulation, losses and efficiency: 40Vin, 48Vin and 72Vin with external airflow:

Vin Volts	Iin A	Vout1 Volts	Iout1 A	Losses in W	Efficiency %
72.0	1.4795	3.291	30.0	7.794	92.7
72.0	1.233	3.294	25.0	6.426	92.8
72.0	0.9895	3.296	20.0	5.324	92.5
72.0	0.7495	3.299	15.0	4.479	91.7
72.1	0.515	3.301	10.0	4.121	88.9
72.0	0.283	3.303	5.0	3.861	81.1
72.0	0.168	3.305	2.5	3.834	68.3
72.0	0.058	3.306	0	4.176	
48.05	2.205	3.291	30.0	7.220	93.2
48.01	1.835	3.2935	25.0	5.761	93.5
48.01	1.4705	3.296	20.0	4.679	93.4
48.00	1.1105	3.298	15.0	3.834	92.8
48.02	0.757	3.301	10.0	3.341	90.8
48.03	0.4085	3.303	5.0	3.105	84.2
48.00	0.237	3.304	2.5	3.116	72.6
48.01	0.0675	3.305	0	3.241	
39.98	2.649	3.291	30.0	7.177	93.2
40.03	2.200	3.293	25.0	5.741	93.5
39.98	1.764	3.296	20.0	4.605	93.5
40.03	1.329	3.298	15.0	3.730	93.0
40.00	0.906	3.300	10.0	3.240	91.1
40.04	0.487	3.303	5.0	2.984	84.7
39.94	0.282	3.304	2.5	3.003	73.3
39.97	0.0775	3.305	0	3.098	

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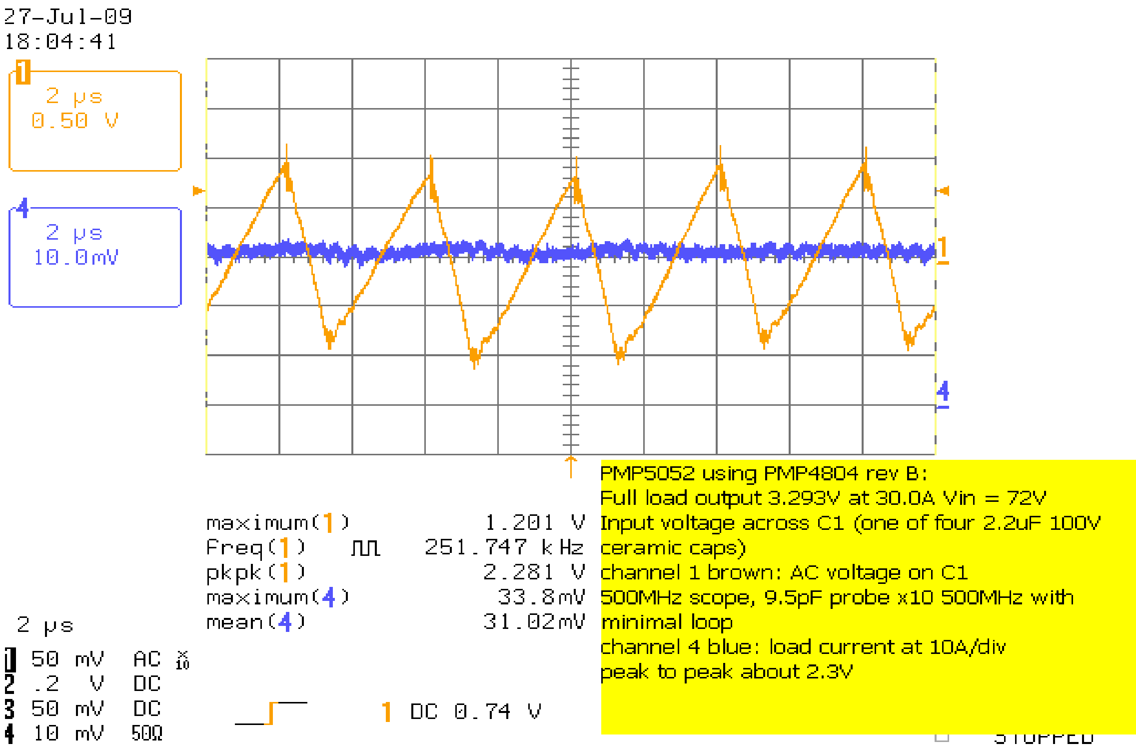
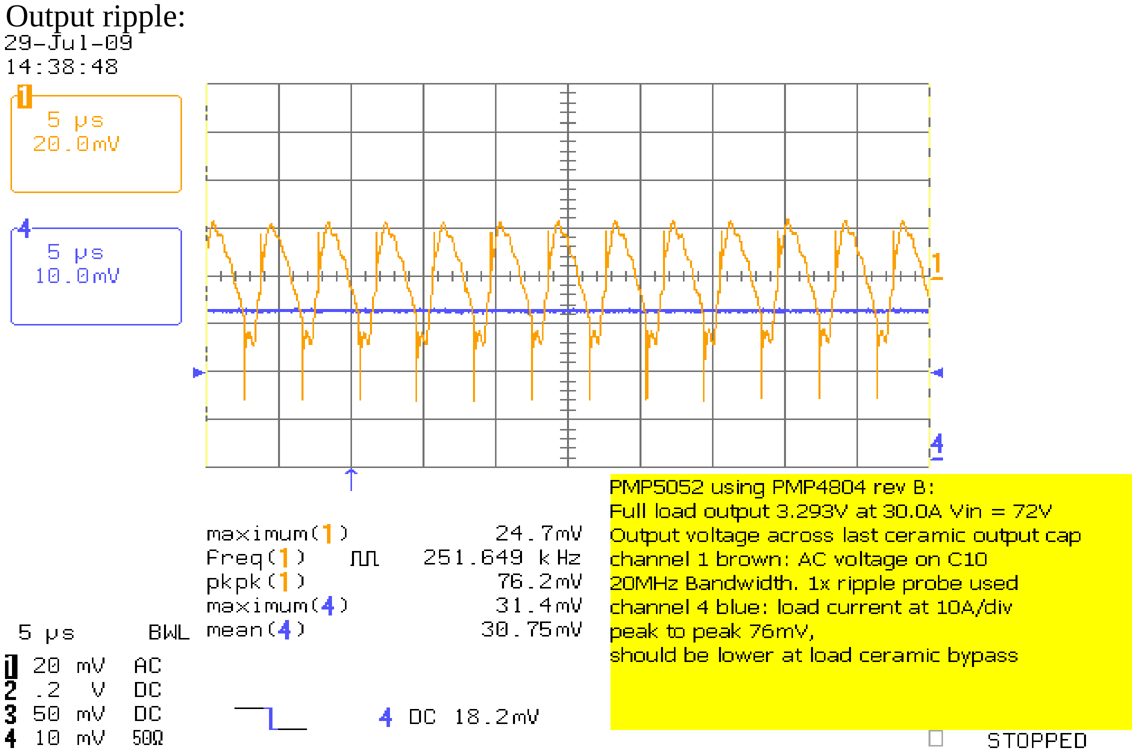
Input ripple:

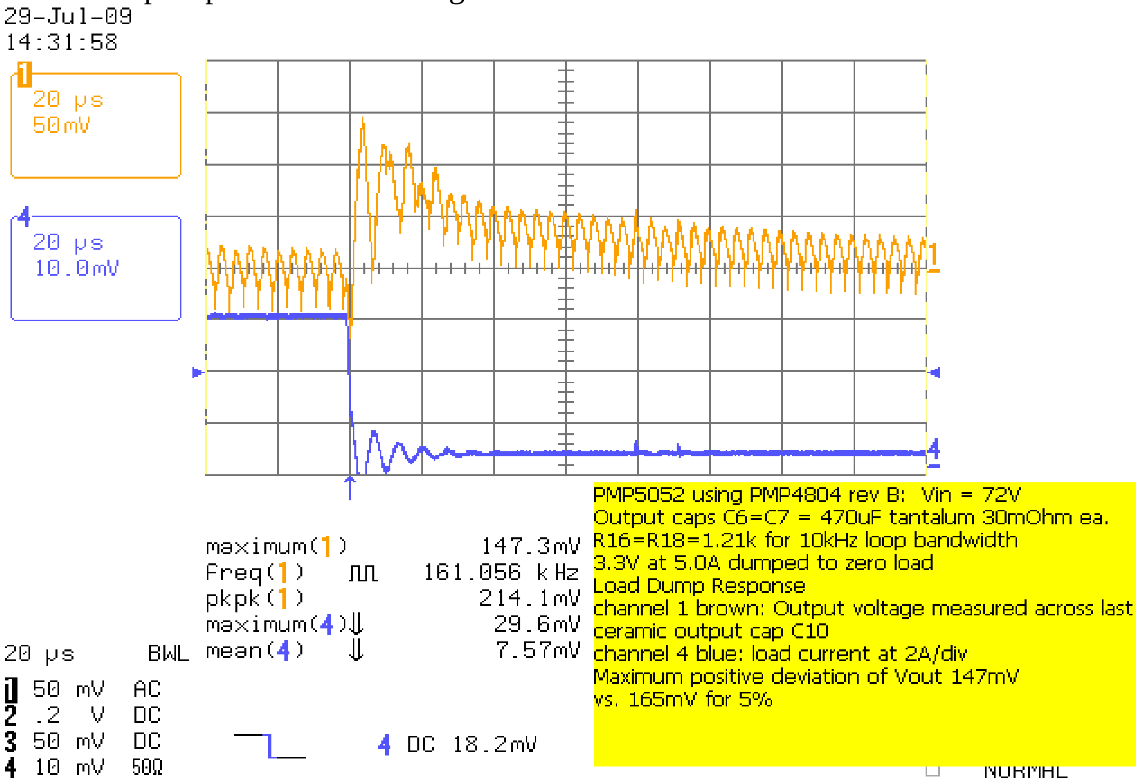


Q

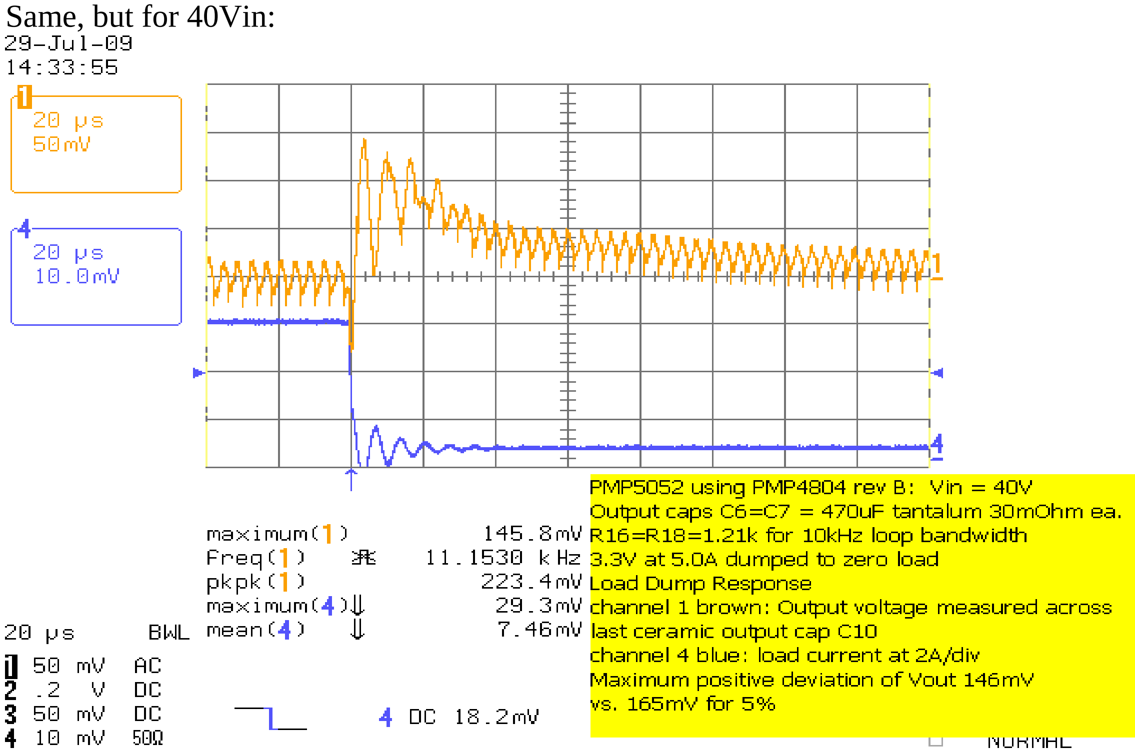
Output ripple:



Load dump response: 72Vin Going from 5A to zero A:

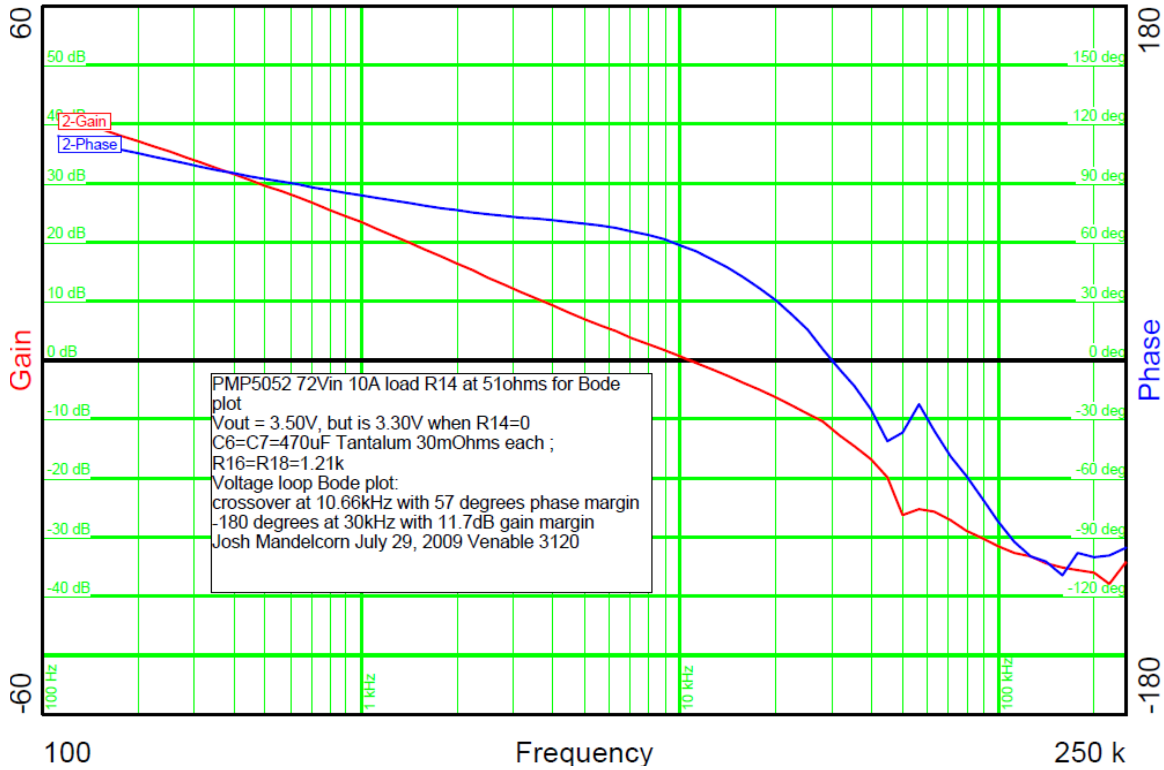


Same, but for 40Vin:



Qq

Bode Plots: First at 72Vin



Then at 40Vin: