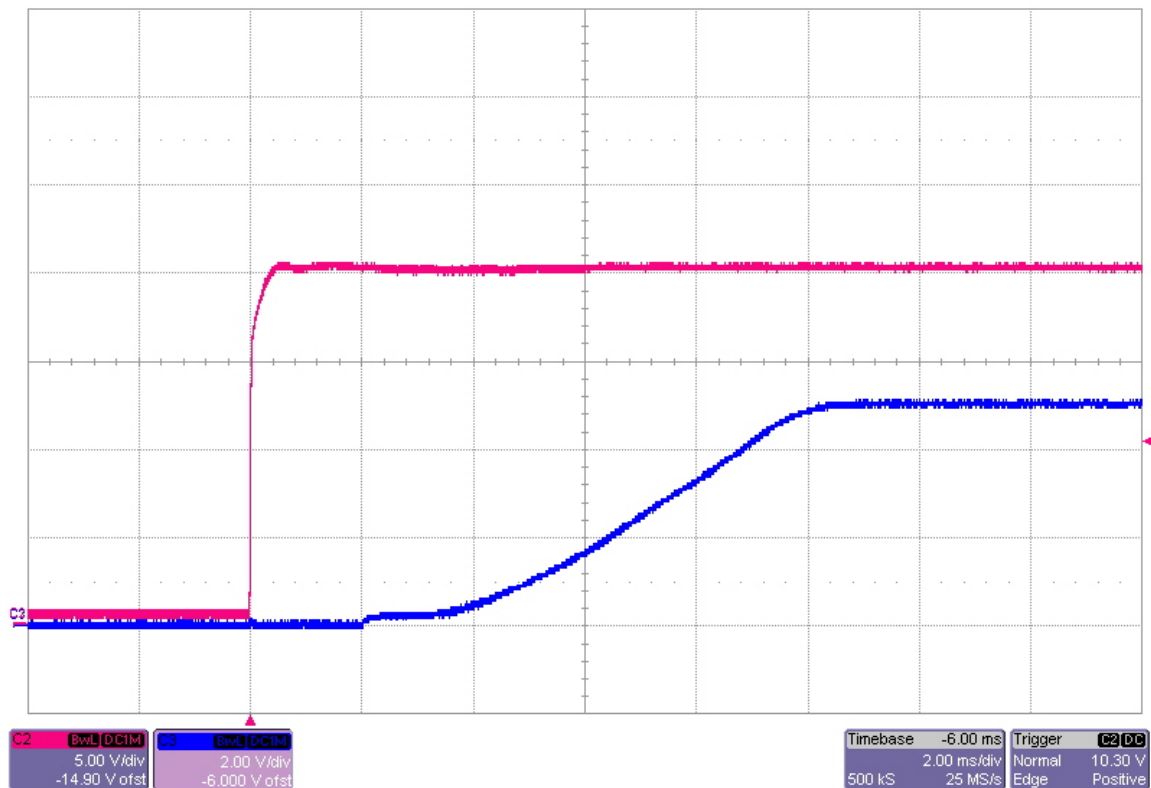


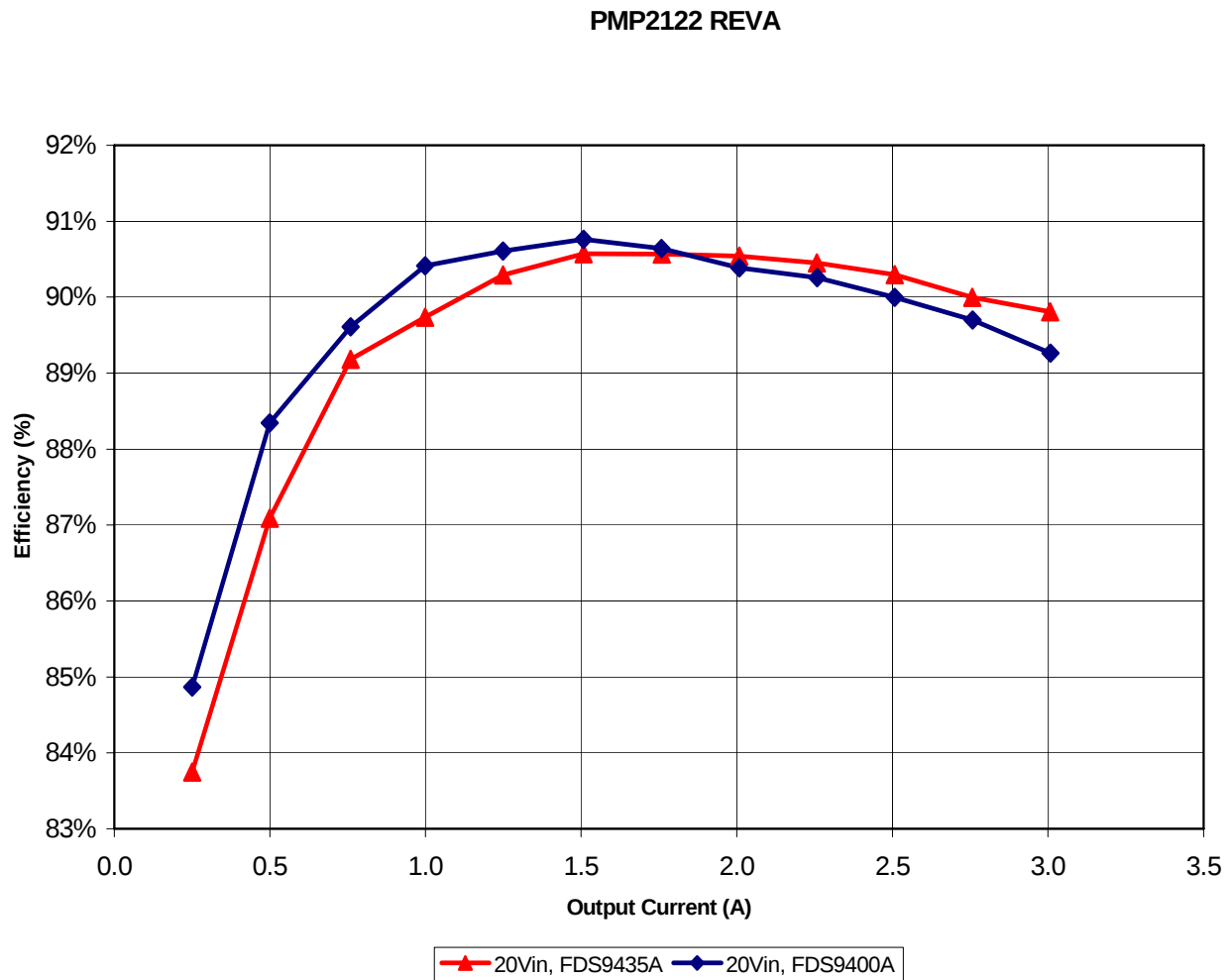
1 Startup

The photo below shows the 5V output voltage startup waveforms after the application of 20Vdc in. The output was loaded to 0A. (Vin is 5V/DIV, Vout is 2V/DIV, 2mS/DIV)



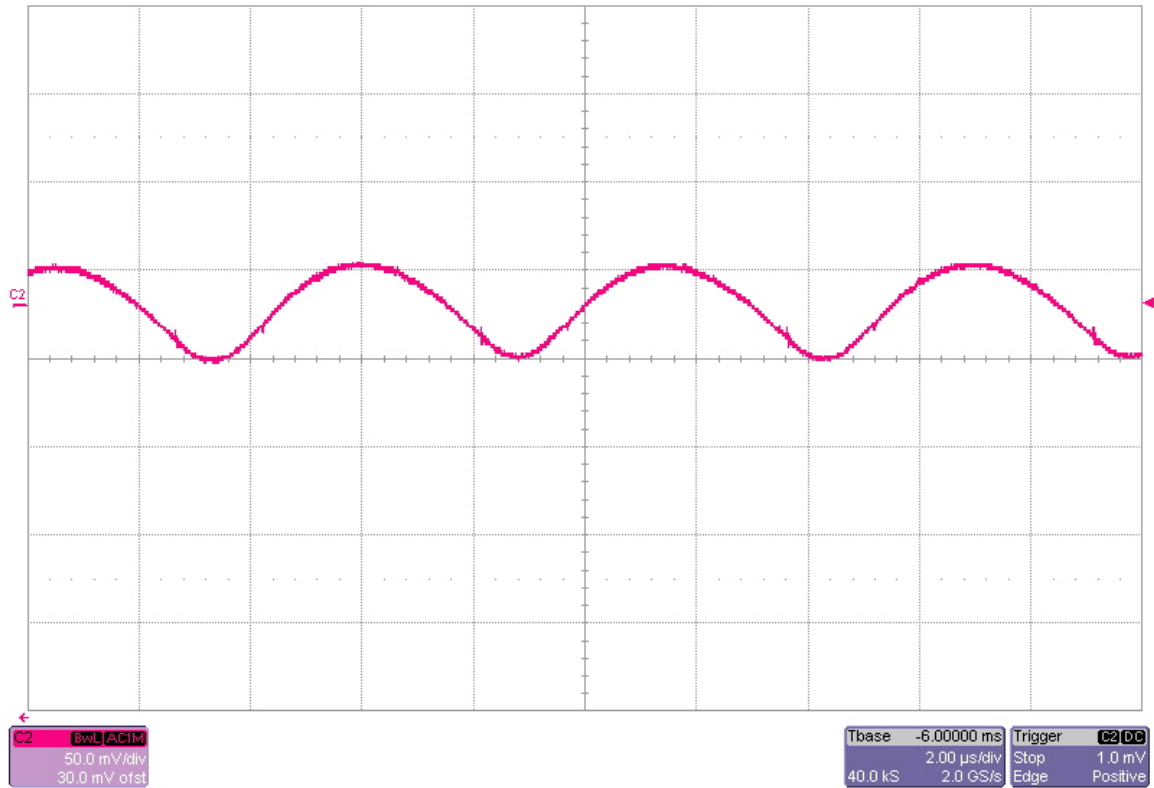
2 Efficiency

The 5V converter efficiency is shown in the figure below.



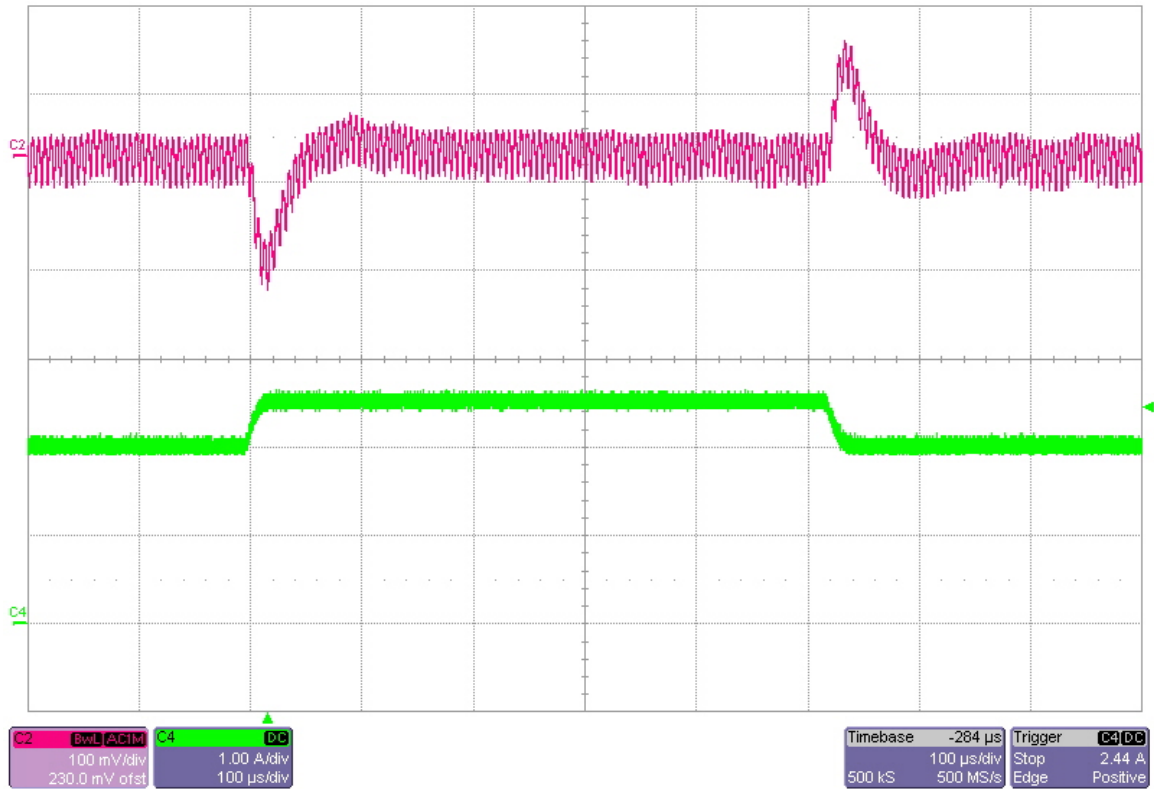
3 Output Ripple Voltage

The 5V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 3A and the input voltage set to 20Vdc. (50mV/DIV, 2uS/DIV)



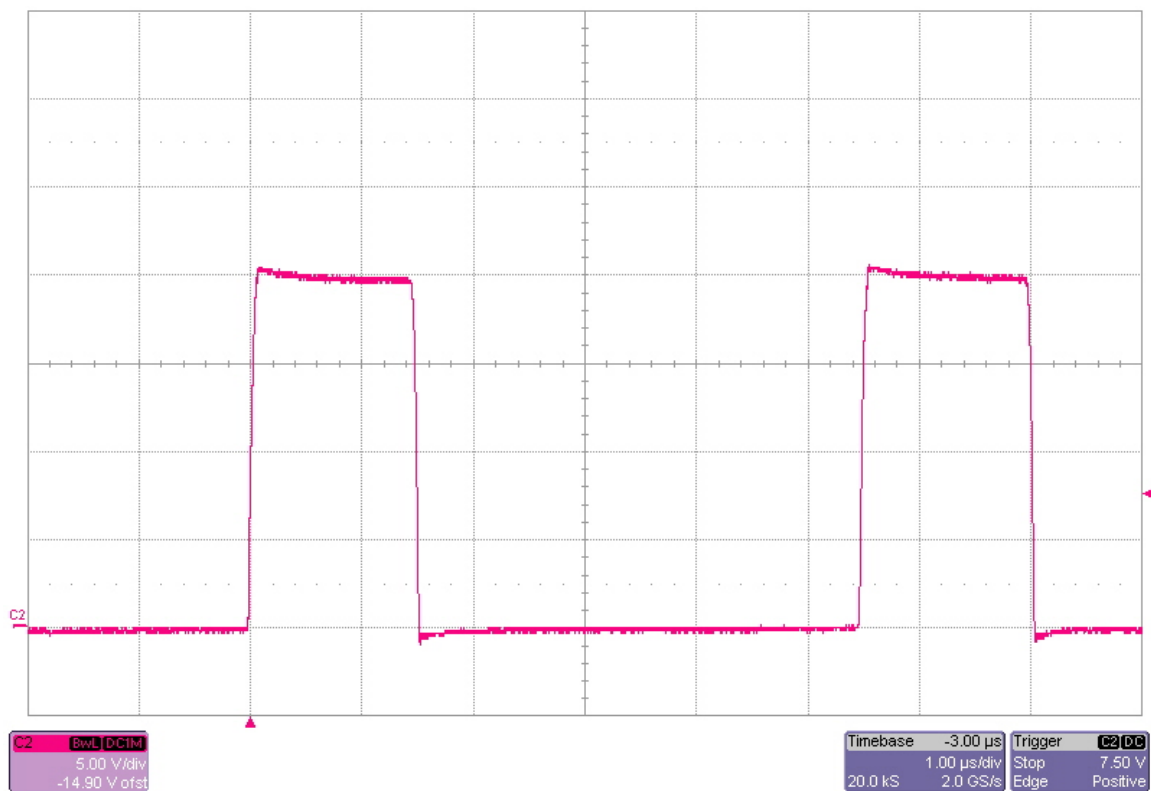
4 Load Transients

The photo below shows the 5V output voltage when the load current is stepped between 2A and 2.5A.
 $V_{in} = 20V_{dc}$. (100mV/DIV, 1A/DIV, 100uS/DIV)



5 Switch Node Waveforms

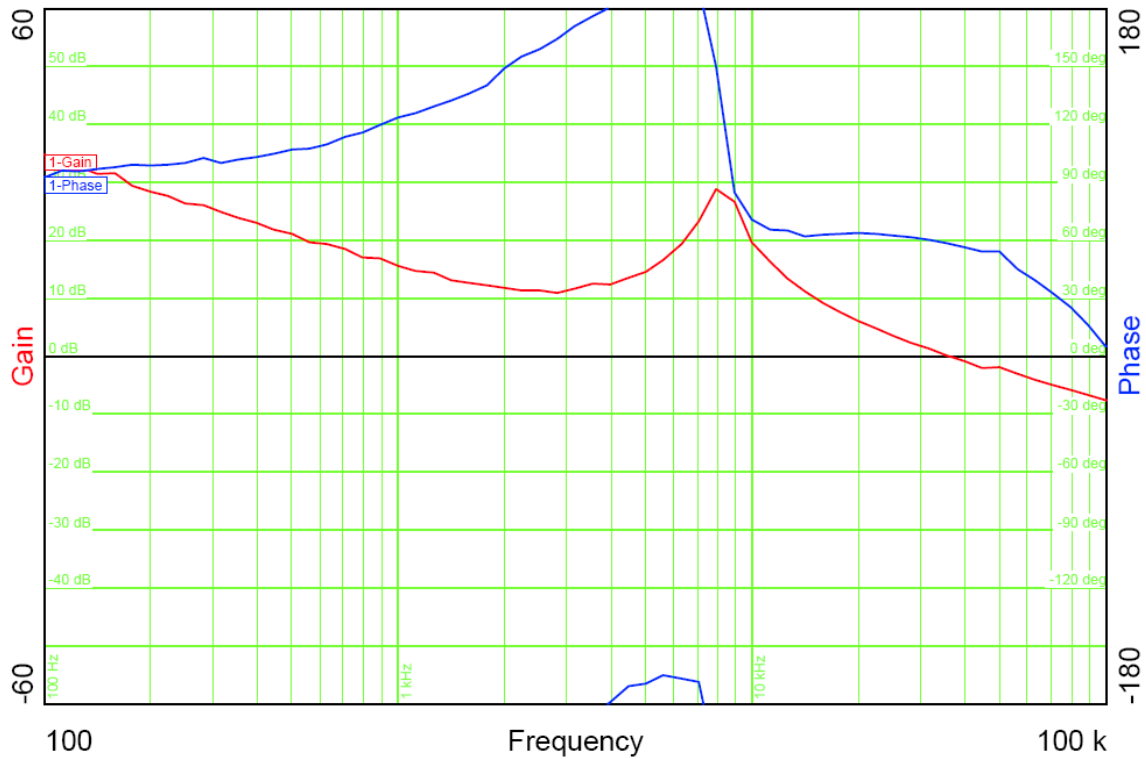
The photo below is of the drain voltage (switch node) for FET Q1. The input voltage is 20V and the output is loaded to 3A. (5V/DIV, 1 μ S/DIV)



6 Control Loop Gain / Stability

The plot below shows the 5V loop gain and phase margin with the input voltage set to 20V and the output loaded to 3A.

Band Width = 35KHz, Phase Margin = 59 degrees



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