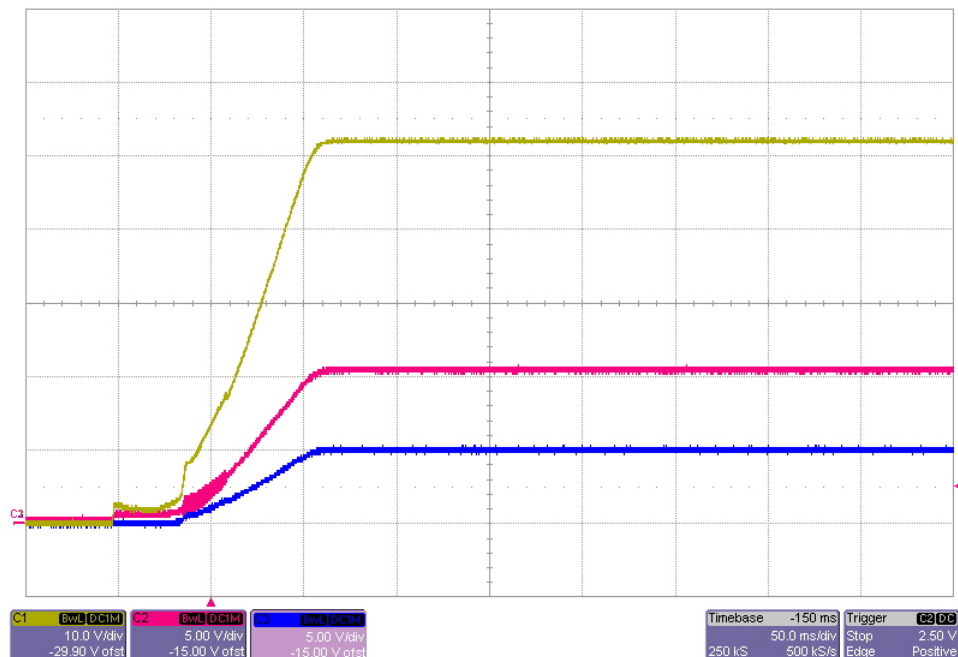


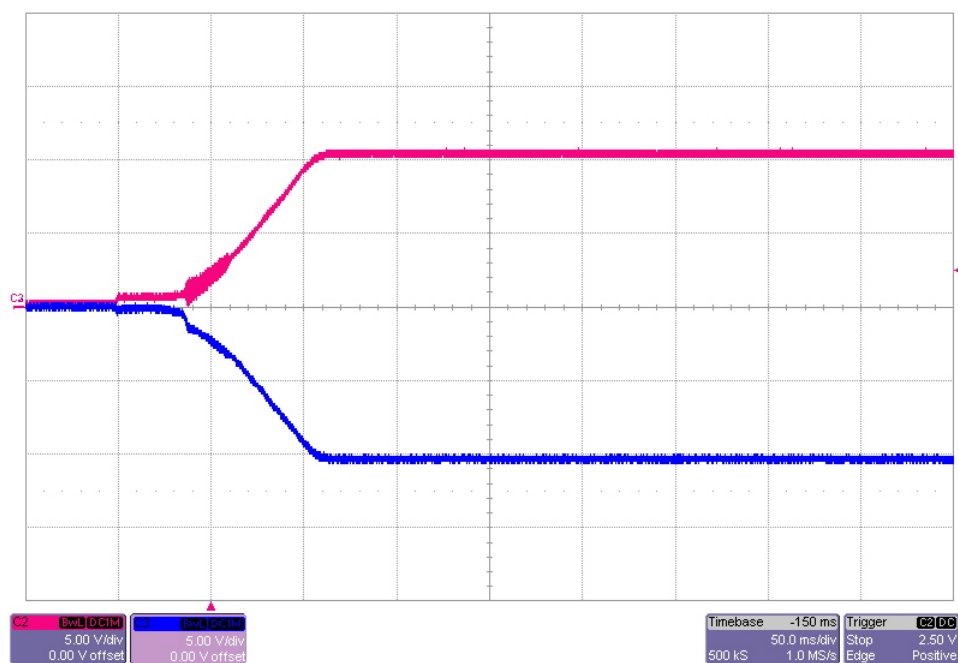
1 Startup

The photo below shows the 5V, +10V and 50V output voltage startup waveforms after the application of 12Vdc in. The outputs were loaded to max.

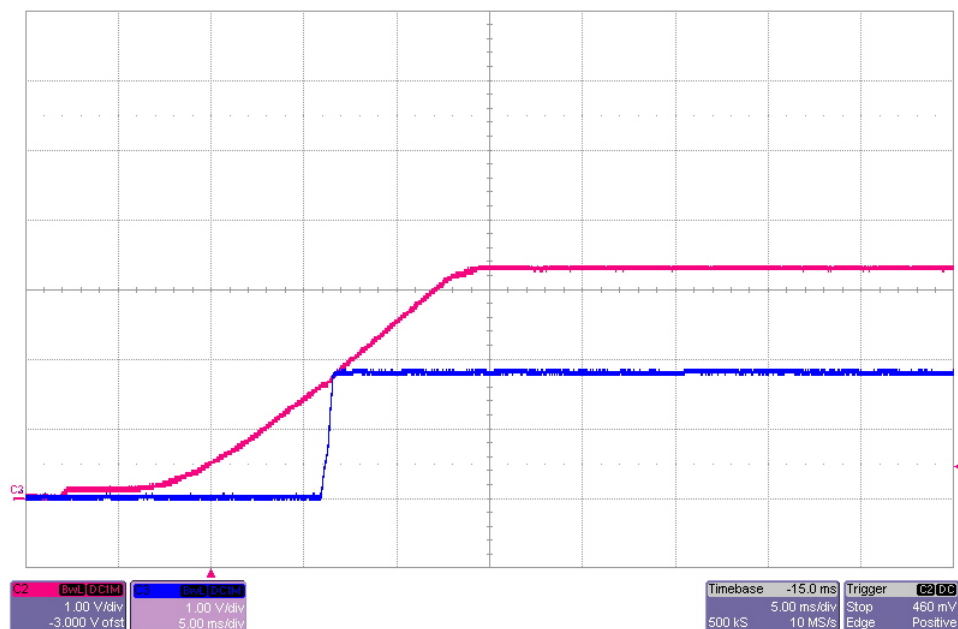
(5V/DIV (5V and +10V outputs), 10V/DIV (50V output), 50mS/DIV)



The photo below shows the +10V and -10V output voltage startup waveforms after the application of 12Vdc in. The outputs were loaded to max. (5V/DIV, 50mS/DIV)

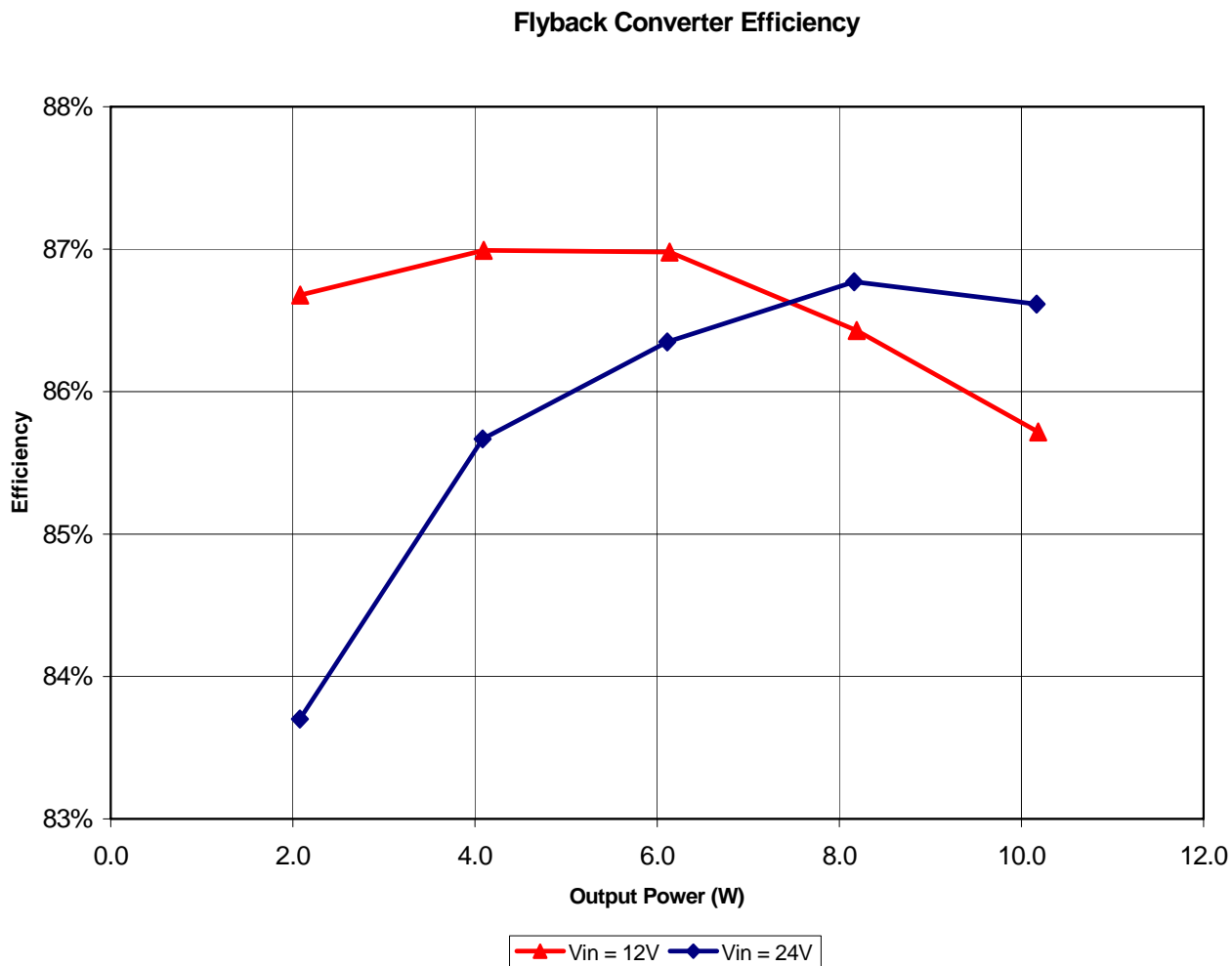


The photo below shows the 3.3V and 1.8V output voltage startup waveforms after the application of 12Vdc in. The outputs were loaded to 0A. (1V/DIV, 5mS/DIV)



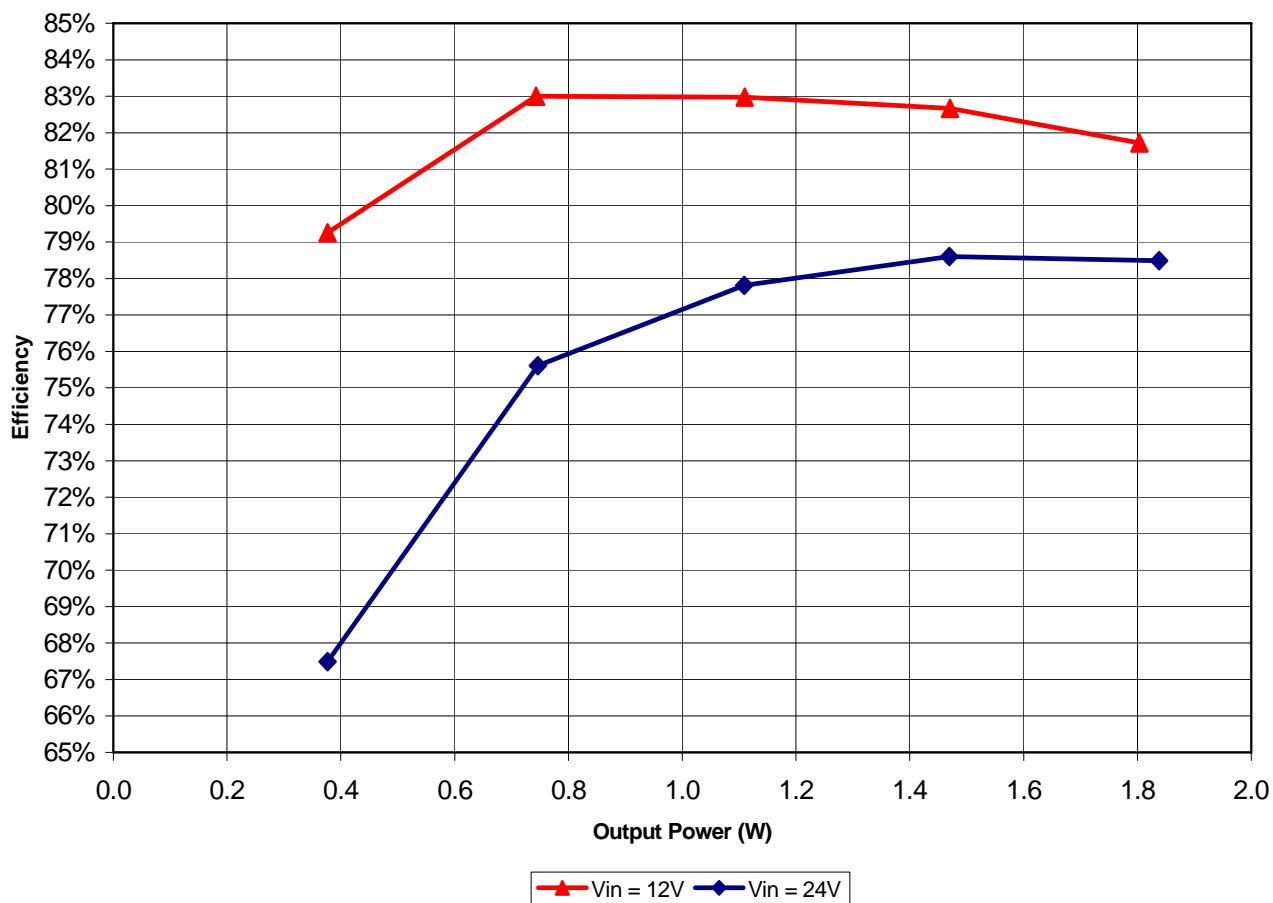
2 Efficiency

The flyback Converter efficiency is shown in the figure below. All output voltages are loaded proportionally. The 3.3V/1.8V converter is disabled.



The 3.3V and 1.8V converter efficiency is shown in the figure below. All output voltages are loaded proportionally. The flyback converter is disabled.

3.3V and 1.8V Buck Converter Combined Efficiency



Cross Load Regulation Data (Flyback Converter)

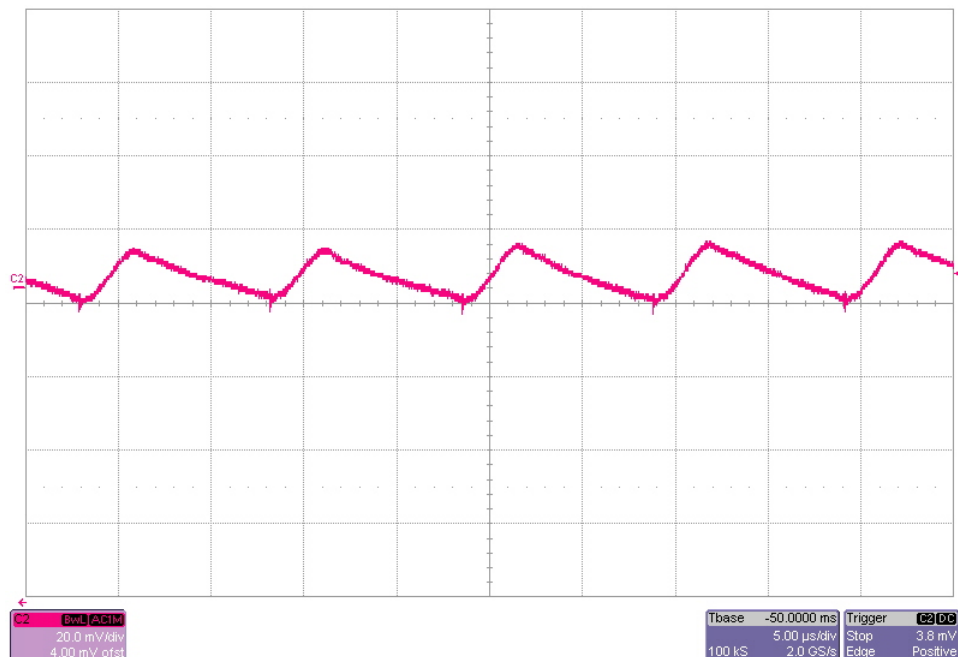
Vin = 12.2V							
+10V	+10V I	-10V	-10V I	5V	5V I	50V	50V I
10.252V	0.044A	-10.39V	0.043A	4.912V	0.149A	51.4V	0.021A
10.253V	0.044A	-10.31V	0.044A	4.988V	0.030A	51.3V	0.021A
10.255V	0.044A	-10.26V	0.044A	4.899V	0.149A	51.8V	0.004A
10.252V	0.044A	-10.24V	0.044A	5.285V	Open	52.1V	Open
10.253V	0.403A	-10.35V	0.403A	5.049V	0.153A	52.6V	0.021A
10.254V	0.403A	-10.33V	0.403A	5.112V	0.031A	52.6V	0.021A
10.254V	0.403A	-10.35V	0.403A	5.054V	0.153A	52.9V	0.004A
10.255V	0.403A	-10.33V	0.403A	5.367V	Open	53.4V	Open
10.255V	0.403A	-11.09V	0.045A	5.060V	0.153A	53.0V	0.021A
10.254V	0.044A	-9.99V	0.405A	4.995V	0.030A	51.5V	0.004A

Balanced Loading Regulation Data (Flyback Converter)

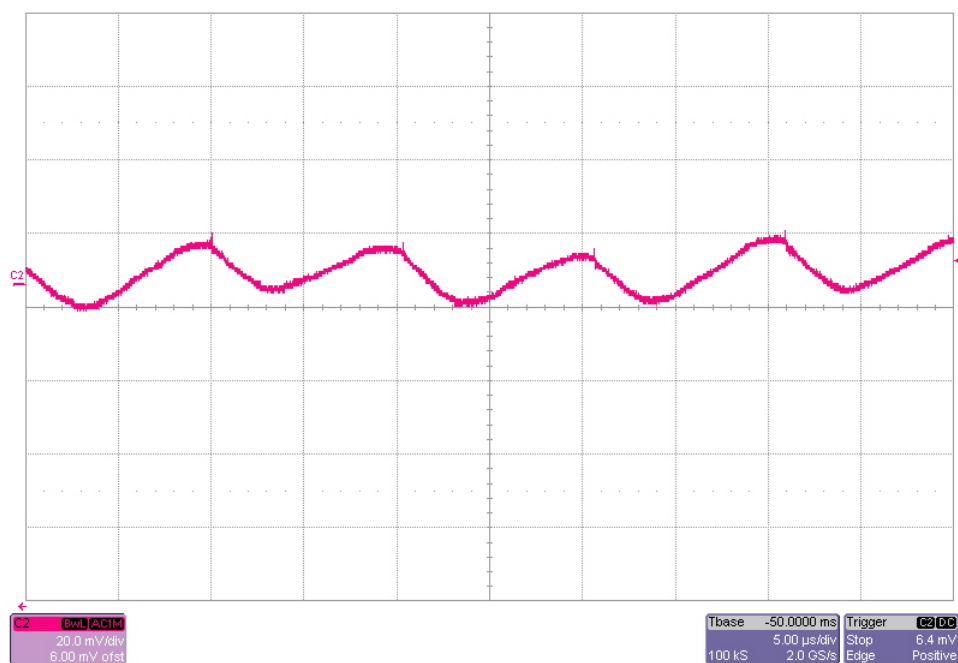
Vin = 12V								
Vout1	Iout1	Vout2	Iout2	Vout3	Iout3	Vout4	Iout4	Po
10.252	0.084	-10.29	0.083	5.012	0.030	51.9	0.0042	2.081
10.252	0.163	-10.32	0.164	5.018	0.060	52.1	0.0083	4.096
10.253	0.244	-10.33	0.244	5.028	0.091	52.3	0.0126	6.138
10.253	0.323	-10.34	0.328	5.040	0.120	52.5	0.0168	8.190
10.254	0.403	-10.35	0.403	5.052	0.153	52.6	0.021	10.184

3 Output Ripple Voltage

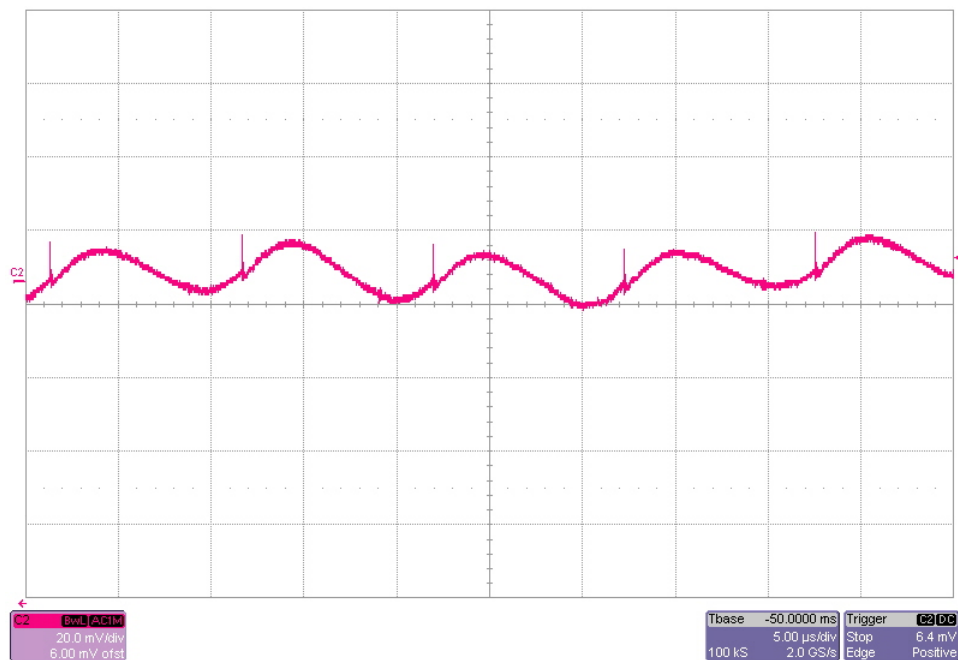
The 5V output ripple voltage is shown in the figure below. The image was taken with all outputs loaded to max and the input voltage set to 12Vdc. (20mV/DIV, 5uS/DIV)



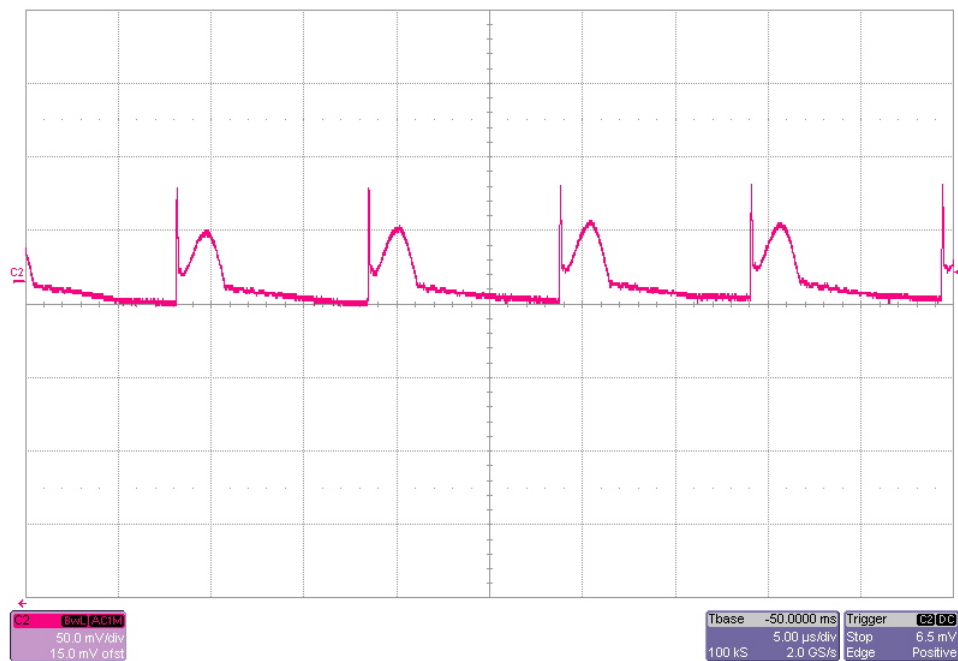
The +10V output ripple voltage is shown in the figure below. The image was taken with all outputs loaded to max and the input voltage set to 12Vdc. (20mV/DIV, 5uS/DIV)



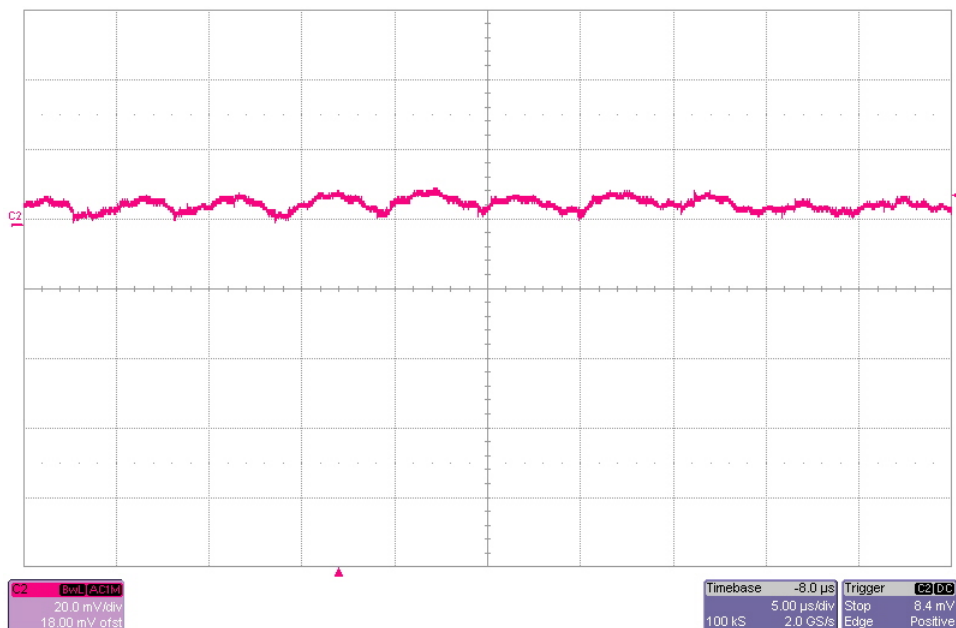
The -10V output ripple voltage is shown in the figure below. The image was taken with all outputs loaded to max and the input voltage set to 12Vdc. (20mV/DIV, 5uS/DIV)



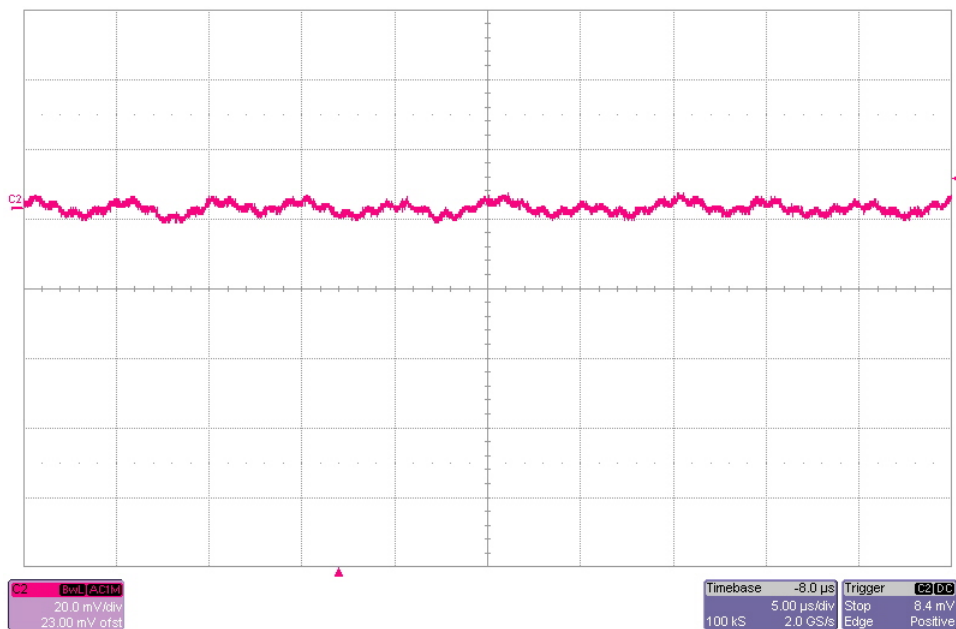
The 50V output ripple voltage is shown in the figure below. The image was taken with all outputs loaded to max and the input voltage set to 12Vdc. (50mV/DIV, 5uS/DIV)



The 3.3V output ripple voltage is shown in the figure below. The image was taken with the 3.3V and the 1.8V outputs loaded to max. The input voltage was set to 30Vdc. (20mV/DIV, 5uS/DIV)

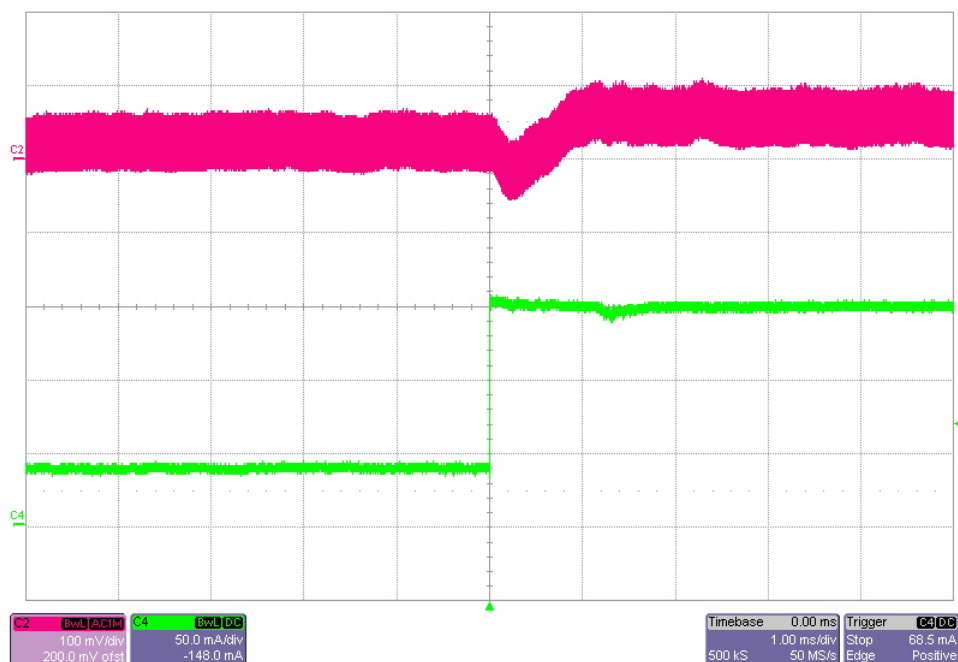


The 1.8V output ripple voltage is shown in the figure below. The image was taken with the 3.3V and the 1.8V outputs loaded to max. The input voltage was set to 30Vdc. (20mV/DIV, 5uS/DIV)

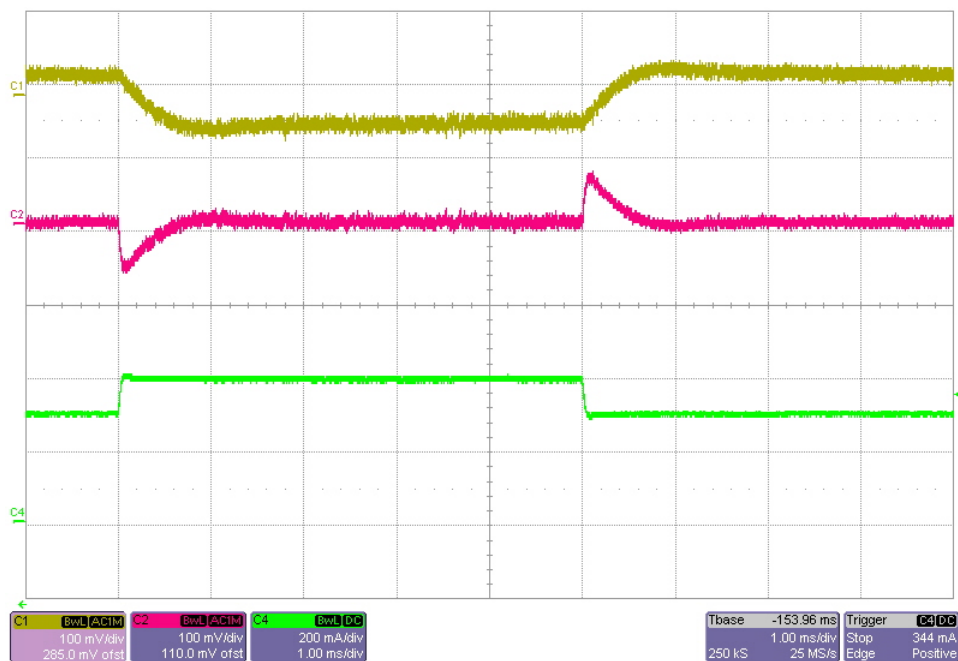


4 Load Transients

The photo below shows the 5V output voltage when the load current is stepped between 40mA and 150mA. $V_{in} = 12V_{dc}$. (100mV/DIV, 50mA/DIV, 1mS/DIV)

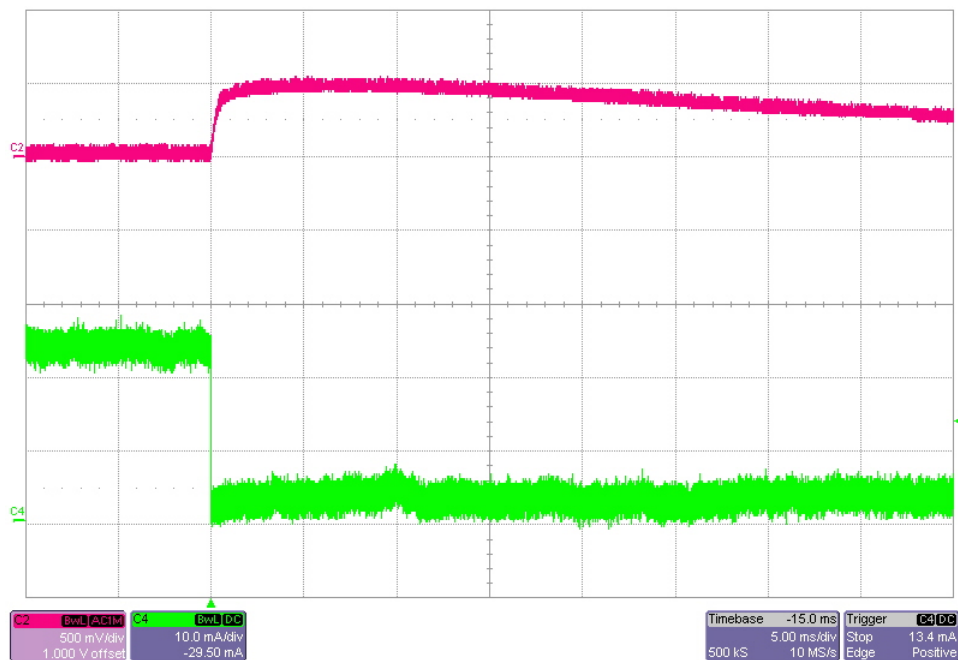


The photo below shows the +10V and -10V output voltage when the +10V load current is stepped between 300mA and 400mA. $V_{in} = 12V_{dc}$. (100mV/DIV, 200mA/DIV, 1mS/DIV)

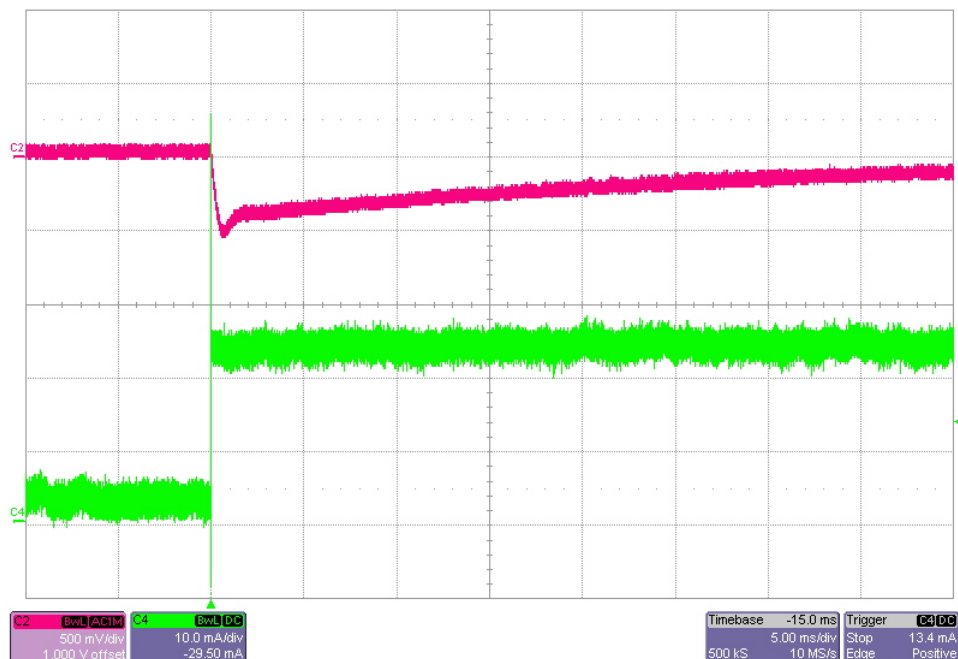


PMP3004 REVB Test Results

The photo below shows the 50V output voltage when the load current is stepped between 20mA and 0mA.
 $V_{in} = 12V_{dc}$. (500mV/DIV, 10mA/DIV, 5mS/DIV)



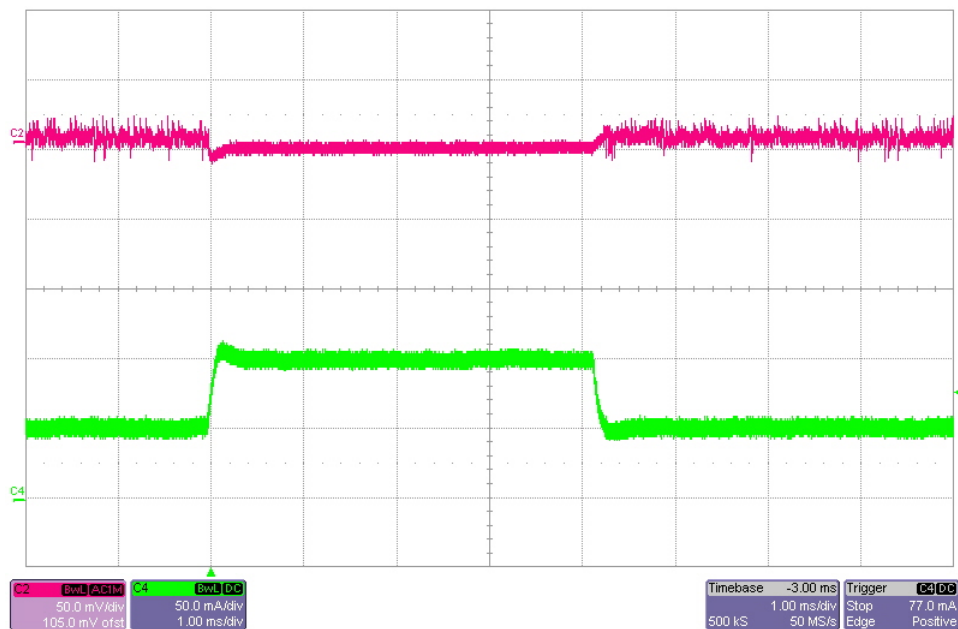
The photo below shows the 50V output voltage when the load current is stepped between 0mA and 20mA.
 $V_{in} = 12V_{dc}$. (500mV/DIV, 10mA/DIV, 5mS/DIV)



The photo below shows the 3.3V output voltage when the load current is stepped between 240mA and 360mA. $V_{in} = 12V_{dc}$. (100mV/DIV, 200mA/DIV, 1mS/DIV)

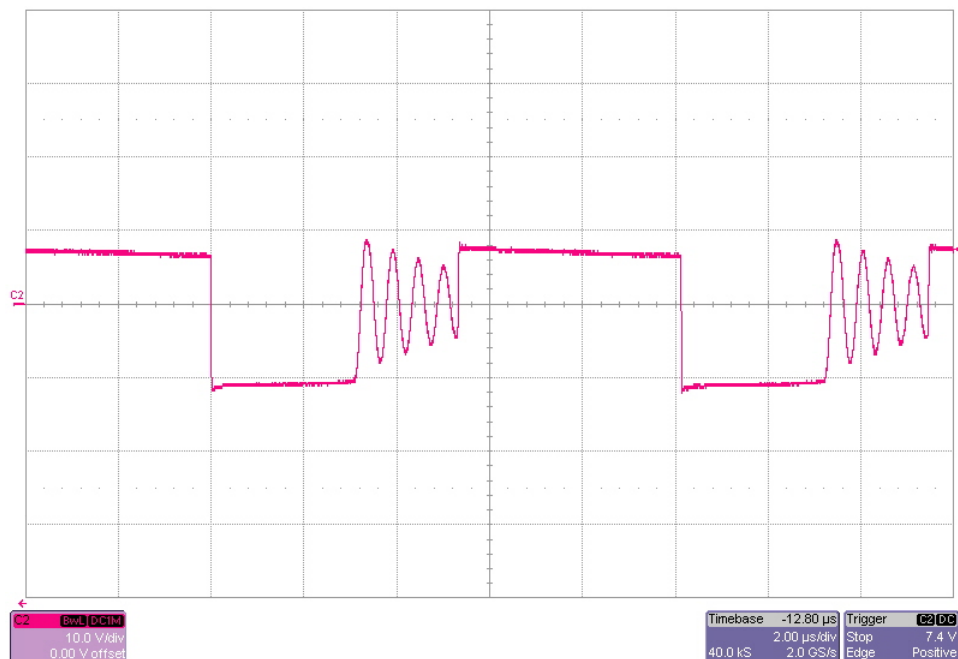


The photo below shows the 1.83V output voltage when the load current is stepped between 50mA and 100mA. $V_{in} = 12V_{dc}$. (50mV/DIV, 50mA/DIV, 1mS/DIV)

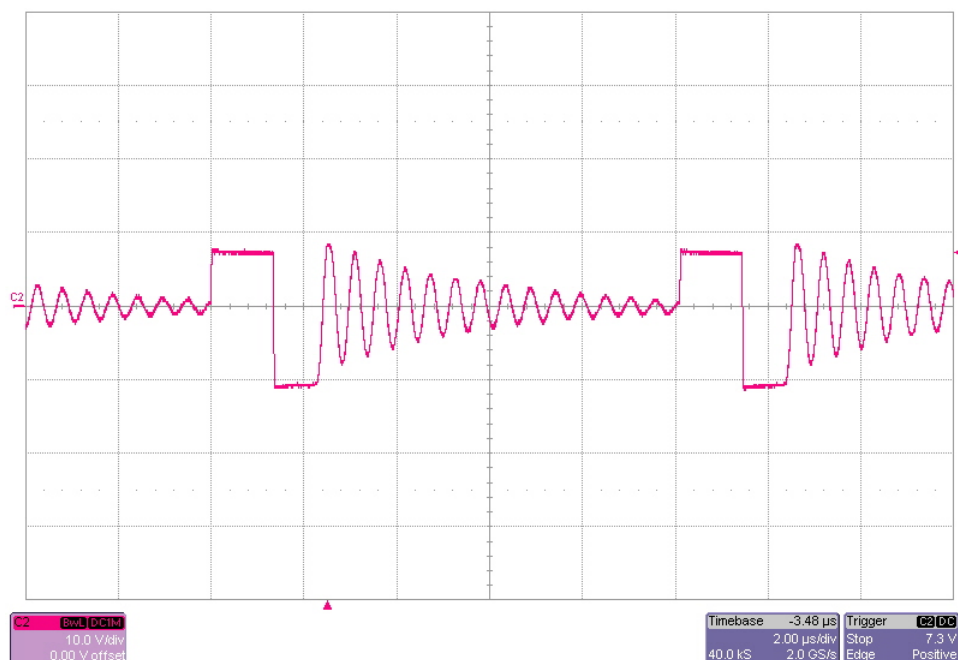


5 Switch Node Waveforms

The photo below is of FET Q1 switch node (TP4). The input voltage is 7.5V and the outputs are loaded to max. (10V/DIV, 2uS/DIV)

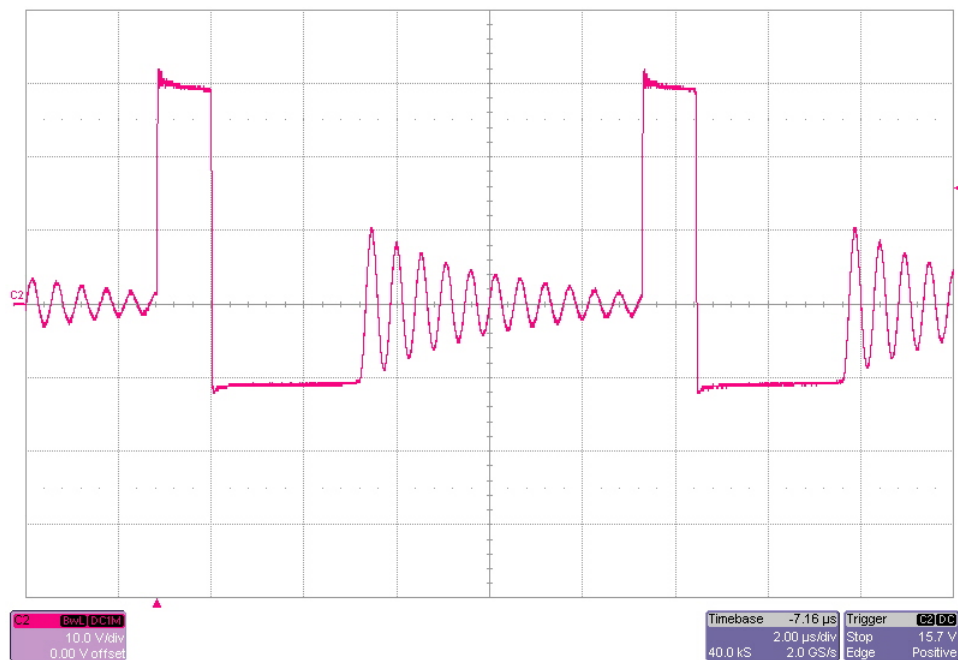


The photo below is of FET Q1 switch node (TP4). The input voltage is 7.5V and the outputs are loaded to min (20% of max load). (10V/DIV, 2uS/DIV)

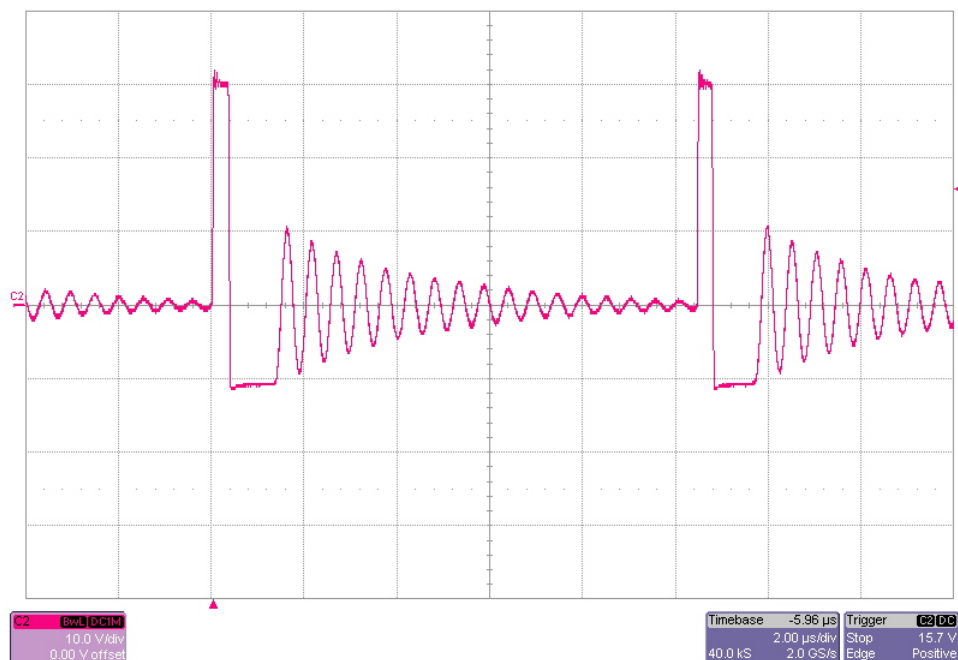


PMP3004 REVB Test Results

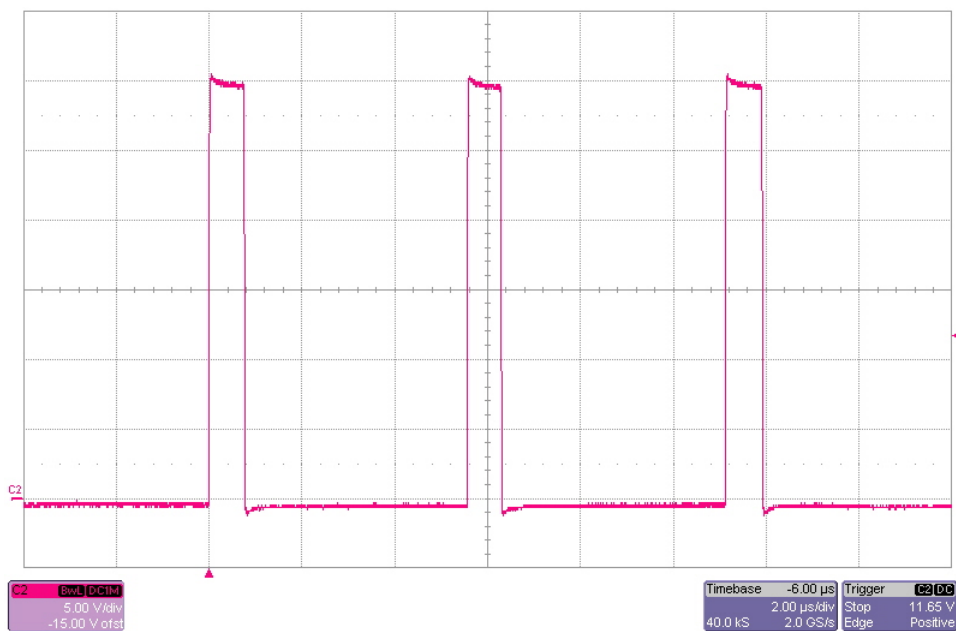
The photo below is of FET Q1 switch node (TP4). The input voltage is 30V and the outputs are loaded to max. (10V/DIV, 2uS/DIV)



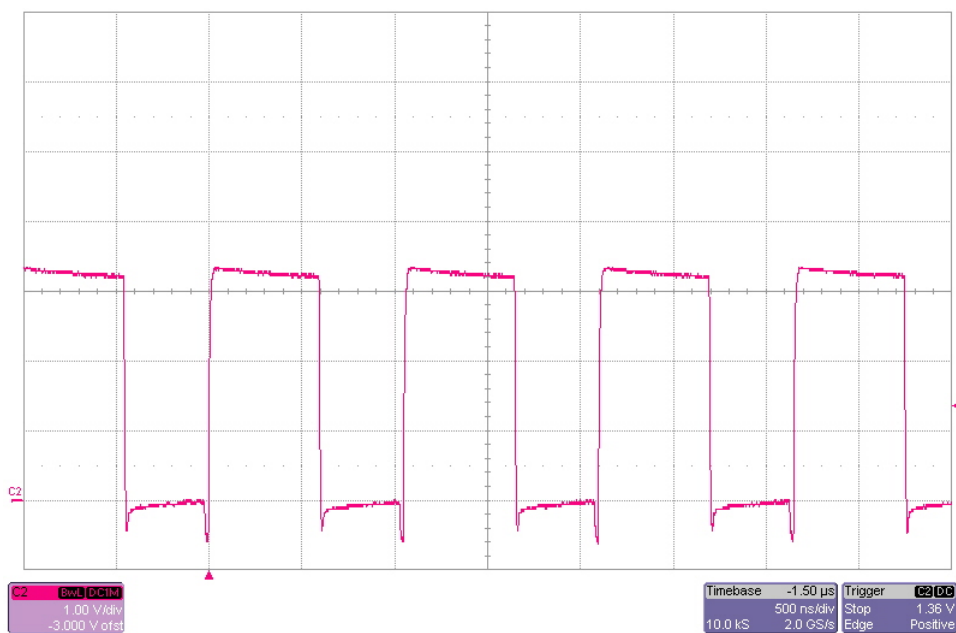
The photo below is of FET Q1 switch node (TP4). The input voltage is 30V and the outputs are loaded to min (20% of max load). (10V/DIV, 2uS/DIV)



The photo below is of FET Q2 switch node (TP12). The input voltage is 30V and the 3.3V and 1.8V outputs are loaded to max. (5V/DIV, 2uS/DIV)



The photo below is of the switch node voltage at U3 - pin5 (SW). The input voltage is 30V and the 3.3V and 1.8V outputs are loaded to max. (1V/DIV, 500nS/DIV)



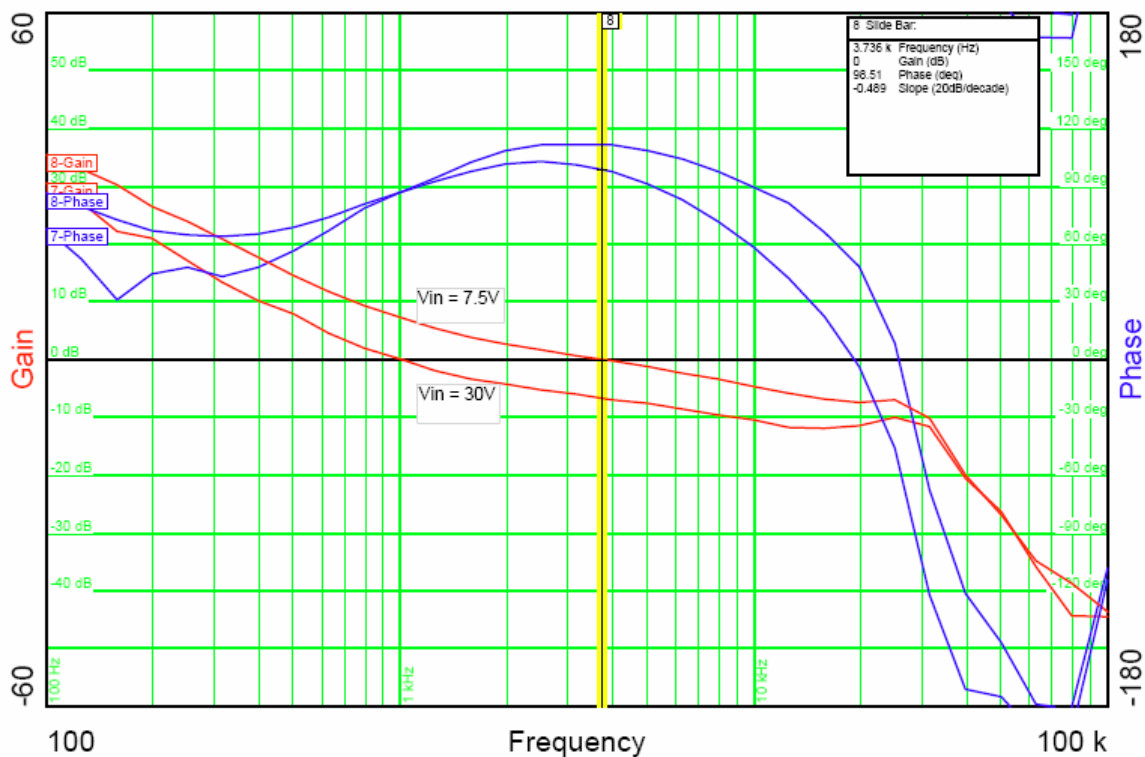
6 Control Loop Gain / Stability

The plot below shows the flyback loop gain and phase margin with the input voltage set to 7.5V and 30V. The outputs are loaded to max.

(7.5Vin)

Band Width = 3.7KHz,

Phase Margin = 98 degrees

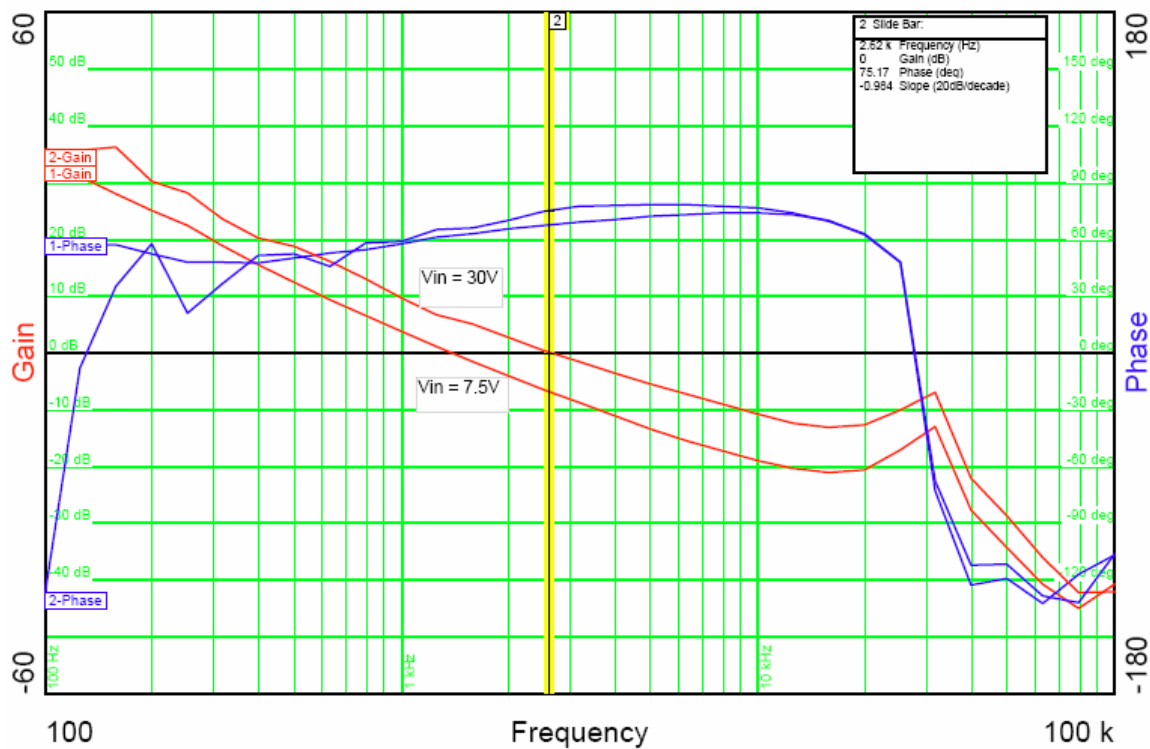


The plot below shows the flyback loop gain and phase margin with the input voltage set to 7.5V and 30V. The outputs are loaded to min.

(30Vin)

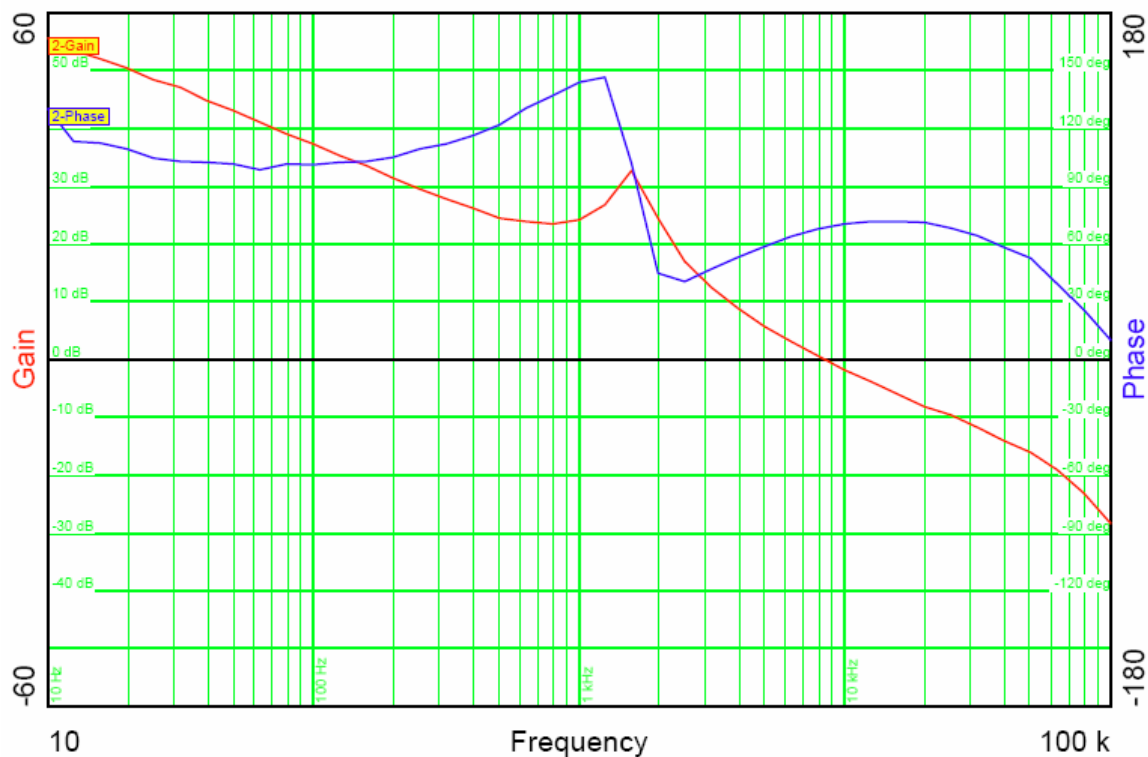
Band Width = 2.6KHz,

Phase Margin = 75 degrees



The plot below shows the 3.3V buck loop gain and phase margin with the input voltage set to 12V. The outputs are loaded to max.

Band Width = 8.5KHz, Phase Margin = 68 degrees



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