1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 12.0V, with no load on the 1.2V output.

Channel C1: **Input voltage**
2V/div, 100us/div

Channel C2: **Output voltage**
500mV/div, 100us/div

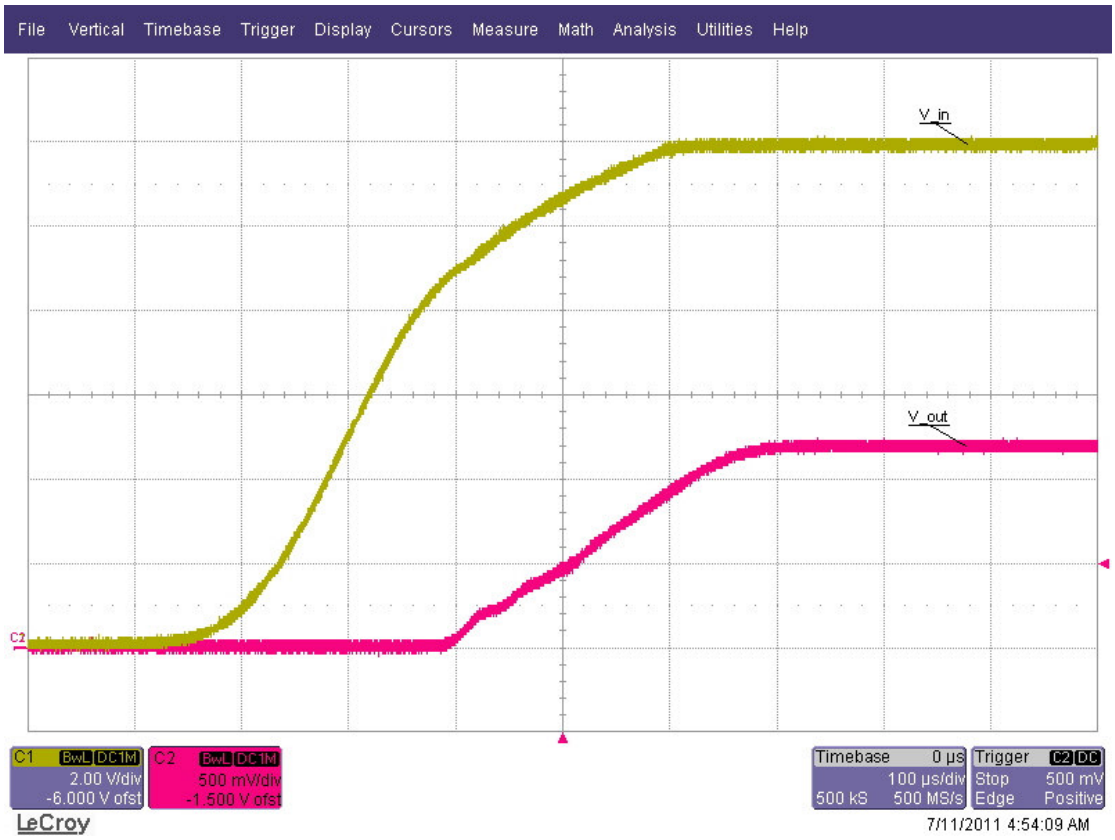

Figure 1

2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage is set at 12.0V with a 3.8A load on the 1.2V output.

Channel C1: **Input voltage**
2V/div, 500us/div

Channel C2: **Output voltage**
500mV/div, 500us/div

Figure 2

3 Efficiency

The efficiency is shown in Figure 3.

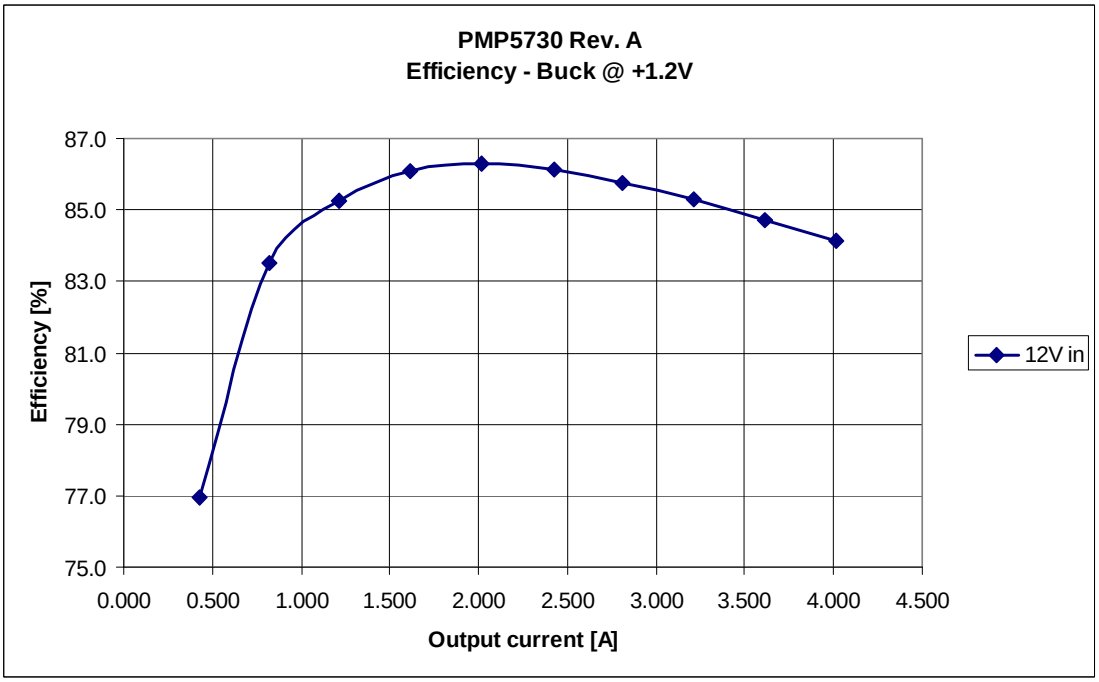

Figure 3

4 Load regulation

The load regulation of the 1.2V output is shown in Figure 4.

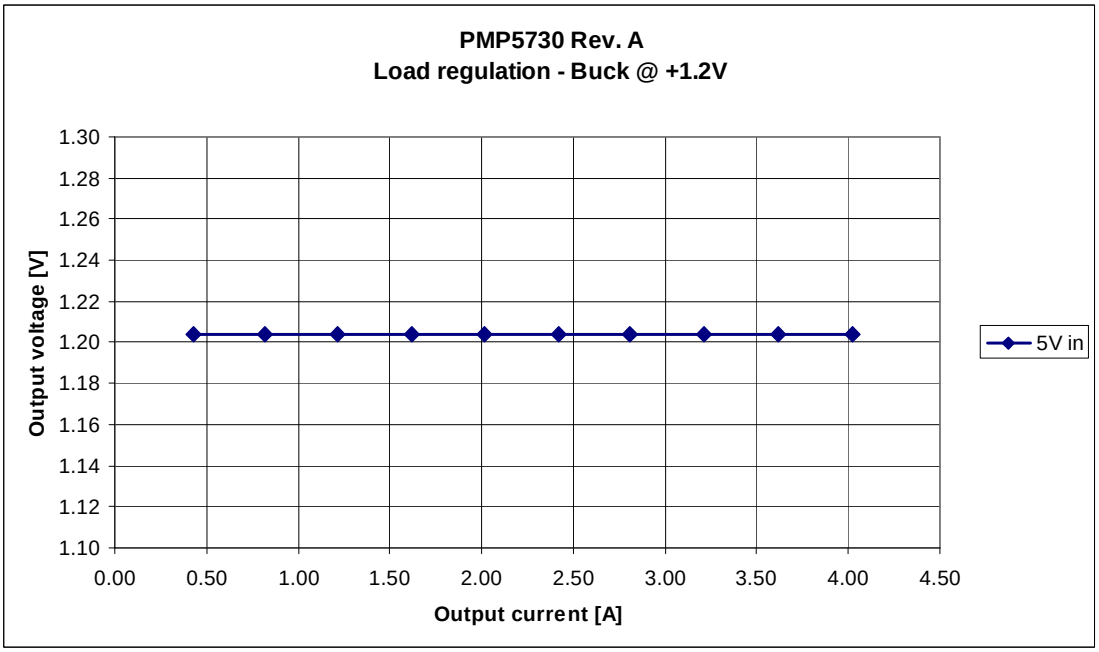

Figure 4

5 Output ripple voltage

The output ripple voltage at 3.8A load and 12.0V input voltage is shown in Figure 5.

Channel C2: **Output voltage**, 3mV peak-peak
20mV/div, 5us/div, AC coupled

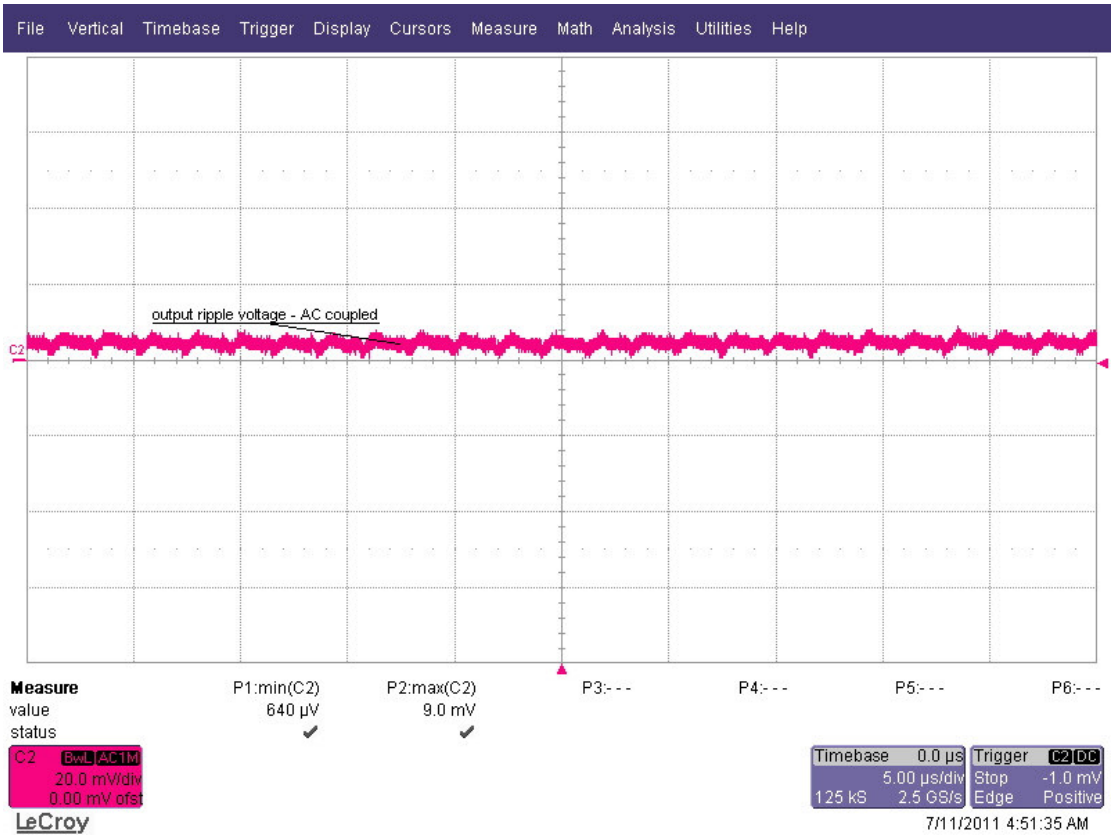

Figure 5

6 Load transients

The response to a load step and a load dump at an input voltage of 12.0V is shown in Figure 6 and Figure 7.

Channel C2: **Output voltage**, -65mV undershoot
50mV/div, 50us/div, AC coupled

Channel C1: **Load current**, load step 30mA to 3.8A
2A/div, 50us/div

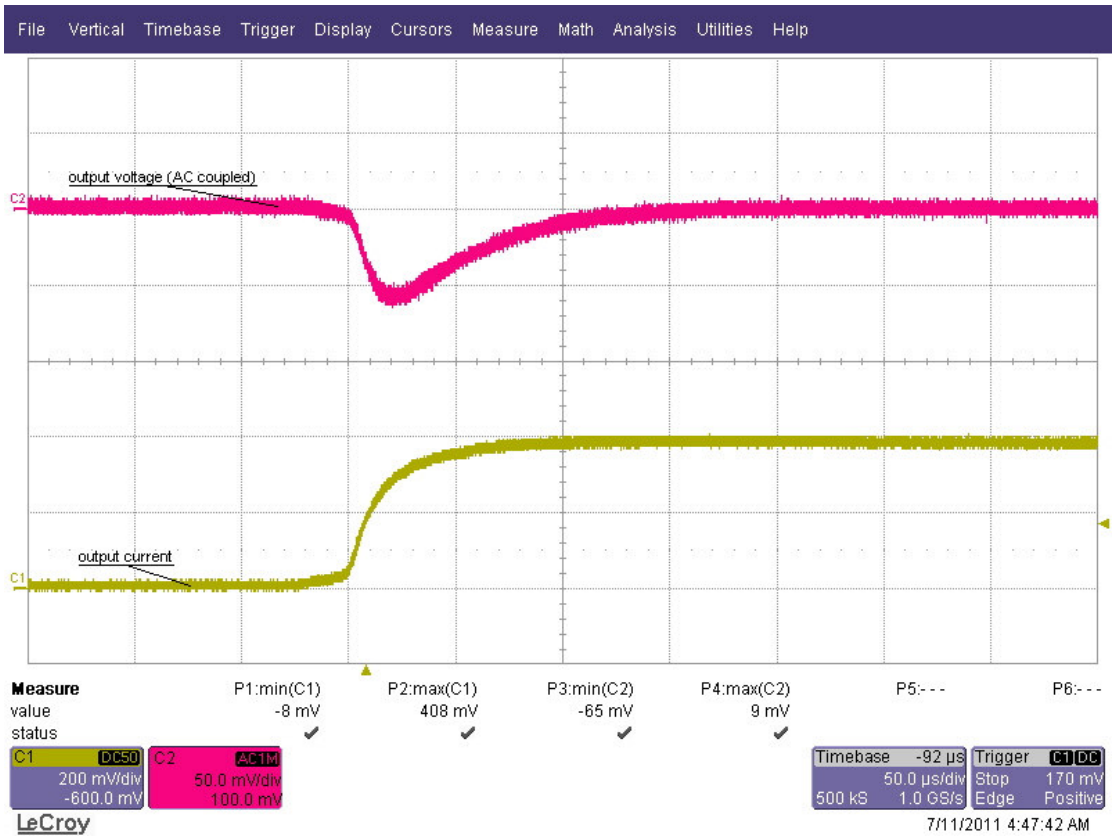

Figure 6

Channel C2: **Output voltage**, 54mV overshoot
50mV/div, 50us/div, AC coupled

Channel C1: **Load current**, load dump 3.8A to 30mA
2A/div, 50us/div

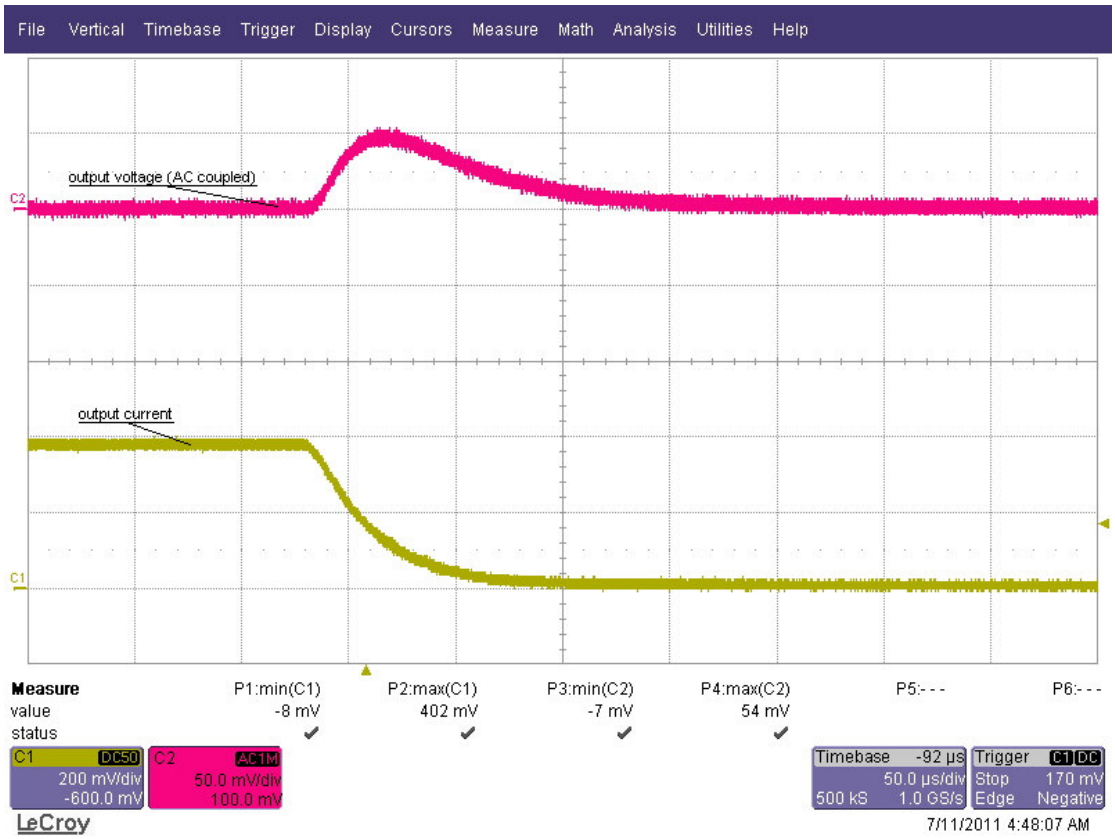

Figure 7

7 Frequency response

Figure 8 shows the loop response of the 1.2V output with 12.0V input and a 2.0A load.

- 59 deg phase margin @ crossover frequency 37.3 kHz
- -12.4db gain margin

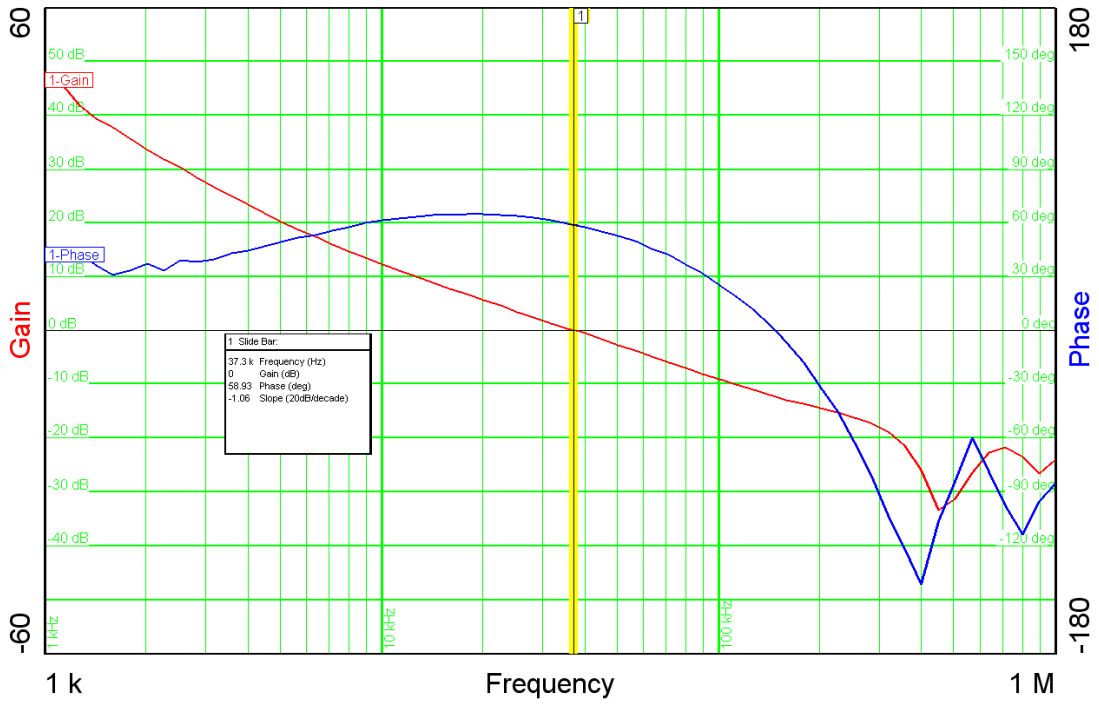

Figure 8

8 Miscellaneous waveforms

The drain-source voltage on the switching node is shown in Figure 9. The image was captured with 12.0V input and a 3.8A load.

Channel C2: **Drain-source voltage**, -1.9V minimum voltage, 12.7V maximum voltage
2V/div, 1us/div

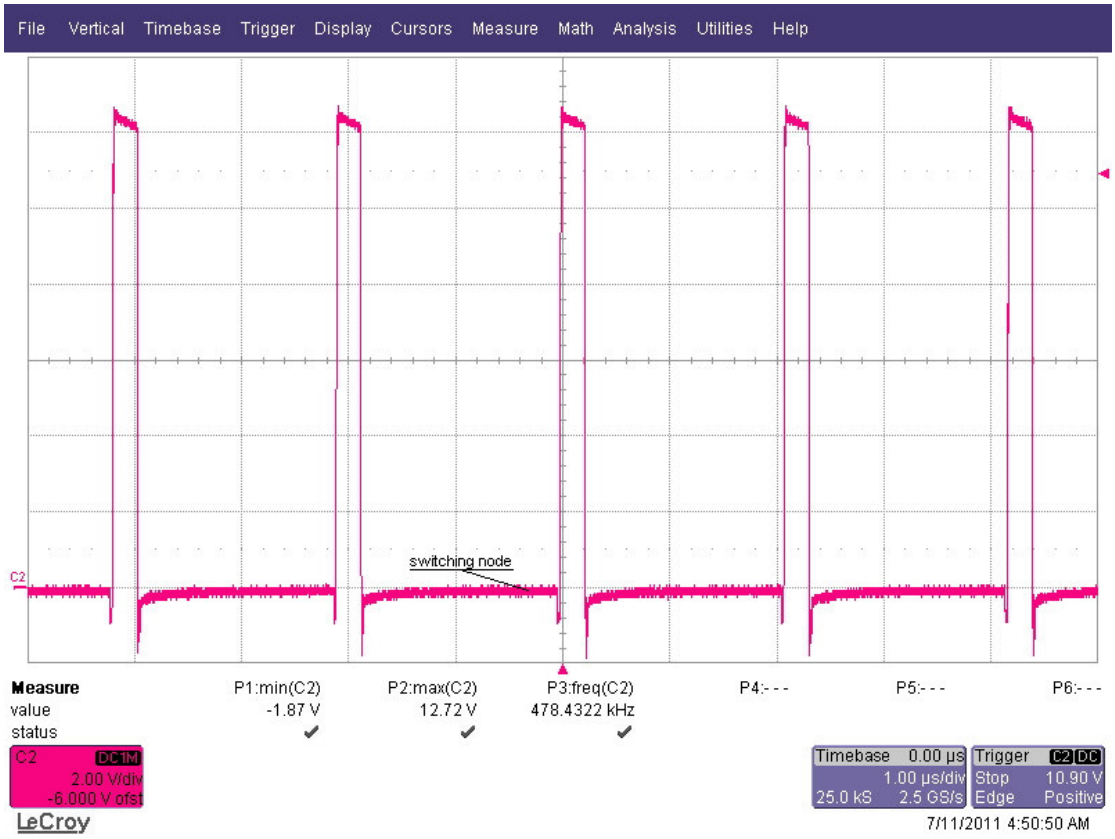

Figure 9

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