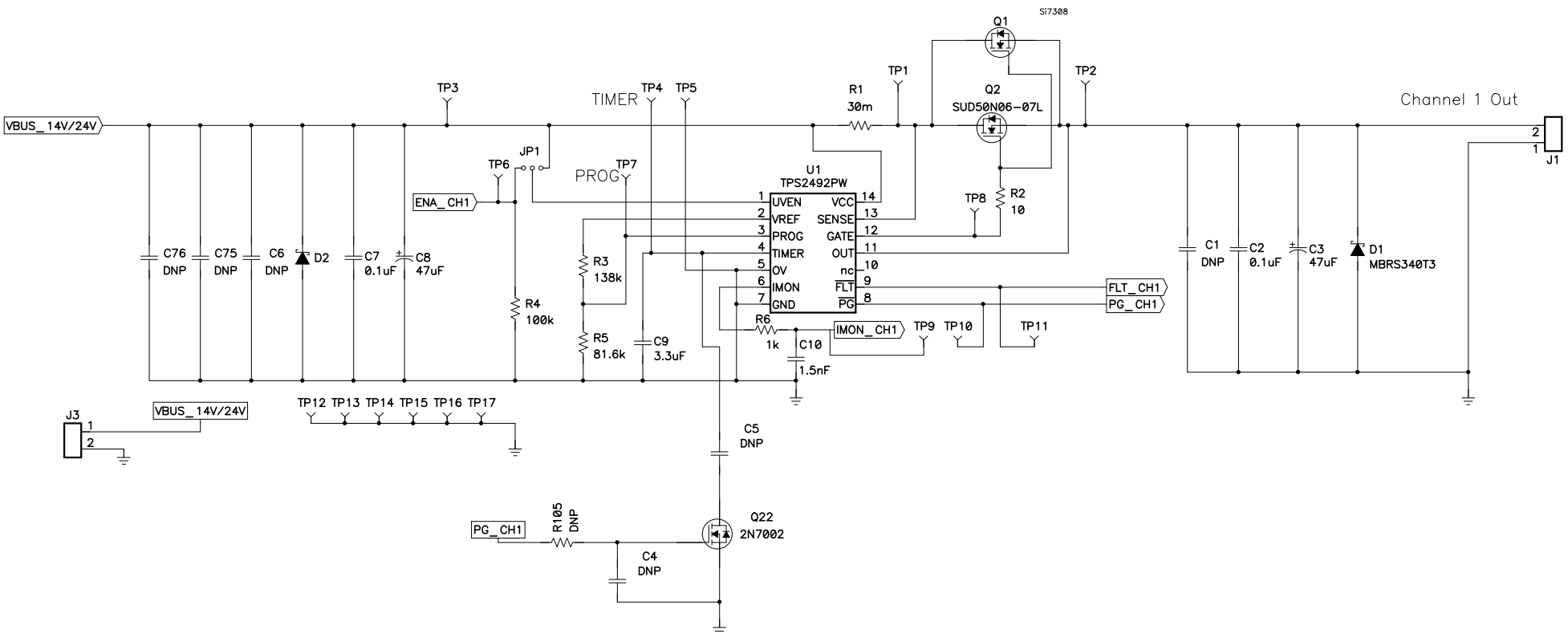

7–Channel Supply derived from 1 Input source.
– All seven channels (Sheet 1–7) are redundant in terms of layout
– The power stage from Vin to Rsense (R1) through FET to Output should be 10–A rated(see HPA491 example)
– 2oz copper
– The current sense resistor, R1, needs to have Kelvin connection on both terminals
– FET Q2 is a DPAK footprint and should be on backside of board. Let's use plenty of Vias from top to bottom
– Drain node should be present on Top, Internal 1, Internal 2, and Gnd
– C7 should be close to IC
– All I/Os to U8 from U1–U7 (UVEN, FLT, PG, IMON) should run on Internal 2
– Bottom and Internal 1 should be comprised of mostly GND and Drain copper

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Size: C	Number: PMP5927	Rev: E1
Date: Sat Oct 30, 2010		Drawn by: R Manack
Engineer: R Manack	Filename: PMP5927A.sch	Sheet: 1 of 9

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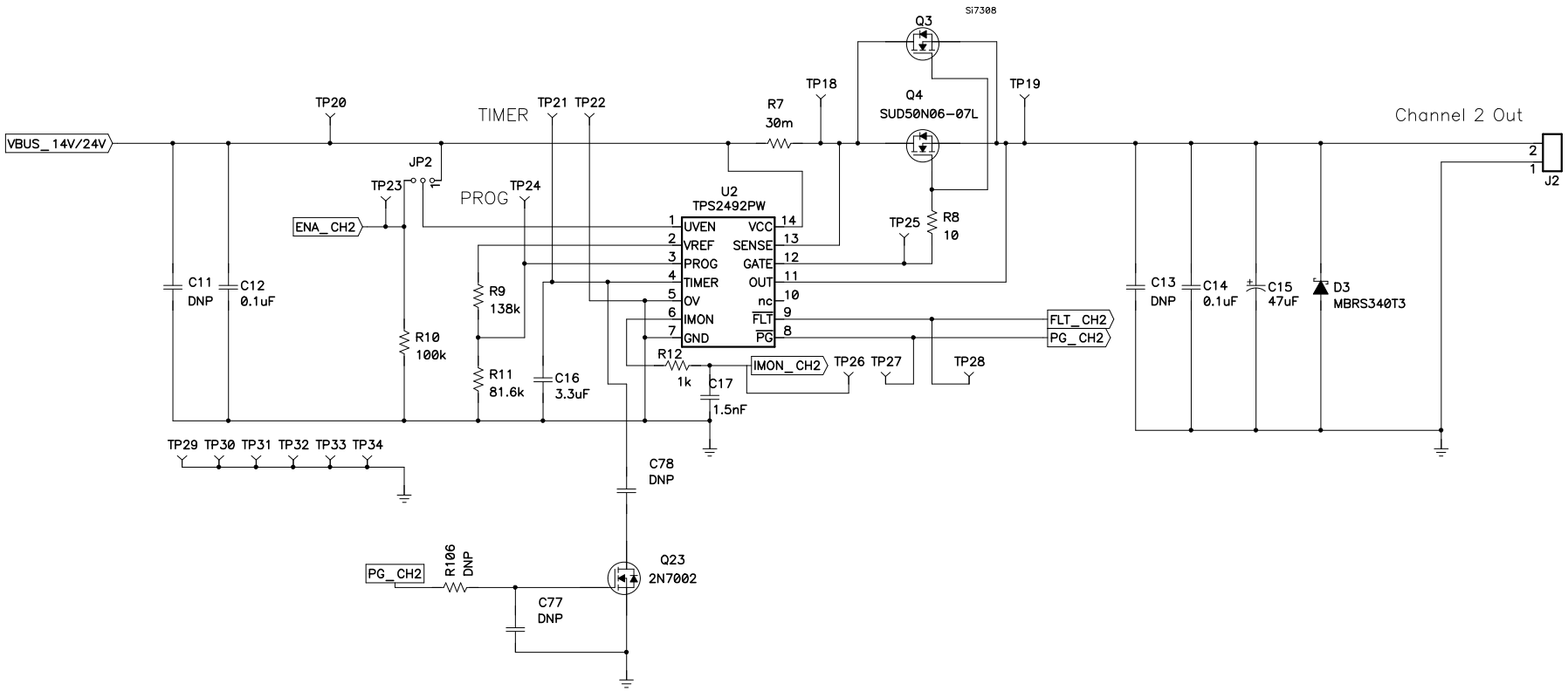

7–Channel Supply derived from 1 Input source.
– All seven channels (Sheet 1–7) are redundant in terms of layout
– The power stage from Vin to Rsense (R7) through FET to Output should be 10–A rated(see HPA491 example)
– 2oz copper
– The current sense resistor, R7, needs to have Kelvin connection on both terminals
– FET Q4 is a DPAK footprint and should be on backside of board
– Drain node should be present on Top, Internal 1, Internal 2, and Gnd
– C12 should be close to IC
– All I/Os to U8 from U1–U7 (UVEN, FLT, PG, IMON) should run on Internal 2
– Bottom and Internal 1 should be comprised of mostly GND and Drain Copper

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Size: C	Number: PMP5927	Rev: E1
Date: Sat Oct 30, 2010		Drawn by: R Manack
Engineer: R Manack	Filename: PMP5927A.sch	Sheet: 2 of 9

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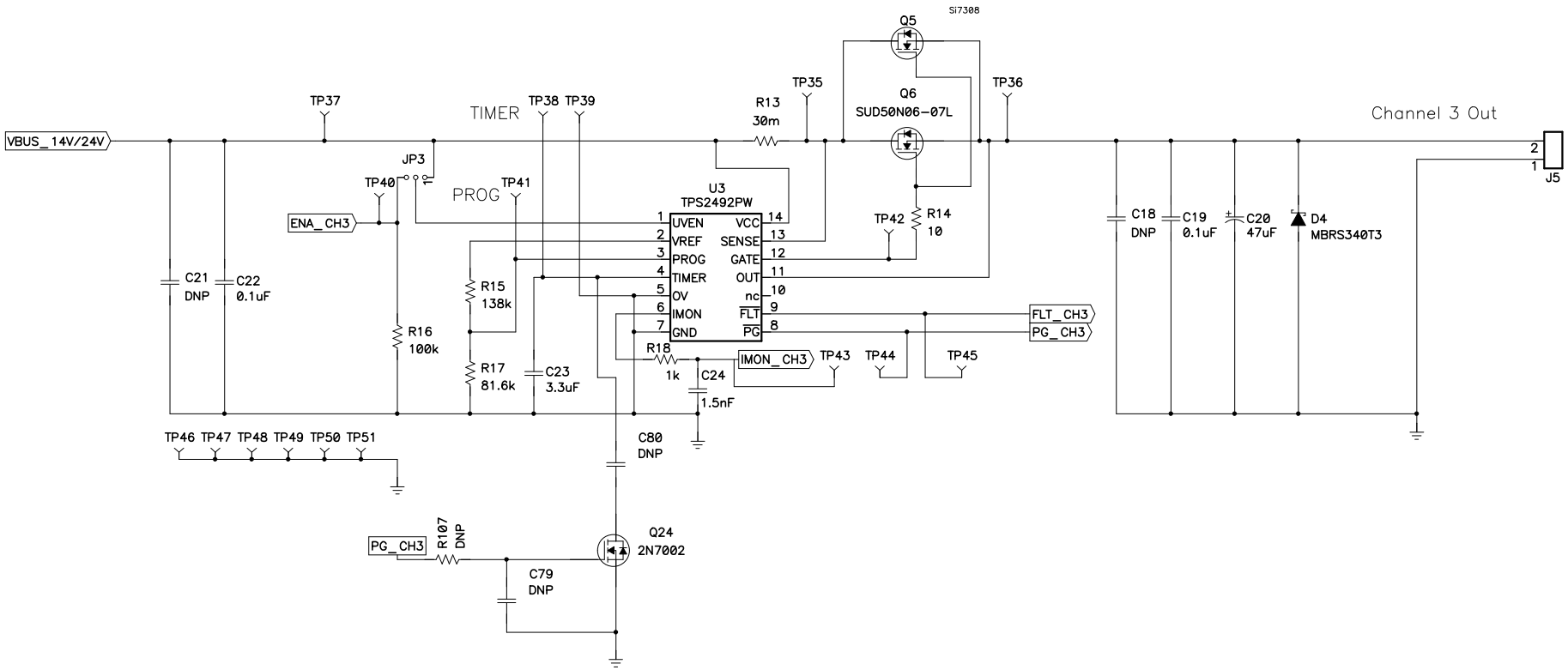

7-Channel Supply derived from 1 Input source.

- All seven channels (Sheet 1-7) are redundant in terms of layout
- The power stage from Vin to Rsense (R13) through FET to Output should be 10-A rated(see HPA491 example)
- 2oz copper
- The current sense resistor, R13, needs to have Kelvin connection on both terminals
- FET Q6 is a DPAK footprint and should be on backside of board
- Drain node should be present on Top, Internal 1, Internal 2, and Gnd
- C22 should be close to IC
- All I/Os to U8 from U1-U7 (UVEN, FLT, PG, IMON) should run on Internal 2
- Bottom and Internal 1 should be comprised of mostly GND and Drain Copper

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Size: C	Number: PMP5927	Rev: E1
Date: Sat Oct 30, 2010		Drawn by: R Manack
Engineer: R Manack	Filename: PMP5927A.sch	Sheet: 3 of 9

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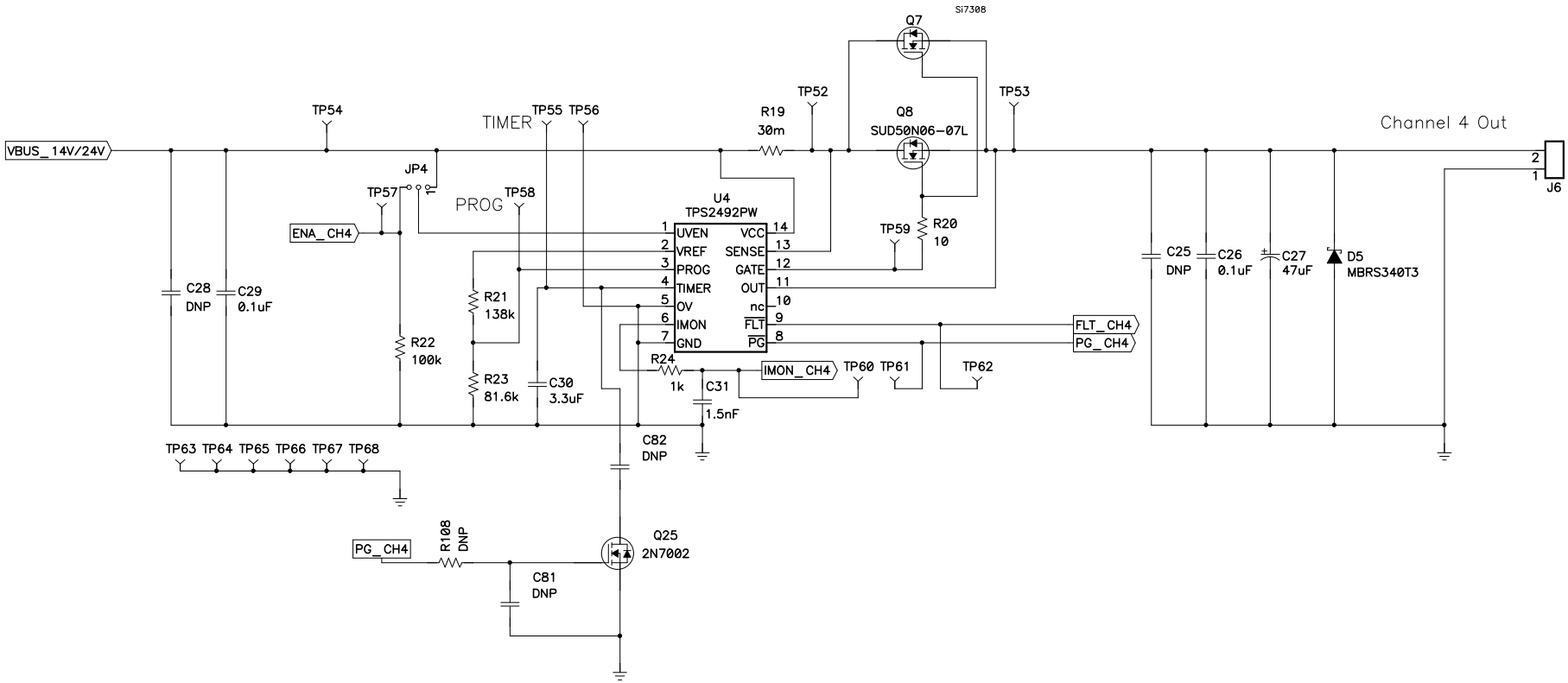

7–Channel Supply derived from 1 Input source.
– All seven channels (Sheet 1–7) are redundant in terms of layout
– The power stage from Vin to Rsense (R19) through FET to Output should be 10–A rated(see HPA491 example)
– 2oz copper
– The current sense resistor, R19, needs to have Kelvin connection on both terminals
– FET Q8 is a DPAK footprint and should be on backside of board
– Drain node should be present on Top, Internal 1, Internal 2, and Gnd
– C29 should be close to IC
– All I/Os to U8 from U1–U7 (UVEN, FLT, PG, IMON) should run on Internal 2
– Bottom and Internal 1 should be comprised of mostly GND and Drain Copper

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Size: C	Number: PMP5927	Rev: E1
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Engineer: R Manack	Filename: PMP5927A.sch	Sheet: 4 of 9

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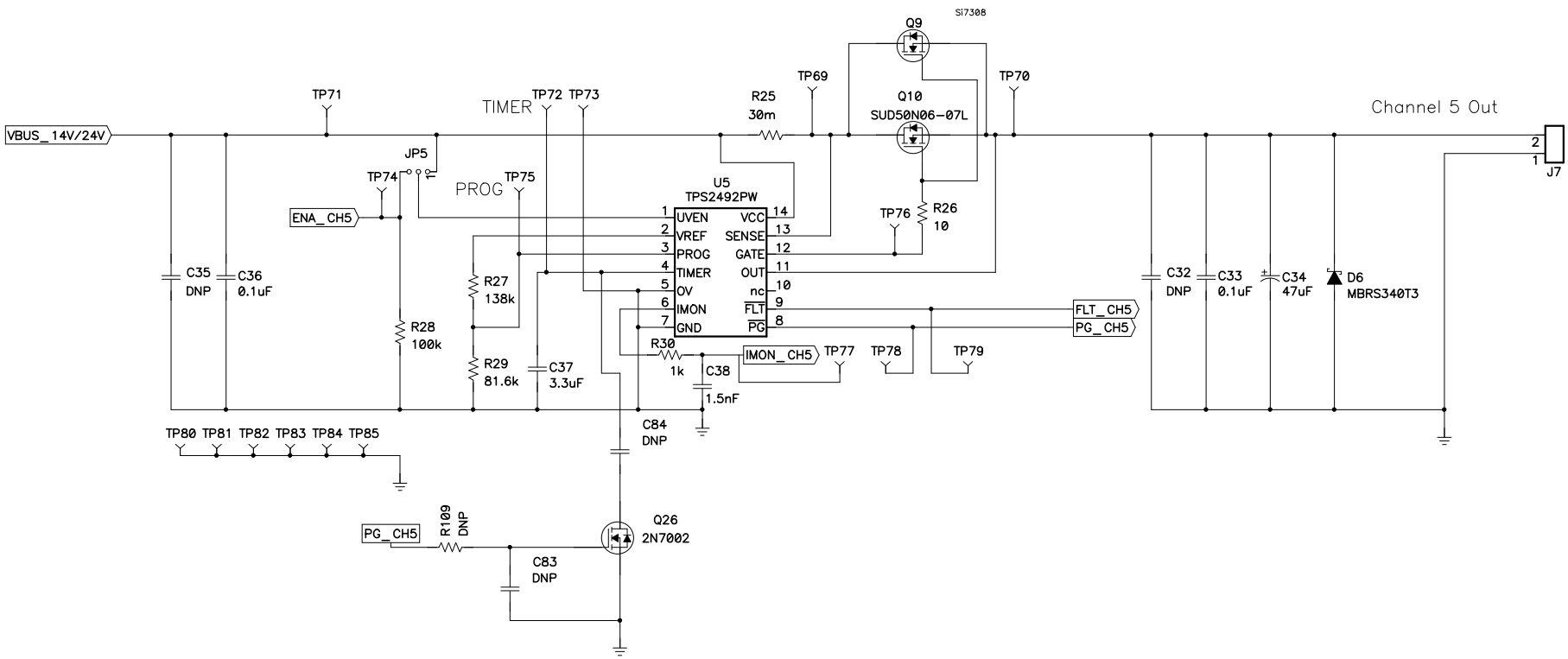

7–Channel Supply derived from 1 Input source.
– All seven channels (Sheet 1–7) are redundant in terms of layout
– The power stage from Vin to Rsense (R25) through FET to Output should be 10–A rated(see HPA491 example)
– 2oz copper
– The current sense resistor, R25, needs to have Kelvin connection on both terminals
– FET Q10 is a DPAK footprint and should be on backside of board
– Drain node should be present on Top, Internal 1, Internal 2, and Gnd
– C7 should be close to IC
– All I/Os to U8 from U1–U7 (UVEN, FLT, PG, IMON) should run on Internal 2
– Bottom and Internal 1 should be comprised of mostly GND and Drain Copper

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Size C	Number PMP5927	Rev E1
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Engineer R Manack	Filename PMP5927A.sch	Sheet 5 of 9

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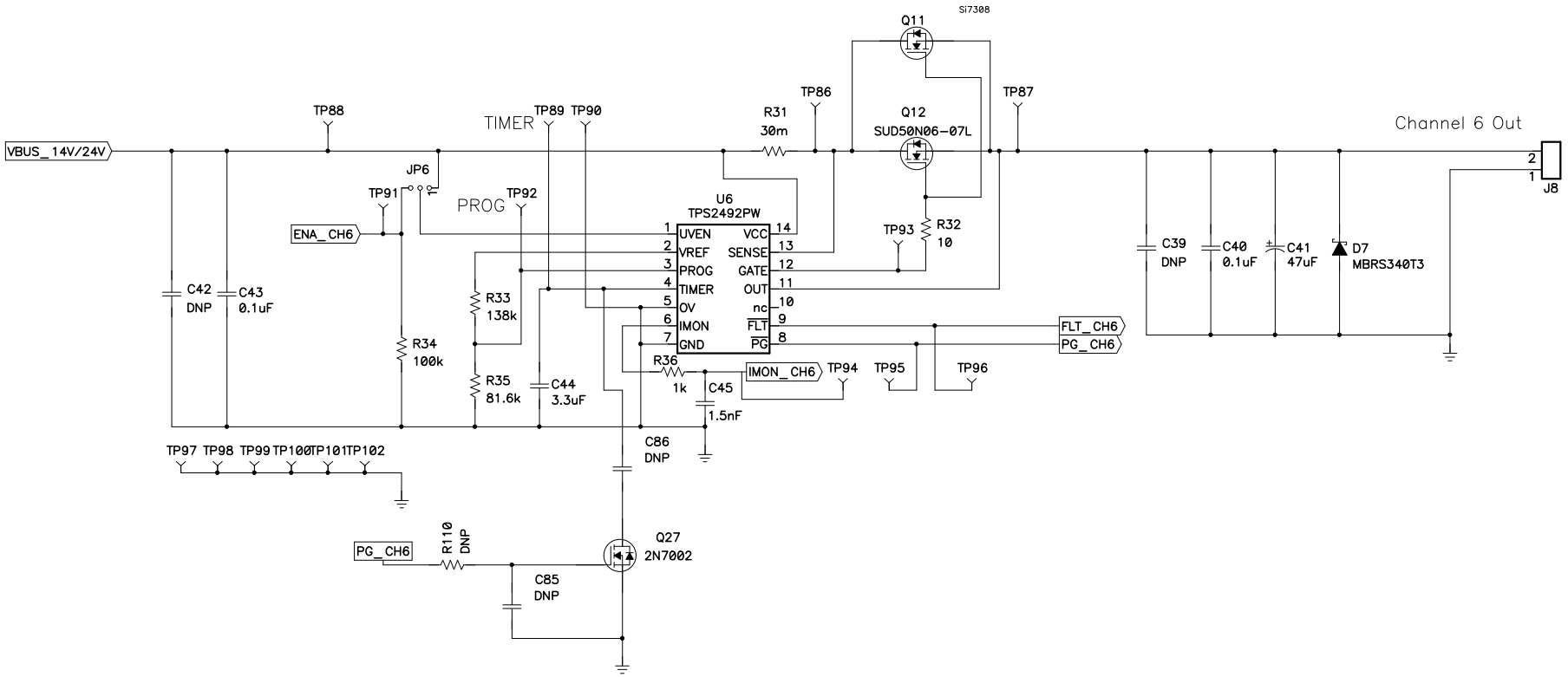

7–Channel Supply derived from 1 Input source.
– All seven channels (Sheet 1–7) are redundant in terms of layout
– The power stage from Vin to Rsense (R31) through FET to Output should be 10–A rated(see HPA491 example)
– 2oz copper
– The current sense resistor, R31, needs to have Kelvin connection on both terminals
– FET Q12 is a DPAK footprint and should be on backside of board
– Drain node should be present on Top, Internal 1, Internal 2, and Gnd
– C43 should be close to IC
– All I/Os to U8 from U1–U7 (UVEN, FLT, PG, IMON) should run on Internal 2
– Bottom and Internal 1 should be comprised of mostly GND and Drain Copper

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Date: Sat Oct 30, 2010		Drawn by: R Manack
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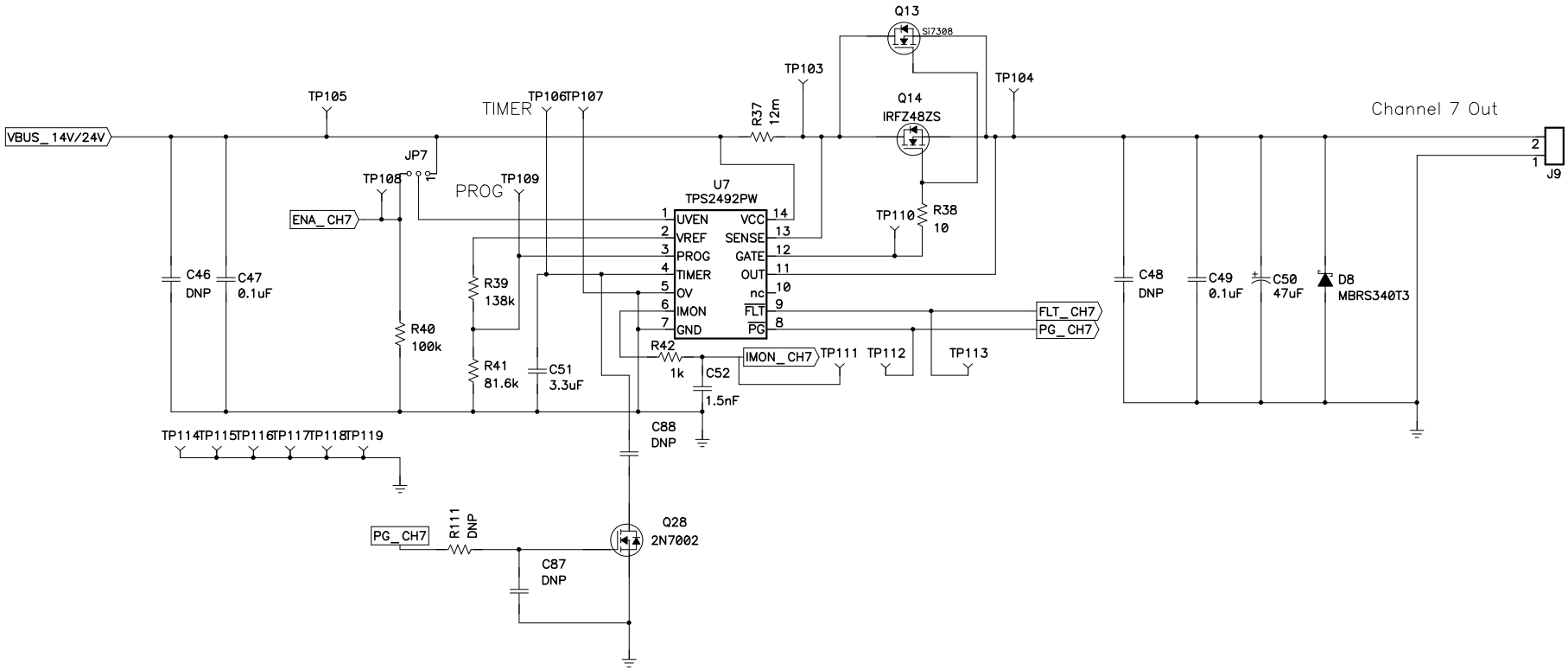

7–Channel Supply derived from 1 Input source.
– All seven channels (Sheet 1–7) are redundant in terms of layout
– The power stage from Vin to Rsense (R37) through FET to Output should be 10–A rated(see HPA491 example)
– 2oz copper
– The current sense resistor, R37, needs to have Kelvin connection on both terminals
– FET Q14 is a DPAK footprint and should be on backside of board
– Drain node should be present on Top, Internal 1, Internal 2, and Gnd
– C47 should be close to IC
– All I/Os to U8 from U1–U7 (UVEN, FLT, PG, IMON) should run on Internal 2
– Bottom and Internal 1 should be comprised of mostly GND and Drain Copper

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Size: C	Number: PMP5927	Rev: E1
Date: Sat Oct 30, 2010		Drawn by: R Manack
Engineer: R Manack	Filename: PMP5927A.sch	Sheet: 7 of 9

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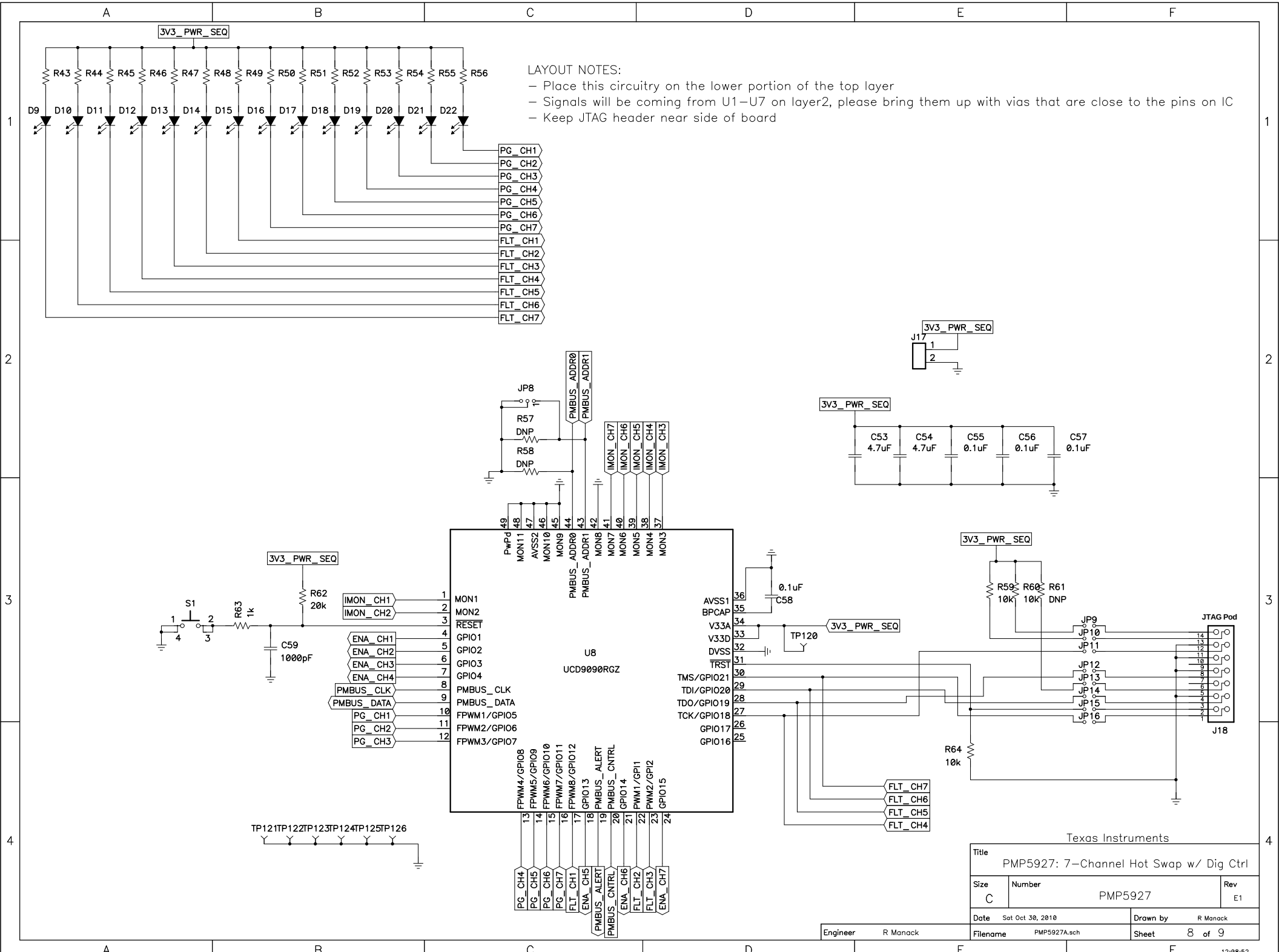

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Title: PMP5927: 7–Channel Hot Swap w/ Dig Ctrl		
Size: C	Number: PMP5927	Rev: E1
Date: Sat Oct 30, 2010		Drawn by: R Manack
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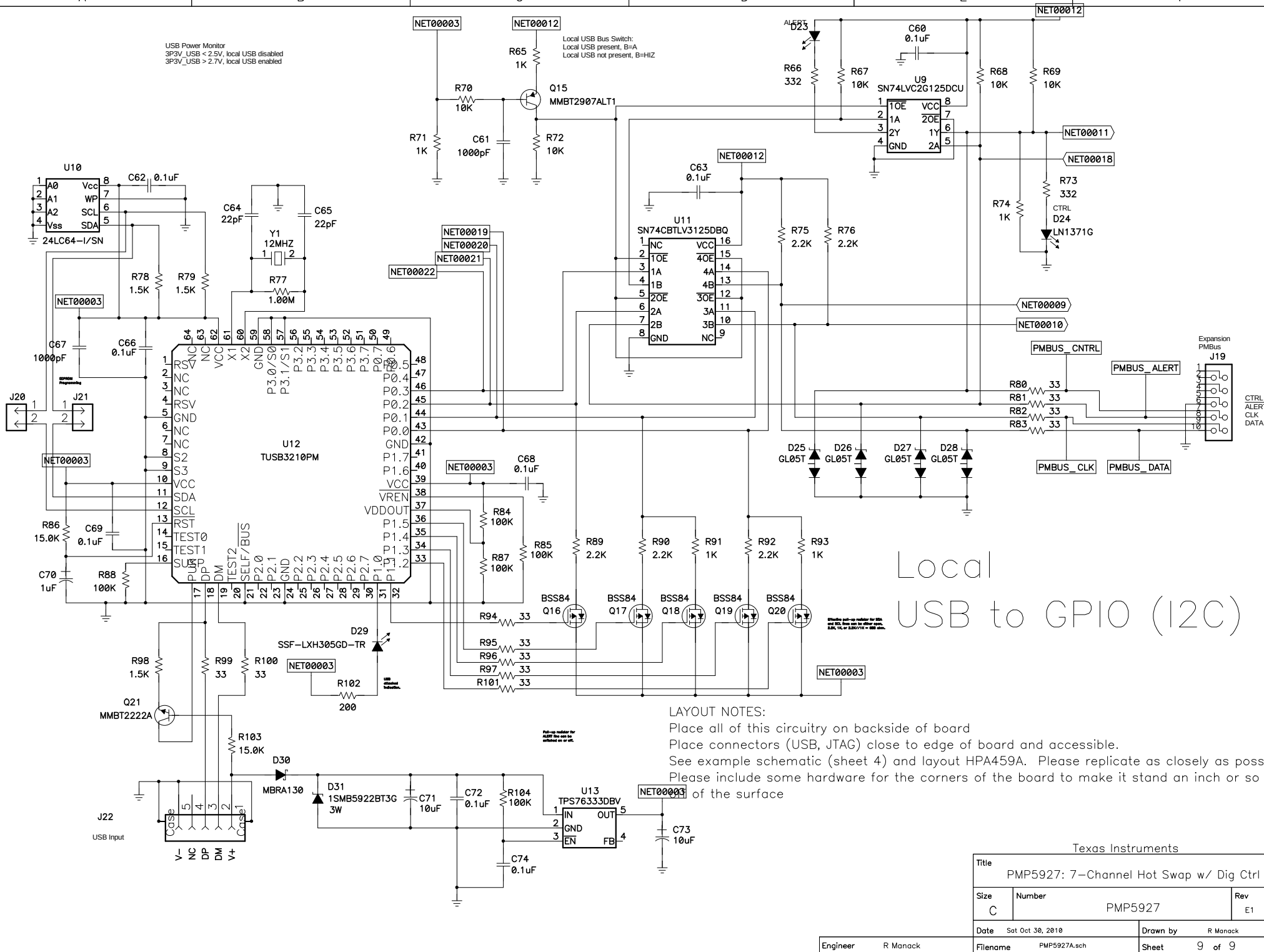
USB Power Monitor
3P3V_USB < 2.5V, local USB disabled
3P3V_USB > 2.7V, local USB enabled
Local USB Bus Switch:
Local USB present, B=A
Local USB not present, B=HIZ
U10
24LC64-I/SN
U11
SN74CBTLV3125DBQ
U9
SN74LVC2G125DCU
U12
TUSB3210PM
Y1
12MHZ
Q15
MMBT2907ALT1
Q21
MMBT2222A
D23
D24
LN1371G
D25
D26
D27
D28
GL05T
D29
SSF-LXH305GD-TR
D30
MBRA130
D31
1SMB5922BT3G
3W
U13
TPS76333DBV
J19
Expansion
PMBus
J20
J21
J22
USB Input
PMBUS_CNTRL
PMBUS_ALERT
PMBUS_CLK
PMBUS_DATA
CTRL
ALERT
CLK
DATA
BSS84
Q16
Q17
Q18
Q19
Q20
Local
USB to GPIO (I2C)
LAYOUT NOTES:
Place all of this circuitry on backside of board
Place connectors (USB, JTAG) close to edge of board and accessible.
See example schematic (sheet 4) and layout HPA459A. Please replicate as closely as possible.
Please include some hardware for the corners of the board to make it stand an inch or so
of the surface
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Title
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Size
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E1
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R Manack
Engineer
R Manack
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