Test Report: DC Power-Line Communication Reference Design

Reference Design

Literature Number: TIDU168
October 2013

System Description

The DC (24 V, nominal) Power-Line Communication (PLC) reference design is intended as an evaluation module for users to develop end-products for industrial applications leveraging the capability to deliver both power and communications over the same DC-power line. The reference design provides a complete design guide for the hardware and firmware design of a master (PLC) node, slave (PLC) node in an extremely small (approximately 1-inch diameter) industrial form factor. The design files include schematics, BOMs, layer plots, Altium files, Gerber Files, a complete software package with the application layer, and an easy-to-use Graphical User Interface (GUI).

The application layer handles the addressing of the slave (PLC) nodes as well as the communication from the host processor (PC or Sitara™ ARM® MPU from Texas Instruments). The host processor communicates only to the mater (PLC) node through a USB-UART interface. The master node then communicates to the slave nodes through PLC. The easy-to-use GUI is also included in the EVM that runs on the host processor and provides address management as well as slave-node status monitoring and control by the user.

The reference design has been optimized from each slave (PLC)-node source-impedance perspective that multiple slaves can be connected to the master (see Section 2.1). Protection circuitry has also been added to the analog front-end (AFE) so that it can be reliably AC coupled to the 24-V line (see Section 2.4). Also note that this reference design layout has been optimized to meet the PLC-power requirements. See for the AFE031 layout requirements for high-current traces.

At the heart of this reference design are the AFE from TI, AFE031, to interface with power lines and the TMS320F28035 Piccolo™ Microcontroller that runs the PLC-Lite protocol from TI.

1.1 AFE031

The AFE031 device is a low-cost, integrated, power-line communication (PLC) AFE device that is capable of capacitive-coupled or transformer-coupled connections to the power line while under the control of a DSP or microcontroller. The AFE031 device is also ideal for driving low-impedance lines that require up to 1.5 A into reactive loads. The integrated receiver is able to detect signals down to 20 µVRMS and is capable of a wide range of gain options to adapt to varying input signal conditions. This monolithic integrated circuit provides high reliability in demanding power-line communications applications. The AFE031 transmit power-amplifier operates from a single supply in the range of 7 V to 24 V. At a maximum output current, a wide output swing provides a 12-VPP (IOUT = 1.5 A) capability with a nominal 15-V supply.

The analog and digital signal-processing circuitry operates from a single 3.3-V power supply. The AFE031 device is internally protected against overtemperature and short-circuit conditions. The AFE031 device also provides an adjustable current limit. An interrupt output is provided that indicates both current limit and thermal limit. There is also a shutdown pin that can be used to quickly put the device into its lowest power state. Through the four-wire serial-peripheral interface, or SPI™, each functional block can be enabled or disabled to optimize power dissipation. The AFE031 device is housed in a thermally-enhanced, surface-mount PowerPAD™ package (QFN-48). Operation is specified over the extended industrial junction temperature range of –40°C to +125°C.

1.2 C2000

The F2803x Piccolo family of microcontrollers (C2000™) provides the power of the C28x core and control-law accelerator (CLA) coupled with highly integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code, as well as providing a high level of analog integration. An internal voltage regulator allows for single-rail operation. Enhancements have been made to the HRPWM module to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0 to 3.3-V fixed full scale range and supports ratiometric VREFHI and VREFLO references. The ADC interface has been optimized for low overhead and latency.

Based on TI's powerful C2000-microcontroller architecture and the AFE031 device, developers can select the correct blend of processing capacity and peripherals to either add power-line communication to an existing design or implement a complete application with PLC communications.

Test Data

NOTE: The test data for the DC-PLC Reference Design is also included in the reference design document TIDU160.

2.1 Multiple Slave Nodes Support

The reference design is optimized from an impedance perspective to support multiple slave nodes. Refer to the SAT0021 schematic (see Figure A-1), as more and more nodes are added, the C11 capacitor is added in parallel and therefore the total capacitance as seen by a slave node increases. To support multiple slave nodes, the source impedance must be very small as compared to the load impedance (see Figure 2-1).

C11 (100 pF) creates a low-pass filter and, as multiple nodes are added, the effective capacitance increases. Note that a PLC network is a star topology where each node drives the effective combination load of every other node. Thus C11 is chosen to be 100 pF such that even when up to 10 nodes are added the effective capacitance would be 100 pF x× 10 = 1nF. Therefore the impedance at the PLC-modulation band (see) is calculated with Equation 1

$$\text{Impedance} = \frac{1}{2\pi f C} = \text{approximately } 1.8\,\text{k}\Omega$$

where

- f = 90 kHz
- C = 1 nF = 100 pF × 10 (1)

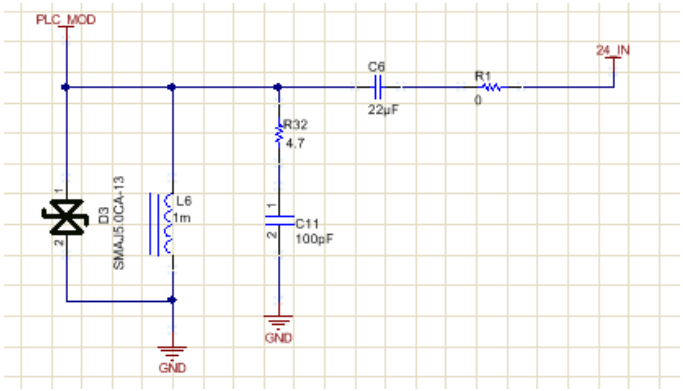


Figure 2-1. Power-Line Communication AC-Coupling Protection Circuitry

NOTE: Equation 2 is a key requirement to drive multiple slave nodes.

Source Impedance << Load Impedance (2)

For the following calculation assume that the PLC-Lite modulation frequency is approximately 40 KHz. The source impedance of a PLC node is then calculated as shown in Equation 3.

$$\text{Source Impedance} = \frac{1}{2\pi f c} = \frac{1}{2\pi(40000)(0.000022)} = 0.18\ \Omega$$

where

- c = C6 = 22 µF (see) (3)

Assume that the load impedance of a given slave node as seen by the driver PLC-node is approximately 30 Ω. As multiple slaves are added, this load impedance is reduced as the loads are seen as a parallel combination of load impedances. For example, if there are nine slaves on the system, then the total load impedance as seen by one driver PLC-node is calculated as shown in Equation 4.

9 (slaves) + 1 (Master) = 10 PLC nodes, Load Impedance = 30/10 = 3 Ω (4)

4 (slaves) + 1 (Master) = 5 PLC nodes, Load Impedance = 30/5 = 6 Ω (5)

Based on the system requirements, optimizing the capacitance C6, 22 µF, and C11, 100 pF, is important in order to meet the requirement of Equation 2.

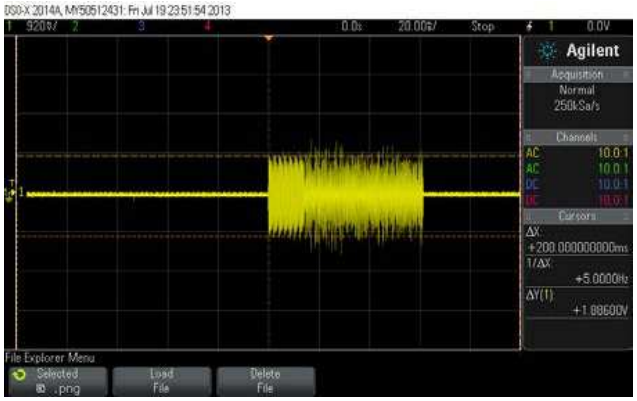


Figure 2-2. Test Results: One Master and Four Slaves

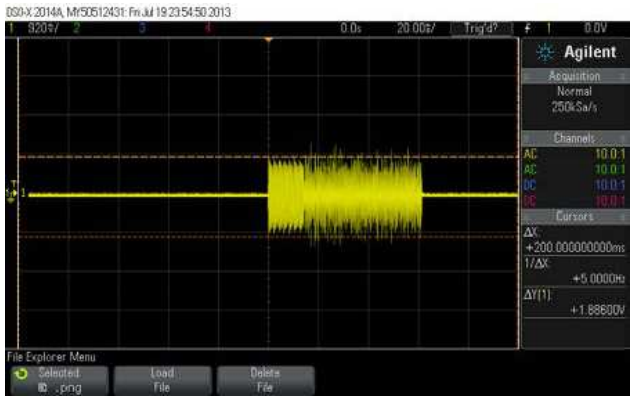


Figure 2-3. Test Results: One Master and No Slaves

As seen in Figure 2-2 and Figure 2-3, there is an insignificant change in amplitude of the modulation signal as more slaves are added. In the previous setup, the 24-V DC line is probed (AC coupled) to the oscilloscope. The oscilloscope is triggered when the button on the PLC node is pressed as it generates a PLC communication packet.

2.2 Multiple Slave transmissions and System Latency

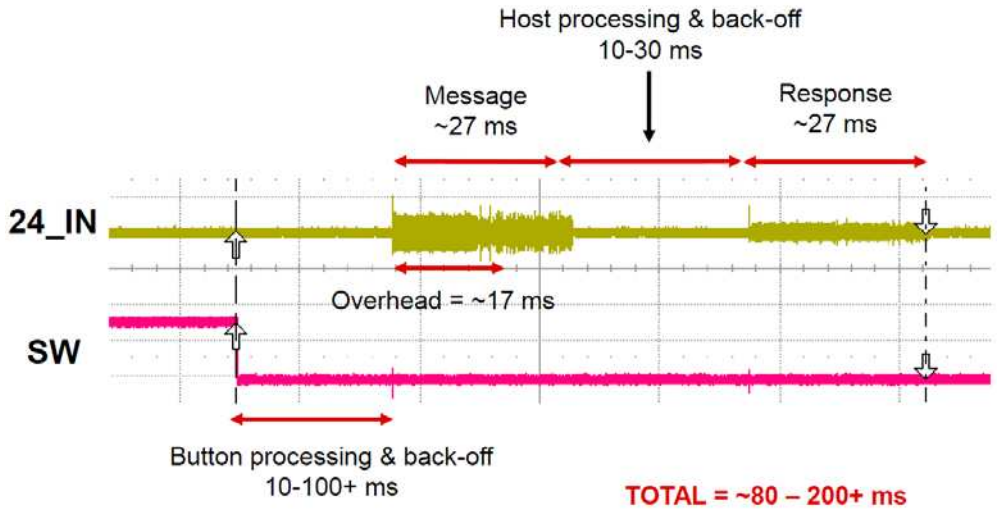


Figure 2-4. System Latency

PLC-Lite contains a simple CSMA/CA, MAC which means that if multiple slaves try to access the 24-V DC line, the MC layer in PLC-Lite senses that the line is busy and backs off for a random duration. The total latency for a typical transaction is thus a function of this random back-off for both the initial message and response, as well as the fixed time required to transmit the messages on the line. As shown in Figure 2-4, the system-level latency with one button press event was captured at approximately 80 to 200 ms. This measurement is typical for the default MAC and PHY layer settings used by the demonstration firmware. Modifying MAC or PHY layer parameters can change the system latency.

2.3 15-V Power-Supply Performance for AFE Power Amplifier

For this reference design, note that the 24-V DC supply generates a 15-V and 3.3-V supply as well as it is modulated by the AFE031 for PLC communication. The key point to note is that the switching-regulator operation that generates the 15 V and 3.3 V can interfere with PLC modulation if proper power supply filtering is not included in the design.

To ensure the above requirement, refer to the schematic as shown in : the first circuit seen by the 24-V DC line is a low-pass filter (see Section 2.3.1) which is a very important element of the design. Without this low-pass filter circuit, PLC communication will not work.

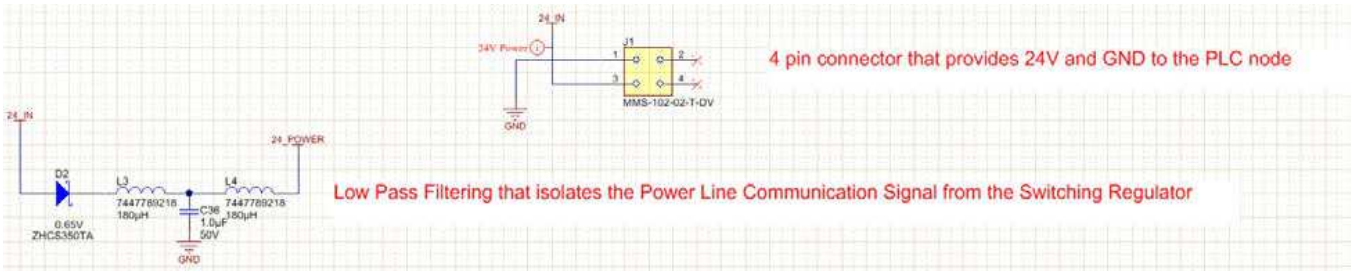


Figure 2-5. Power Section of the Schematic Showing the Low-Pass Filter

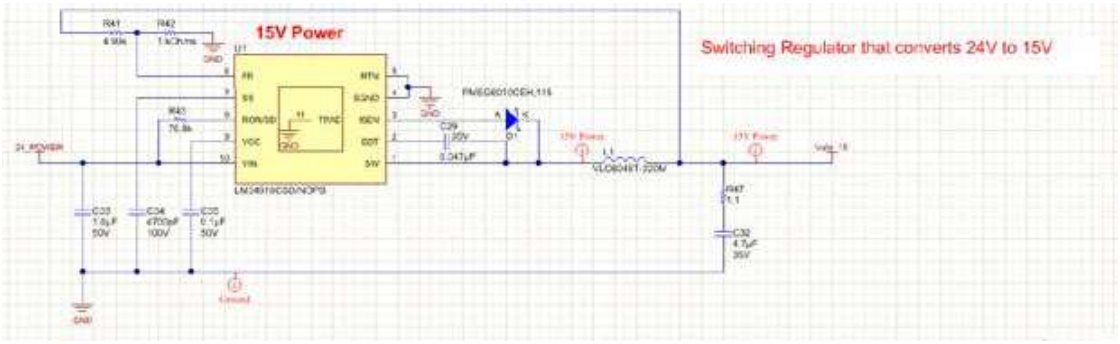


Figure 2-6. 15-V Section of the Power Schematic

In the DC-PLC reference design, another key requirements is to ensure that in an application when a PLC node transmits or receives data, the power amplifier for the AFE031 device is provided with the necessary power (500-mA power budget for the maximum TX swing) to drive the line and to drive the line with a fast response time. The LM34910 step-down switching regulator is used in this reference design (see Figure 2-6) to generate the 15 V for the power amplifier of the AFE031 device. The LM34910 device features all of the functions required to implement a low-cost efficient buck-bias regulator capable of supplying up to 1.25 A to the load. This buck regulator contains a 40-V N-Channel buck switch, and is available in the thermally enhanced WSON-10 package.

NOTE: The LM34910 device features a hysteretic-regulation scheme that requires no loop compensation, results in fast load-transient response, and simplifies circuit implementation.

The operating frequency remains constant with line and load variations because of the inverse relationship between the input voltage and the on-time.

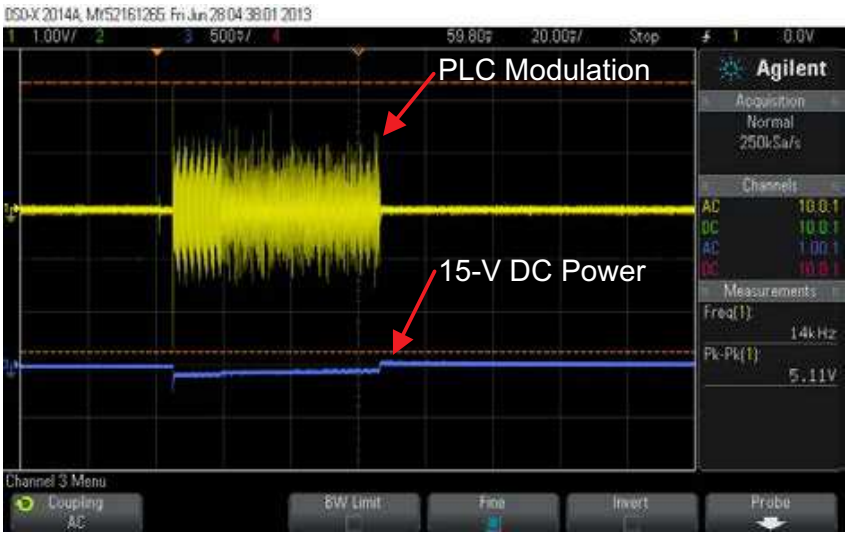


Figure 2-7. LM34910 With a 22-µH Inductor (TX Level 2 Vpp)

As shown in Figure 2-7, the LM34910 device as implemented in this reference design, provides the necessary power for the AFE031 to meet the PLC functionality.

NOTE: As seen in Section 2.5, the TX level of 2 Vpp is enough to drive up to a 40-m (length) cable without any BER.

2.3.1 T-Type Low-Pass Filter Design

As shown in and , a low-pass filter separates the PLC modulation signal from the switching regulator. The Fc of the low-pass filter is calculated based on the band occupied by the PLC modulation. As shown in , the PLC Lite occupies 42 to 90 kHz. Therefore, the Fc as per the low pass filter in comprises of L = 360 µH (180 µH + 180 µH) and C of 1 µF.

$$Fc = \frac{1}{\pi \times \sqrt{LC}} = \text{approximately } 17 \text{ kHz} \quad (6)$$

NOTE: Because of the space constraint on this reference design, the previous values of LC were selected. However in applications where board space is available, a lower cutoff Fc (lower than 10 KHz) is desirable.

2.4 PLC-Coupling Circuit Protection

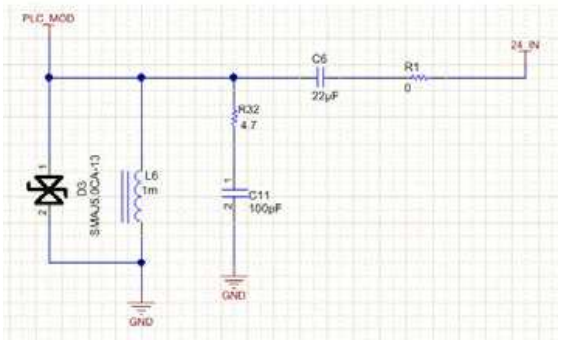


Figure 2-8. First-Stage AC Coupling

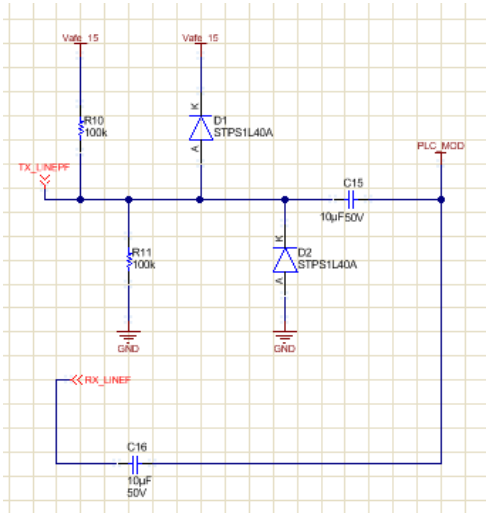


Figure 2-9. Second-Stage AC Coupling

To ensure the reliability of the overall system, the 24-V line is not directly AC coupled to the AFE031 device. The line goes through a two-step AC coupling (see Figure 2-8 and Figure 2-9). In the first stage, the 24-V line is AC coupled to an intermediary stage that has a TVS protection and therefore arrests voltage surges to 9.2 V for a peak surge current of 43.5 A. In this stage the common mode is biased to the GND. In the second-stage AC coupling, the data is AC coupled to the AFE031 device with a DC bias of 7.5 V. To ensure reliability, a simple test of powering off the node completely and then powering up the node was performed on five nodes approximately 250 times. This stress tests ensures that the surges on the power supply can be applied to the node under test.

Table 2-1. Reliability Data

PLC NODE	COMPLETE POWER-ON AND POWER-OFF SEQUENCE	STATUS
1	250 times	Pass, no reliability failure, no change in current drawn observed pre-stress and post-stress
2	250 times	
3	250 times	
4	250 times	
5	250 times	

2.4.1 PLC TX and RX Impedance-Path Testing

The impedance path of the TX and RX is optimized to avoid any signal losses to the PLC-modulation signal.

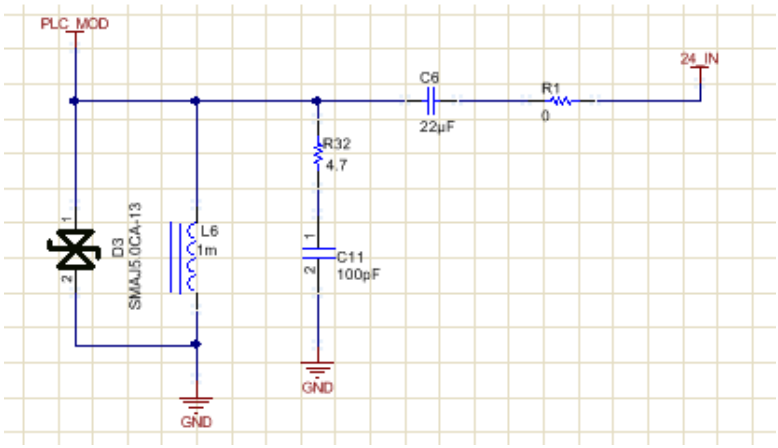


Figure 2-10. Power-Line Communication AC-Coupling Protection Circuitry

Figure 2-10 shows that R1 at 0 Ω provides optimized load impedance to the modulation signal. If R1 in Figure 2-10 is even changed to 15 µH (for example), the modulation signal is severely impeded as shown in Figure 2-11 and Figure 2-12.

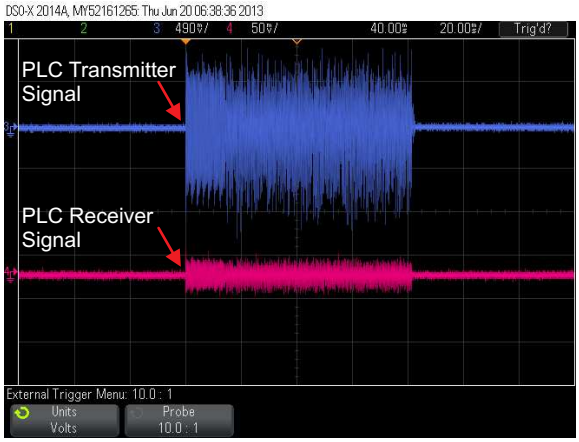


Figure 2-11. RX Signal Impeded With 15-µH Inductance

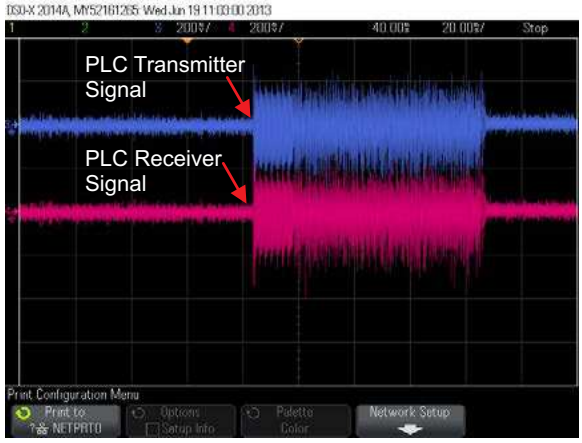


Figure 2-12. RX Signal Optimized With 0-Ω Resistor (R1)

2.5 PLC-Cable Performance Data

For performance characterization, a 40-m cable was used. To characterize the cable, use the following steps:

1. Generate a chirp signal.
2. Capture the response of the chirp after the cable as shown in Figure 2-13.
3. Post-process (correlation) the signal using Matlab® to generate the impulse response.
4. Leverage the impulse response of the given 40-m cable to generate approximately 320-m cable impulse response.

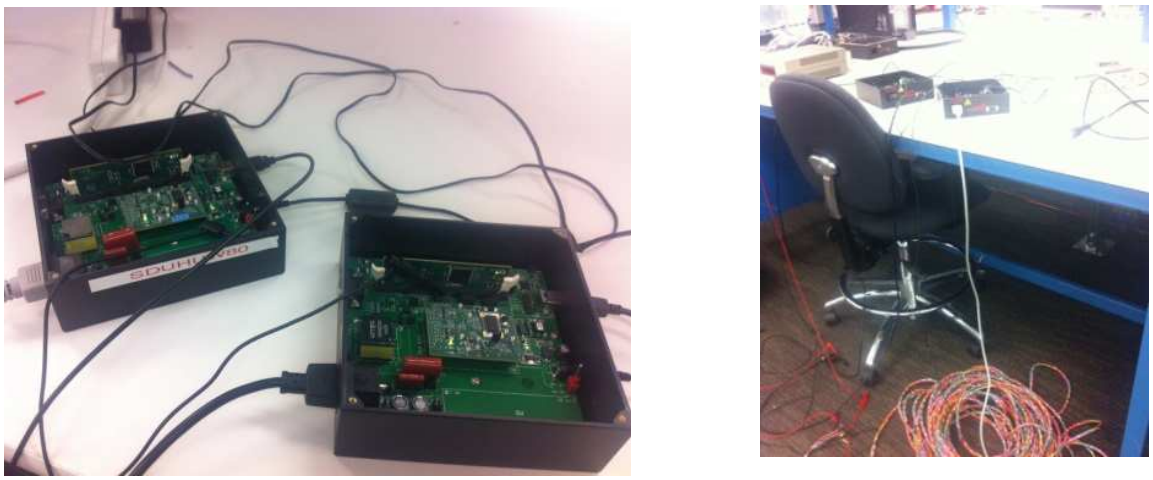


Figure 2-13. Cable Modeling Approach

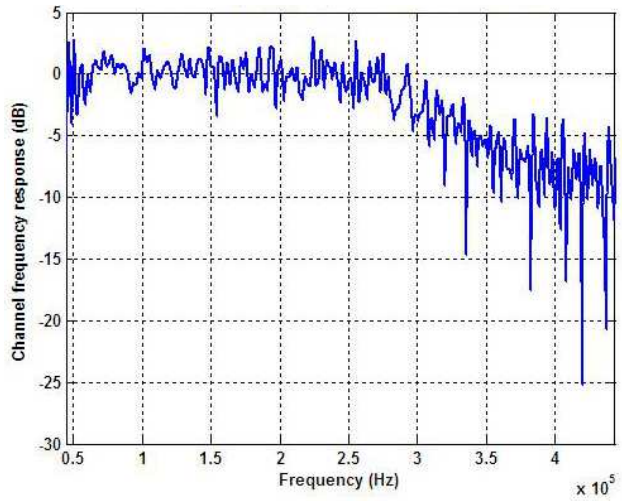


Figure 2-14. Channel-Frequency Response of 40-m Cable (Using Actual Cable)

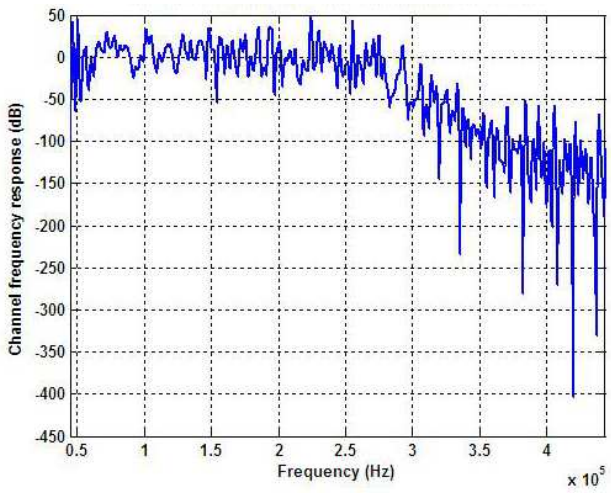


Figure 2-15. Channel-Frequency Response of 320-m Cable (Extrapolated)

The channel loss of the 320-m cable is not significantly more than the 40-m cable even up to 100 KHz as shown in Figure 2-14 and Figure 2-15.

The 40-m cable was then used with the DC-PLC hardware to collect the BER measurements across different AFE031 TX-amplitudes as shown in Figure 2-16. The software and firmware used to conduct BER testing is part of the PLC-Lite SDK and are not included in the demonstration software provided with this design.

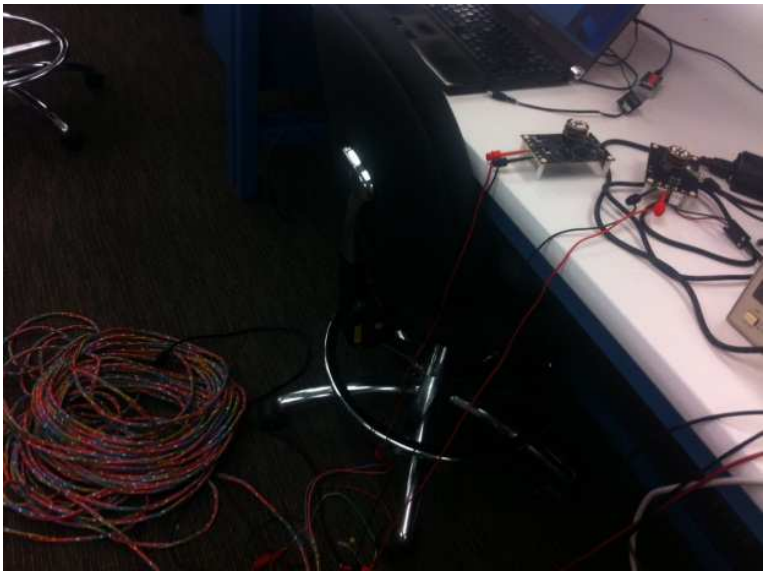


Figure 2-16. BER Measurement Using the 24-V DC PLC Hardware and the 40-m Cable

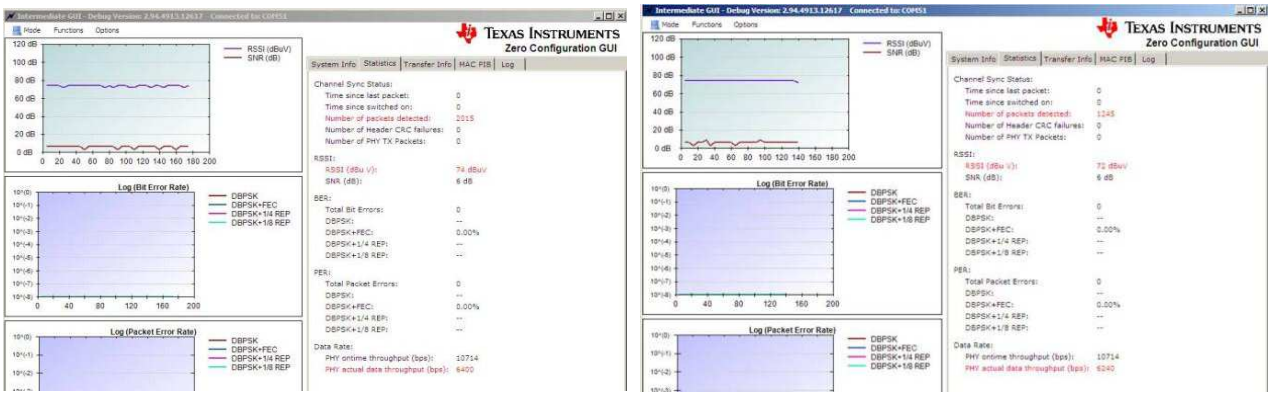


Figure 2-17. BER Data: No Packet Errors With Levels 5 and 6 (15 dB and 18 dB Below 15-V pp)

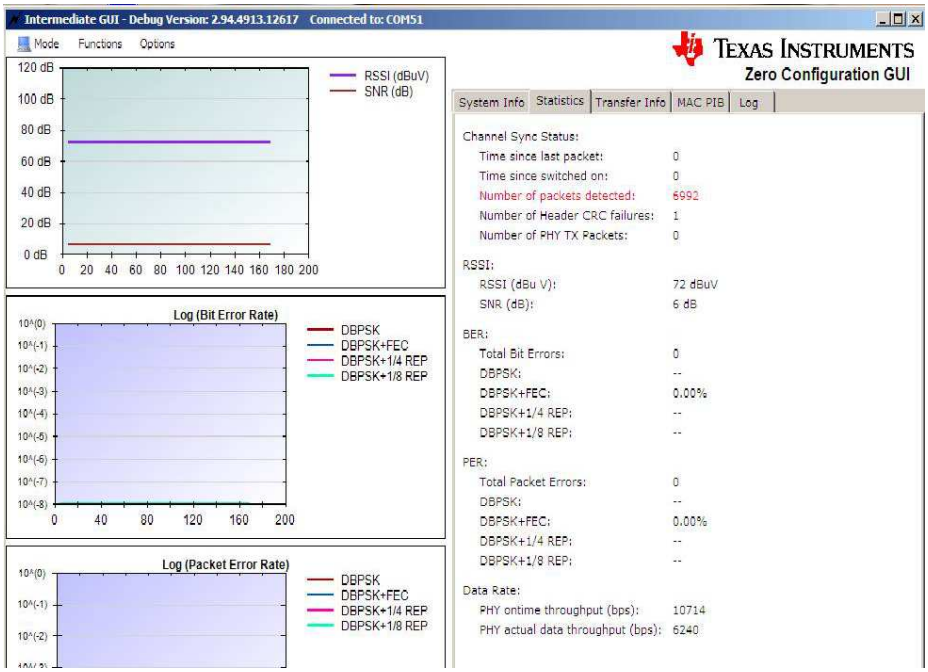


Figure 2-18. BER Data: No Packet Errors, Level 7 (21 dB Below 15-V pp)

Table 2-2. BER Measurement Results

TX AFE031 LEVEL	DECIBELS BELOW MAXIMUM AMPLITUDE	BER DATA
5	15 dB	0 packet error out of 10000 packets transmitted
6	18 dB	
7	21 dB	

The data listed in Table 2-2 confirms that the TI PLC-Lite solution with an OFDM solution can support cable length up to 320 m with a very-low TX amplitude of the AFE031 resulting in a large margin to support even longer cables.

2.5.1 Thermal Performance of the Design

To confirm the thermal performance of the design a simple test was performed. To perform the test, the power amplifier was programmed to send a PLC-modulation signal every 1 second. Thermal-imaging camera hot spots were analyzed at time (t0) and then 30 minutes after launching the application (t1). The purpose of this test is to confirm that the design can effectively dissipate heat without localized heating.

As shown in Figure 2-19 and Figure 2-20, there is no localized heating observed in the system after time, t1, compared to t0. For layout guidelines of the AFE031 device and high-current trace routing, see Section D.1.

NOTE: For the thermal-performance application testing, the TX setting for the AFE031 device was set to Level 3.

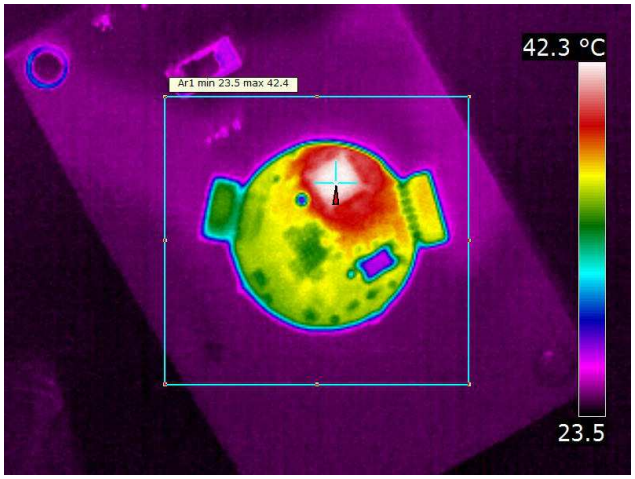


Figure 2-19. t0

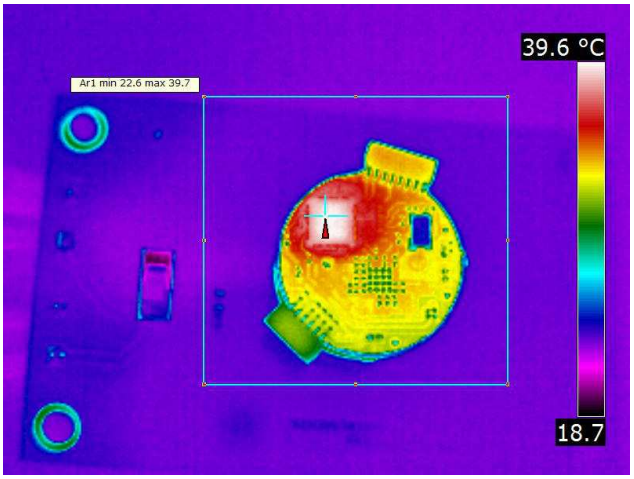


Figure 2-20. t1

2.6 IEC Electrostatic-Discharge Testing

The UART and JTAG interface pins on the SAT0022 processor section have IEC ESD-protection up to ±30-kV air, as well as ±30-kV contact which is provided by the TPD1E10B06 device from TI (see the product folder for more information, http://www.ti.com/product/tpd1e10b06). lists the device level-IEC ESD testing data.

Table 2-3. Device-Level IEC ESD Testing

LEVEL	IEC-CONTACT SPEC = ± 30 kV			IEC-AIR SPEC = ± 30 kV		
	UNIT1	UNIT2	UNIT3	UNIT1	UNIT2	UNIT3
±2 kV	PASS	PASS	PASS	PASS	PASS	PASS
±4 kV	PASS	PASS	PASS	PASS	PASS	PASS
±6 kV	PASS	PASS	PASS	PASS	PASS	PASS
±8 kV	PASS	PASS	PASS	PASS	PASS	PASS
±15 kV	PASS	PASS	PASS	PASS	PASS	PASS
±20 kV	PASS	PASS	PASS	PASS	PASS	PASS
±25 kV	PASS	PASS	PASS	PASS	PASS	PASS
±30 kV	PASS	PASS	PASS	PASS	PASS	PASS

Appendix A
TIDU168–October 2013

Schematics

The schematics are presented in the following order:

1. PLC Node
   - Power Section — SAT0021 (see Figure A-1)
   - C2000 and AFE031 — SAT0022 (see Figure A-2, and Figure A-3)
   - Application Board — SAT0023 (see Figure A-4)
2. USB to UART Board — SAT0045 (see Figure A-5)
3. Master Base Board — SAT0029 (see Figure A-6)
4. Slave Base Board — SAT0030 (see Figure A-7)
5. JTAG Programming Board — SAT0024 (see Figure A-8)

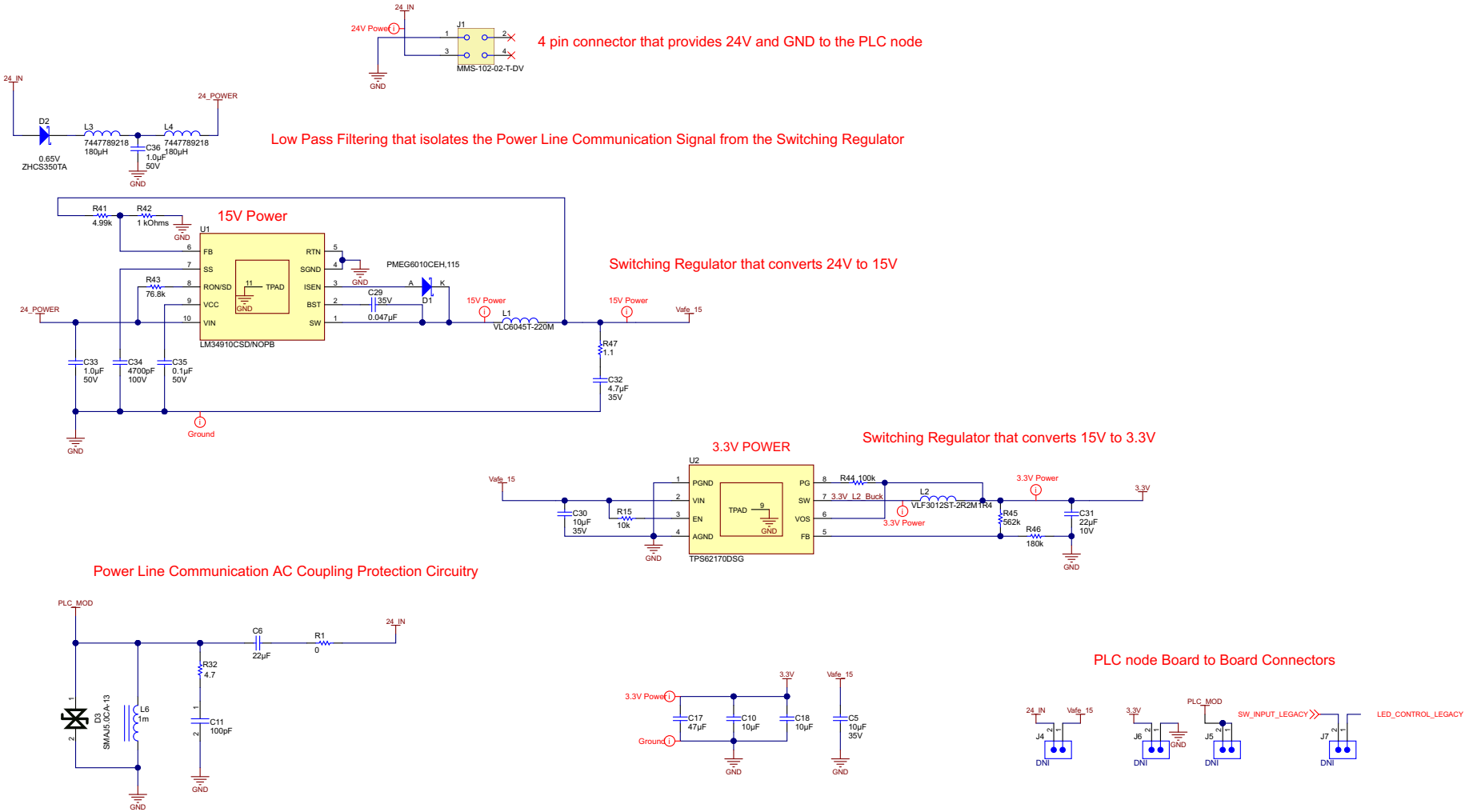


Figure A-1. SAT0021 — Power Section of the PLC Node

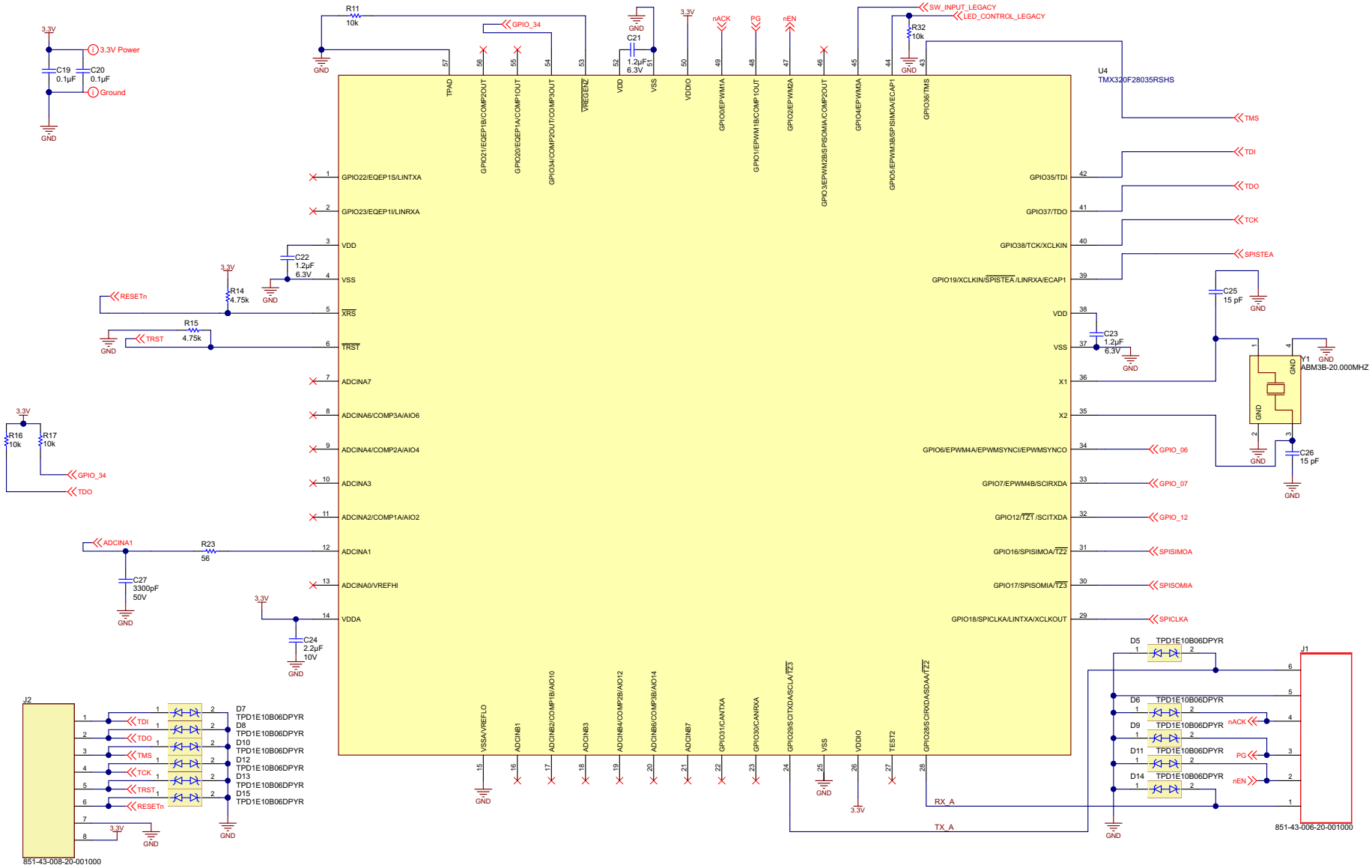


Figure A-2. SAT0022 — Processor Section of the PLC Node

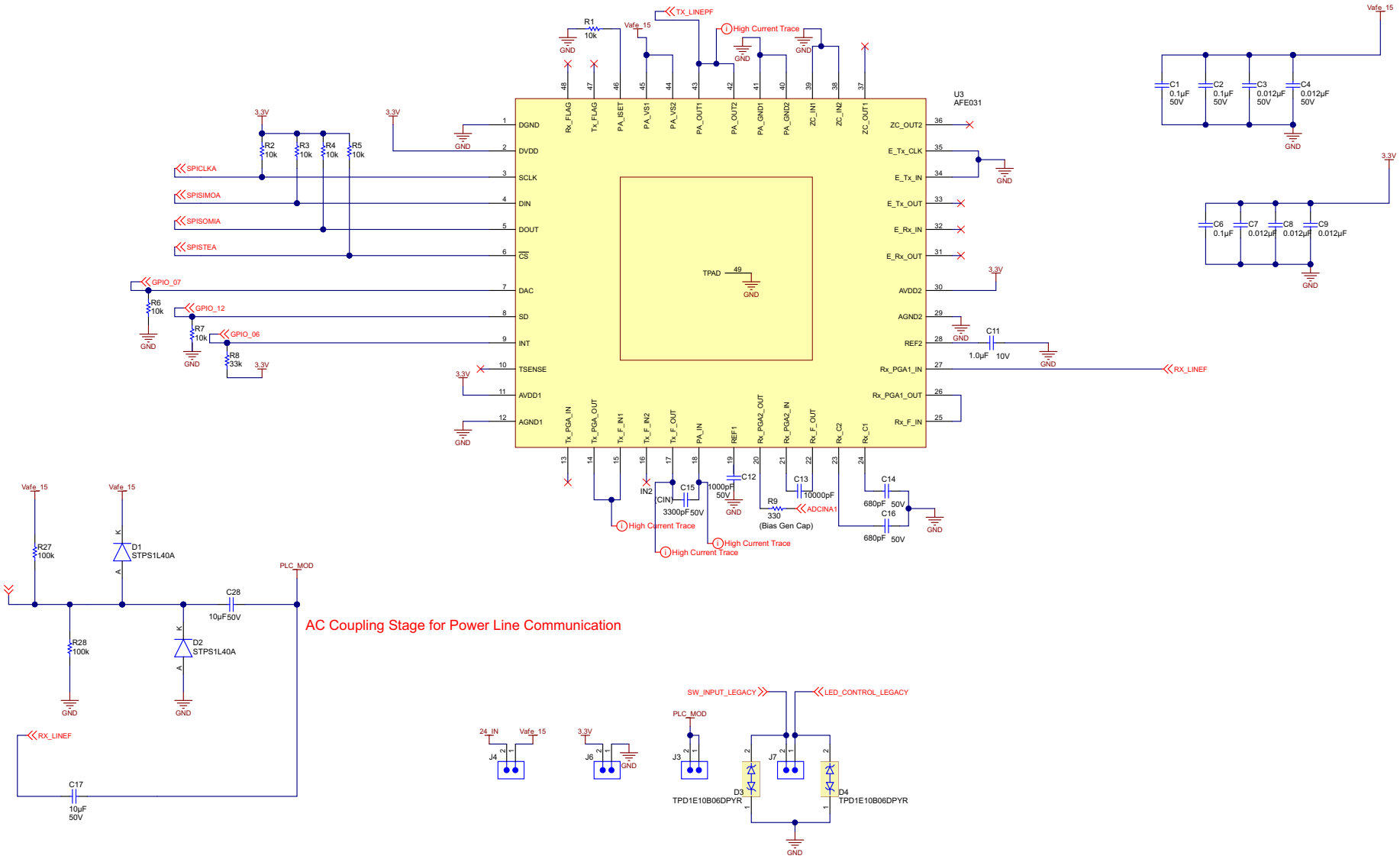


Figure A-3. SAT0022 — AFE Section of the PLC Node

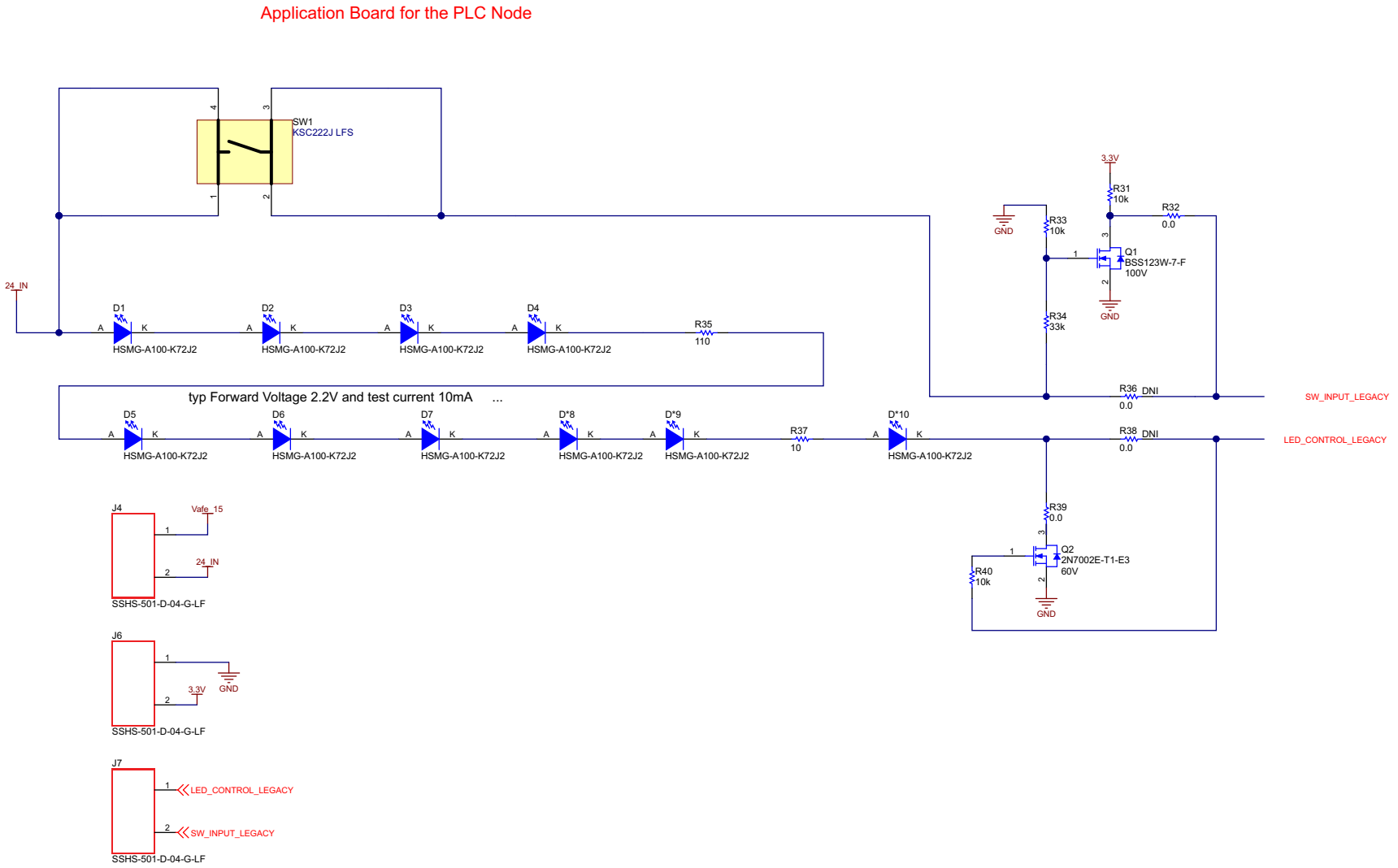


Figure A-4. SAT0023 — Application Section of the PLC Node

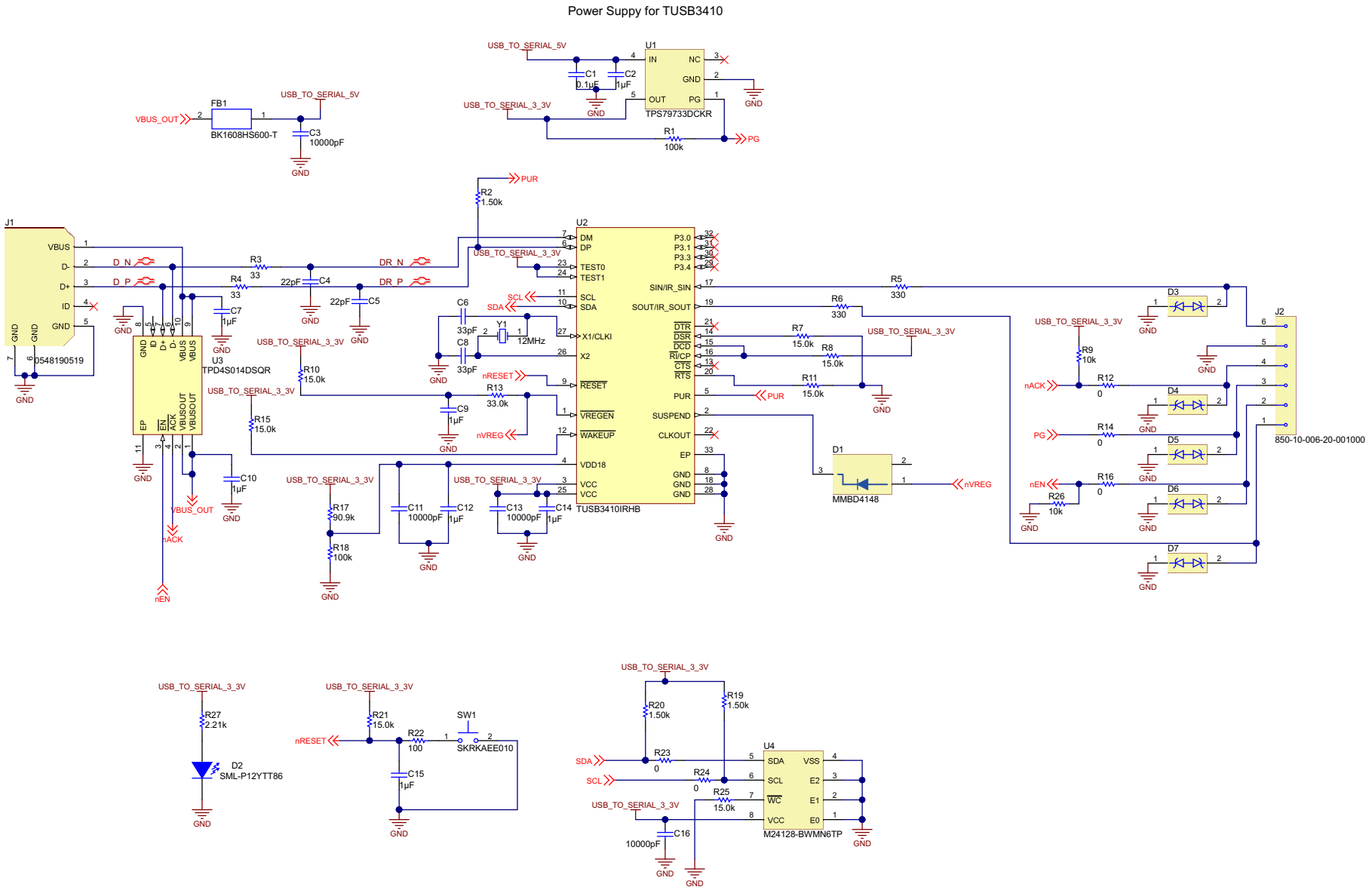
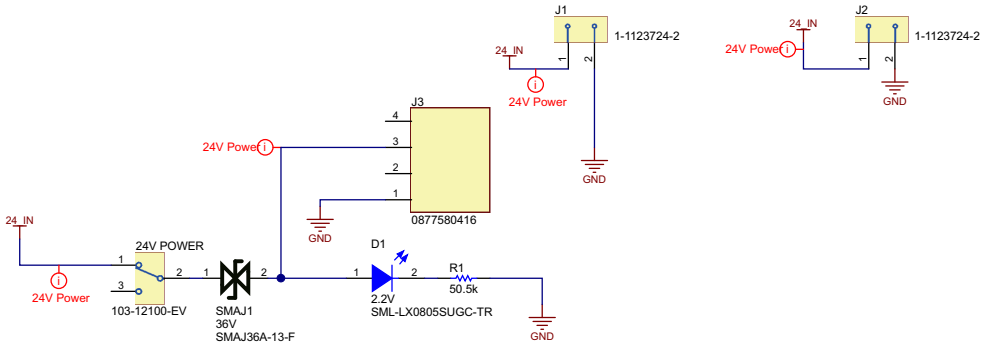
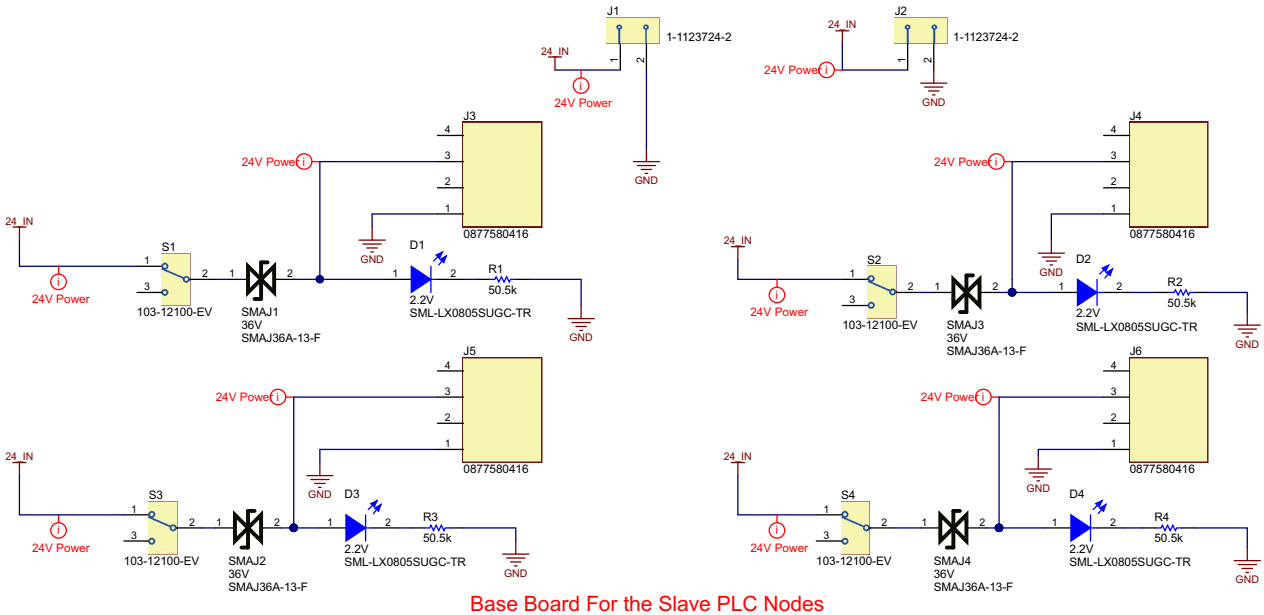


Figure A-5. SAT0045 — USB to UART Interface Board for Host-to-Master PLC-Node Communication



Base Board For the Master PLC Node

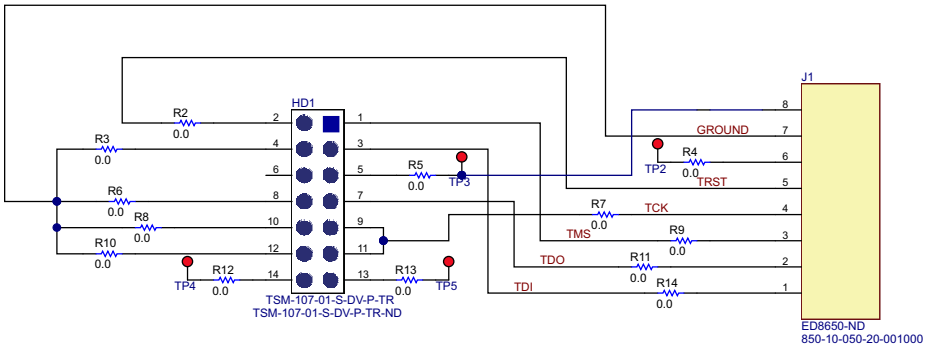
Figure A-6. SAT0029 — Base Board to Mount the Master PLC



Base Board For the Slave PLC Nodes

Figure A-7. SAT0030 — Base Board to Mount the Slave PLC Nodes

Interface Board that connects to the 8 pin connector (C2000 - processor) for JTAG programming



This board connects to the 8-pin connector (C200 processor) for JTAG.

Figure A-8. SAT0024 — JTAG Interface Board for Programming C2000

Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at www.ti.com/tool/24VDCPLCEVM. Figure B-1 shows the BOM for the SAT0022.

LINE NO.	KS PART NUMBER	CUSTOMER PART NUMBER	QTY	VALUE	DESIGNATORS	PKG/ CASE	T.COEFF/ PWR	TOL	VOLT RATED	DESCRIPTION	DISTRIBUTOR	DIST P/N	MANUFACTURER	MNFR. PART #	LOT NO
1	27513	B 14	2	0.012µF	C3, C4	0402	X7R	10	50V	Capacitors	Digi-Key	399-9949-1-ND	Murata	GRM155R71H123KA12D	K10000048010
2	27513	B 14	3	0.012µF	C7, C8, C9	0402	X7R	10	50V	Capacitors	Digi-Key	399-9949-1-ND	Murata	GRM155R71H123KA12D	K10000048010
3	22444	B 7	4	0.1µF	C1, C2, C19, C20	0402	X7R	10	50V	Capacitors	Digi-Key	445-5932-2-ND	Tdk Corporation	C1005X7R1H104K	K10000028604
4	12420	B 9	1	0.1µF	C6	0402	X7R	10	16V	Capacitors	Digi-Key	445-4952-2-ND	Tdk Corporation	C1005X7R1C104K	K10000049921
5	27514	B 14	1	1.0µF	C11	0402	X7S	10	10V	Capacitors	Digi-Key	445-9116-1-ND	Tdk Corporation	C1005X7S1A105K050BC	K10000048128
6	11116	B 1	1	10000pF	C13	0402	X7R	10	50V	Capacitors	Digi-Key	490-4516-2-ND	Murata Electronics North Am	GRM155R71H103KA88D	K10000049918
7	11296	B 1	1	1000pF	C12	0402	X7R	10	50V	Capacitors	Digi-Key	445-1256-2-ND	Tdk Corporation	C1005X7R1H102K	K10000032586
8	11229	B 1	2	15pF	C25, C26	0402	C0G	5	50V	Capacitors	Venkel	C0402COG500-150JNE	Venkel	C0402COG500-150JNE	OB6223AYV
9	11637	B 2	2	3300pF	C15, C27	0402	X7R	10	50V	Capacitors	Digi-Key	311-1034-2-ND	Venkel	C0402X7R500-332KNE	K10000034924
10	13093	B 3	2	680pF	C14, C16	0402	C0G	5	50V	Capacitors	Digi-Key	490-3240-2-ND	Murata	GRM1555C1H681JA01D	K10000011519
11	12509	C 4	1	2.2µF	C24	0603	X7R	10	10V	Capacitors	Digi-Key	445-5958-2-ND	Murata Electronics North Am	GRM188R71A225KE15D	K10000049081
12	27515	C 17	3	1.2µF	C21, C22, C23	0805	X7R	10	6.3V	Capacitors	Digi-Key	399-4929-1-ND	Kemet	C0805C125K9RACTU	K10000045794
13	24690	E 4	2	10µF	C17, C28	1206	X5R	10	50V	Capacitors	Digi-Key	445-5998-2-ND	Tdk Corporation	C3216X5R1H106K	K10000044076
14	27535	U 179	1	TMX320F28035RSHS	U4	56-VFQFN				Integrated Circuits	Mouser	595-TMS320F28035RSHT	Texas Instruments	TMX320F28035RSHS	K10000049505
15	14220	M 14	11	10.0K	R1, R2, R3, R4, R5, R6, R7, R11, R16, R17, R32	0402	1/10W	1		Resistors	Digi-Key	P10.0KLTR-ND	Yageo America	ERJ-2RKF1002	K10000048777
16	11016	M 1	2	100K	R27, R28	0402	1/16W	1		Resistors	Digi-Key	311-100KLRTR-ND	Yageo America	RC0402FR-07100KL	K10000045631
17	11322	M 4	1	33.2K	R8	0402	1/16W	1	50V	Resistors	Digi-Key	P33.2KLTR-ND	Panasonic - Ecg	ERJ-2RKF3322X	510283380
18	21035	M 24	1	330	R9	0402	±100ppm/°C	1	1/10W	Resistors	Digi-Key	P330LTR-ND	Panasonic - Ecg	ERJ-2RKF3300X	K10000049592
19	28777		2	4.75K	R14, R15	0402	1/16W	0.1		Resistors			Panasonic - Ecg	ERA-2AEB4751X	
20	13137	M 11	1	56.2	R23	0402	1/16W	1	75V	Resistors	Digi-Key	P56.2LTR-ND	Panasonic - Ecg	ERJ-2RKF56R2X	7121255502
21	24301	X 8	13	TPD1E10B06DPY	D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15	0402			6.0V	Circuit Protection	Texas Instruments	TPD1E10B06DPYR	Texas Instruments	TPD1E10B06DPY	K10000042224
22	27533	AE 41	2	STPS1L40A	D1, D2	DO-214AC, SMA	1A		40V	Discrete Semiconductor Products	Digi-Key	497-3753-1-ND	Stmicroelectronics	STPS1L40A	K10000048127
23	27534	U 175	1	AFE031AIRGZT	U3	48-VQFN				Integrated Circuits	Texas Instruments	AFE031AIRGZT	Texas Instruments	AFE031AIRGZT	K10000045657
24	27536	W 13	1	20.0000MHz	Y1	4-SMD 5mm x 3.2mm	-20°C ~ 70°C	20	18pF	Crystals	Digi-Key	535-9125-1-ND	Abracon Corporation	ABM3B-20.000MHZ-B2-T	K10000049524
25	20983-6	AM 78/LB 12	1	1 X 6 R/A	J1	0.05"				Connectors	Digi-Key	851-43-010-20-001000	Mill-Max	851-43-010-20-001000	K10000044132
26	20983-8	AM 78/LB 12	1	1 X 8 R/A	J2	0.05"				Connectors	Digi-Key	851-43-010-20-001000	Mill-Max	851-43-010-20-001000	K10000044132
27	26194	AM 88	4	FW-50-01-L-D	J3, J4, J6, J7	0.05"				Connectors	Samtec	FW-50-01-L-D-300-280	Samtec	FW-50-01-L-D-300-280	K10000041242

Figure B-1. SAT0022 — BOM

Layer Plots

To download the layer plots for each board, see the design files at www.ti.com/tool/24VDCPLCEVM. Figure C-2, Figure C-2, and Figure C-3 show the layer plots for the SAT0021, SAT0022, and SAT0023 respectively.

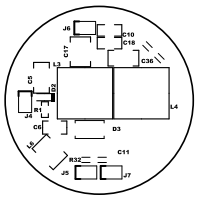


Figure C-1. SAT0021 — Layer Plot

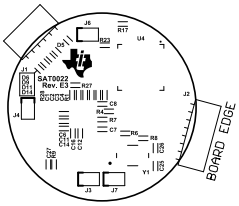


Figure C-2. SAT0022 — Layer Plot

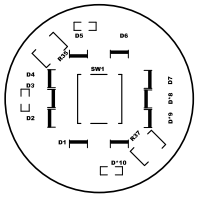


Figure C-3. SAT0023 — Layer Plot

Altium Project

To download the Altium project files for each board, see the design files at www.ti.com/tool/24VDCPLCEVM. Figure D-1, Figure D-2, and Figure D-3 show the layout for the SAT0021, SAT0022, and SAT0023 respectively.

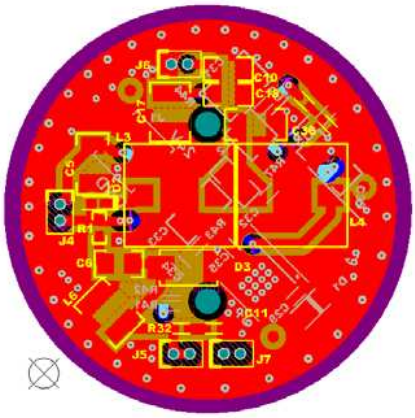


Figure D-1. SAT0021 — Layout

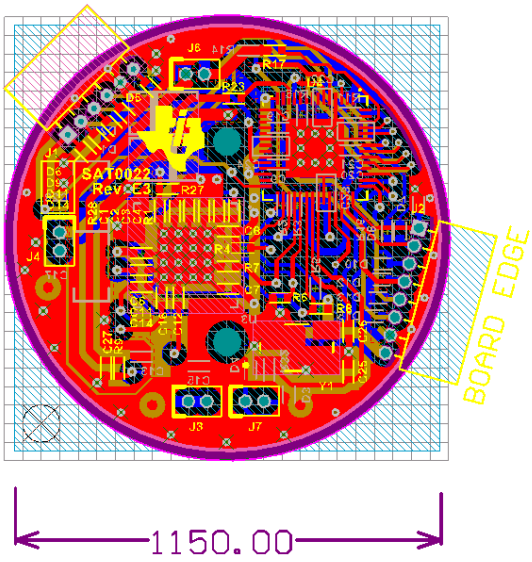


Figure D-2. SAT0022 — Layout

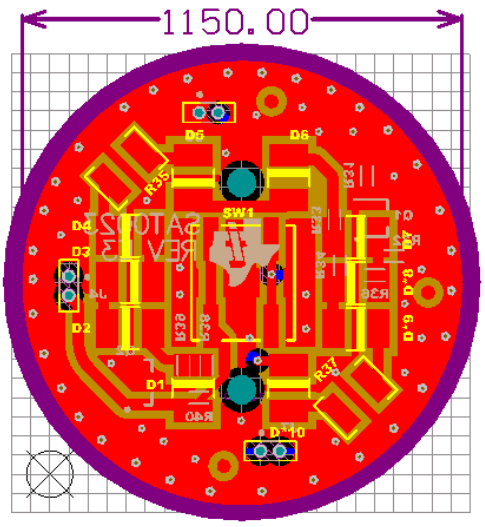


Figure D-3. SAT0023 — Layout

D.1 AFE031 High-Current Trace Layout

In a typical power-line communications application, the AFE031 device dissipates 2 W of power when transmitting into the low impedance of the AC line. This amount of power dissipation can increase the junction temperature. An increase in junction temperature can lead to a thermal overload that results in signal transmission interruptions if the proper thermal design of the PCB has not been performed. Proper management of heat flow from the AFE031 device as well as good PCB design and construction are required to ensure proper device temperature, maximize performance, and extend device operating life.

For a layout example of high-current traces see Figure D-4. To achieve lower thermal resistance, 2-oz copper was used in the design as shown in Figure D-5.

NOTE: The AFE031 device has a power amplifier that requires high-current trace layout.

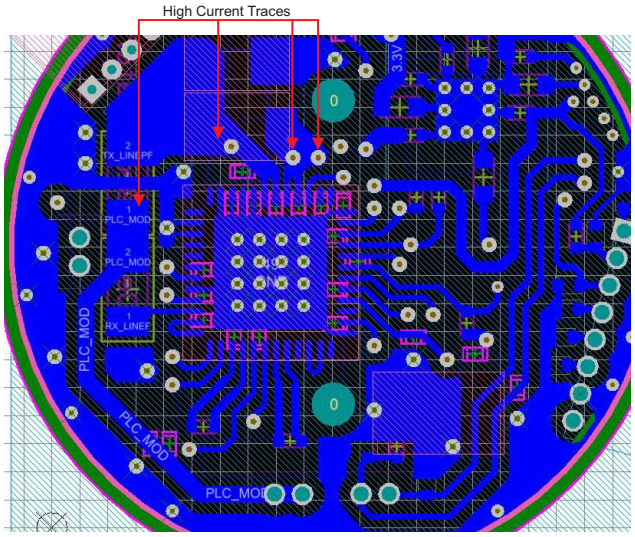


Figure D-4. High-Current Traces

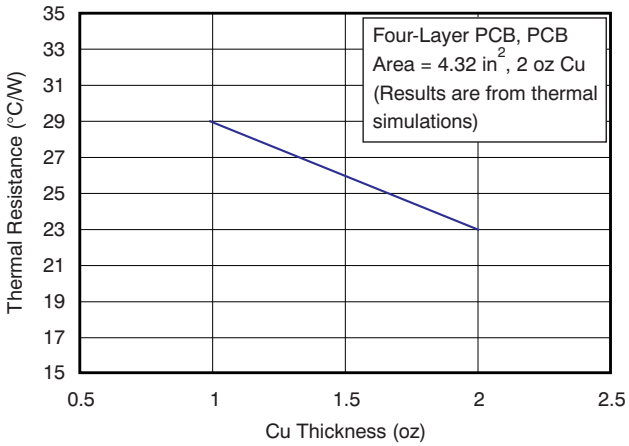


Figure D-5. AFE031 — Thermal Resistance as a Function of Copper Thickness

See Section 2.5.1 for thermal performance data of the design when the application software is running.

Appendix E
TIDU168–October 2013

Gerber Files

To download the Gerber files for each board, see the design files at www.ti.com/tool/24VDCPLCEVM

Appendix F
TIDU168–October 2013

Software Files

To download the software files for the reference design, see the design files at www.ti.com/tool/24VDCPLCEVM

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