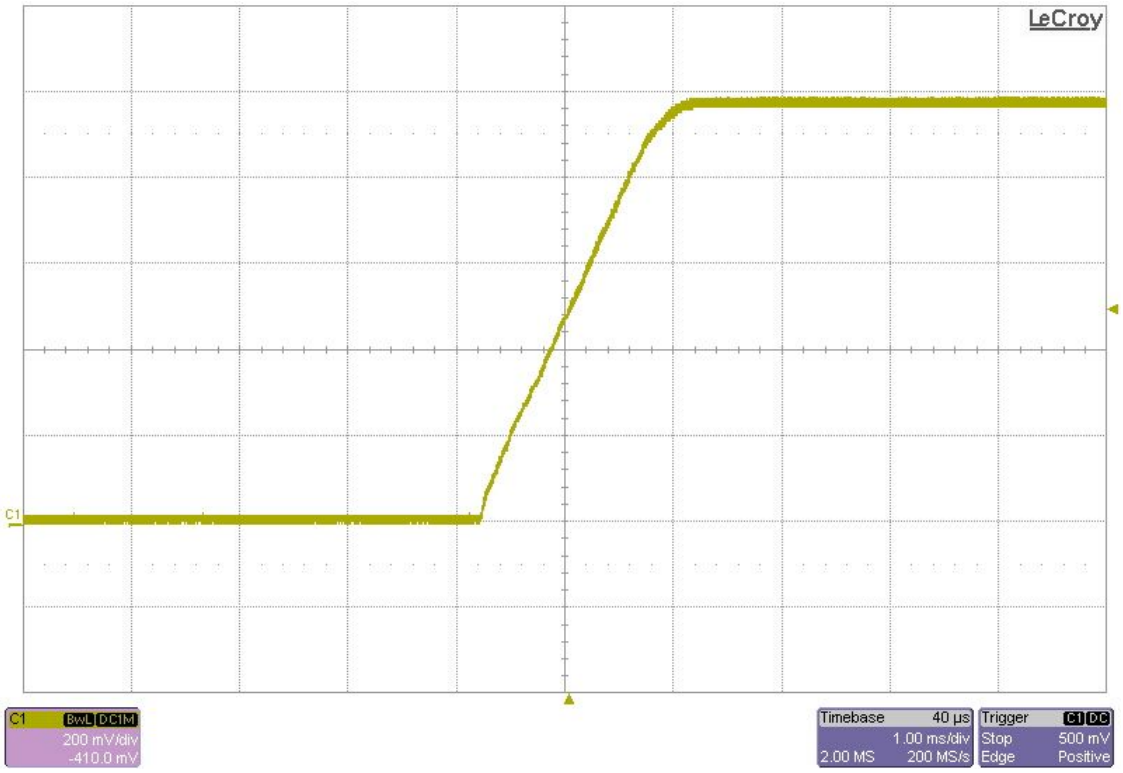
PMP7256 Test Results

Abstract:

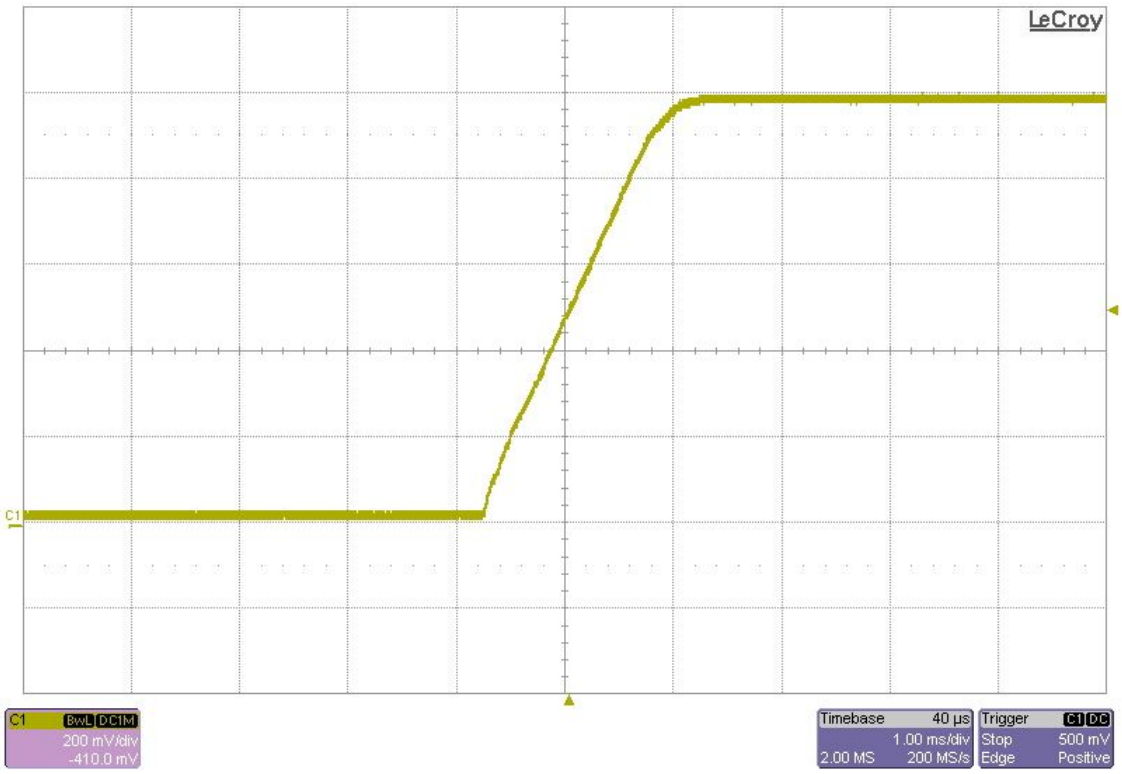
All the equations used to calculate component values in the PMP7256 design are located in the “Design Procedures” section of the TPS56121 Datasheet. The datasheet of the LM10010 details how to design the feedback network of the system.

1 Startup

Input voltage = 12V
Output voltage = 1V
Load current = 5A

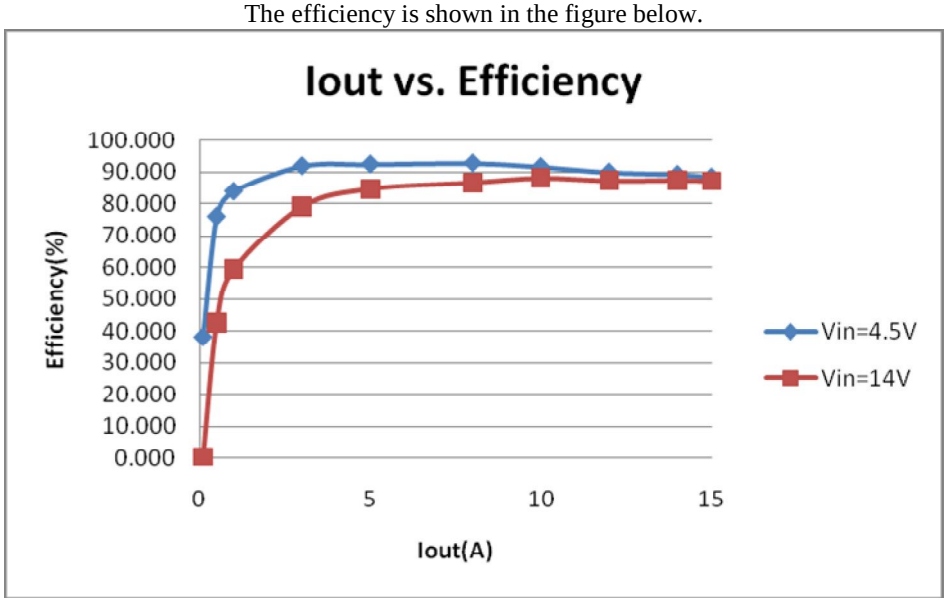


Input voltage = 12V
Output voltage = 1V
Load current = 0A



2 Efficiency

The efficiency is shown in the figure below.



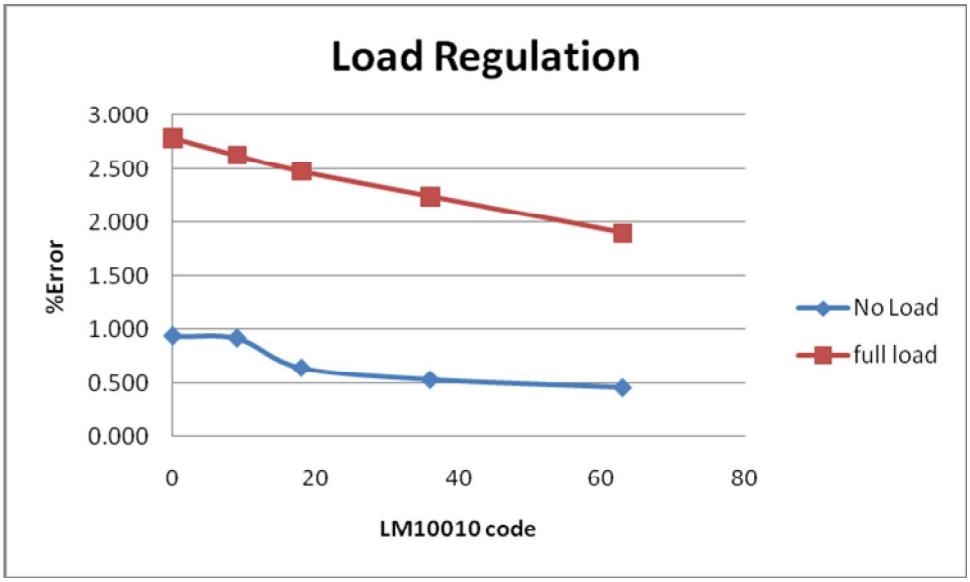
Vin(V)	Iin(A)	Vout(V)	Iout(A)	Efficiency(%)
4.5	0.058	0.999	0.1	38.276
4.5	0.146	0.998	0.5	75.951
4.5	0.264	0.996	1	83.838
4.5	0.719	0.991	3	91.887
4.5	1.189	0.989	5	92.421
4.5	1.888	0.985	8	92.750
4.5	2.384	0.983	10	91.629
4.5	2.91	0.981	12	89.897
4.5	3.415	0.979	14	89.188
4.5	3.694	0.979	15	88.341

Vin(V)	Iin(A)	Vout(V)	Iout(A)	Efficiency(%)
14	0.054	0.994	0.1	0.581
14	0.083	0.993	0.5	42.728
14	0.119	0.99	1	59.424
14	0.268	0.989	3	79.078
14	0.417	0.988	5	84.618
14	0.651	0.987	8	86.636
14	0.8	0.986	10	88.036
14	0.967	0.984	12	87.221
14	1.125	0.983	14	87.378
14	1.209	0.983	15	87.114

3 Load Regulation (DC Accuracy with LM10010)

The max error that can be tolerated in terms of Vout on the DSP was given to be 5%. The goal of the design was to keep the DC error to a max 2.5%, in order to allow for room to compensate for the AC error.
There are 4 main contributors to the final error seen on the output. They are: the error caused by the LM10010 (2%max), feedback voltage error, the error of resistors in the feedback network, and the load regulation error from the IC. If the compilation of these errors are more than the targeted 2.5%, they can be decreased by using higher precision resistors(.1% or .5%), choosing an IC to minimize the feedback voltage error as well as the load regulation error, and to use the LM10010.
Below shows the total DC error seen on the output of the PMP7256. The expected output voltage was calculated using the spreadsheet titled “LM10010_Error_Analysis_locked.xlsx”. Please add the load regulation error to the “feedback Voltage error” input. The feedback network resistors were doubled in value and put in parallel to reduce the feedback error of the system. The resistors were precise to 1%. The IC,

TPS56121, has a max load regulation error of 0.5% and a feedback voltage error of 1%.The load regulation of the output is shown in the graph below.



	LM10010 Code	Expected output voltage	Vout_act (no load)	%ERROR (No load)	Vout_act (full load)	%ERROR (Full load)
VIDA,B,C=0	0	0.703	0.696	0.939	0.683	2.790
VIDA=1	9	0.761	0.754	0.920	0.741	2.628
VIDB=1	18	0.819	0.814	0.647	0.799	2.478
VIDC=1	36	0.936	0.931	0.534	0.915	2.244
VIDA,B,C=1	63	1.111	1.106	0.459	1.090	1.899

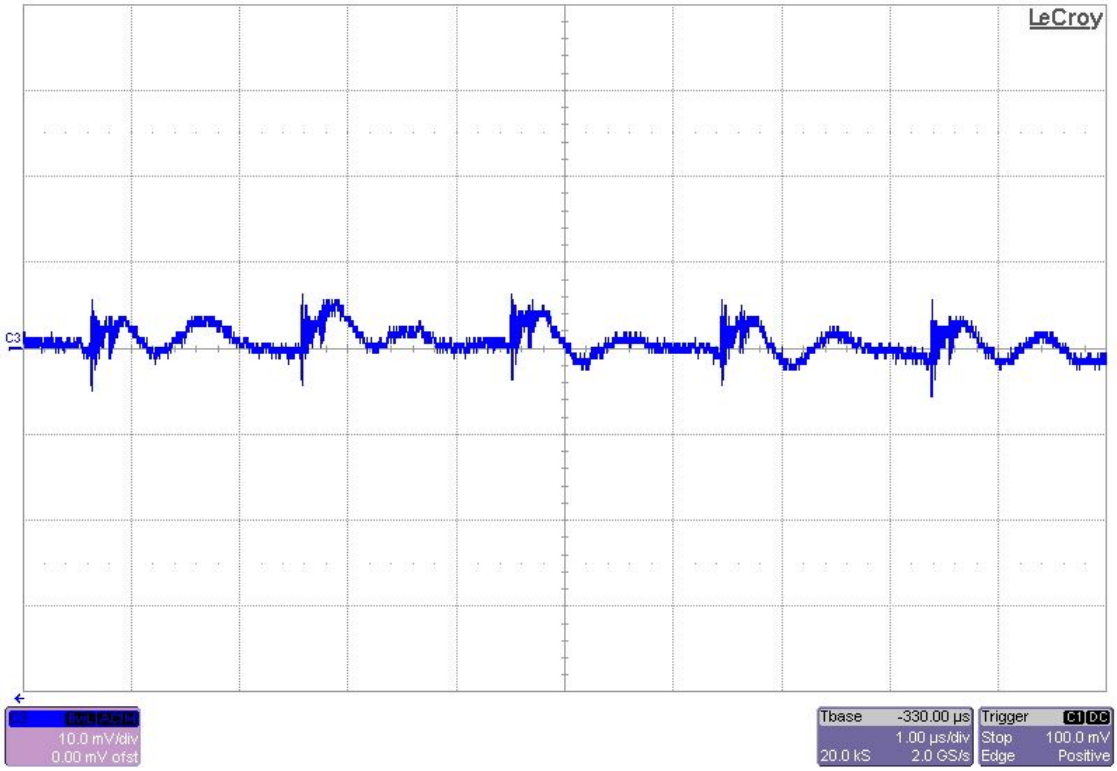
Various VID codes (column 2) were used as input to the LM10010. Vout was measured with no load(Vout_act(no load)) and at full load (Vout_act (full load)) to show the load regulation error. Percent error shows the difference between the expected output voltage and the measured output voltage, both at no load and full load.

4 Output Ripple Voltage

The output ripple voltage is shown in the figure below. Channel 2 is the switch node waveform and Ch1 is the Vout ripple.

Input voltage = 12V
Output voltage = 1V
Load current = 15A

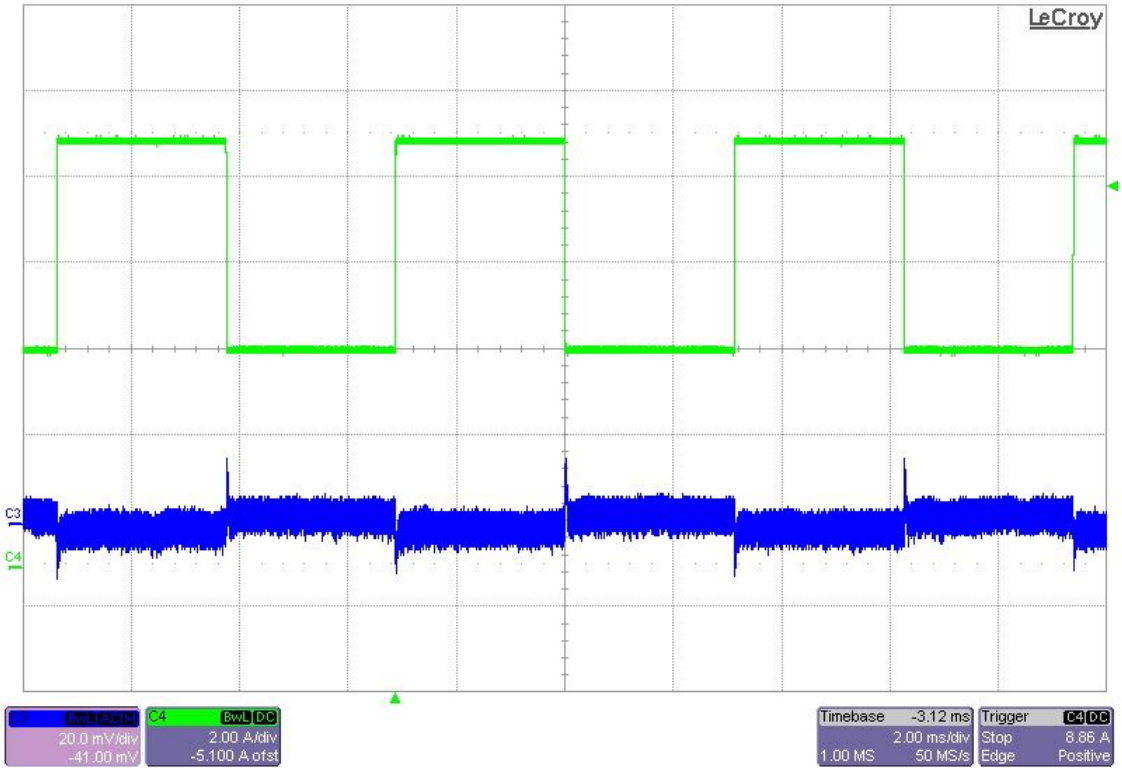
PMP7256 Test Results

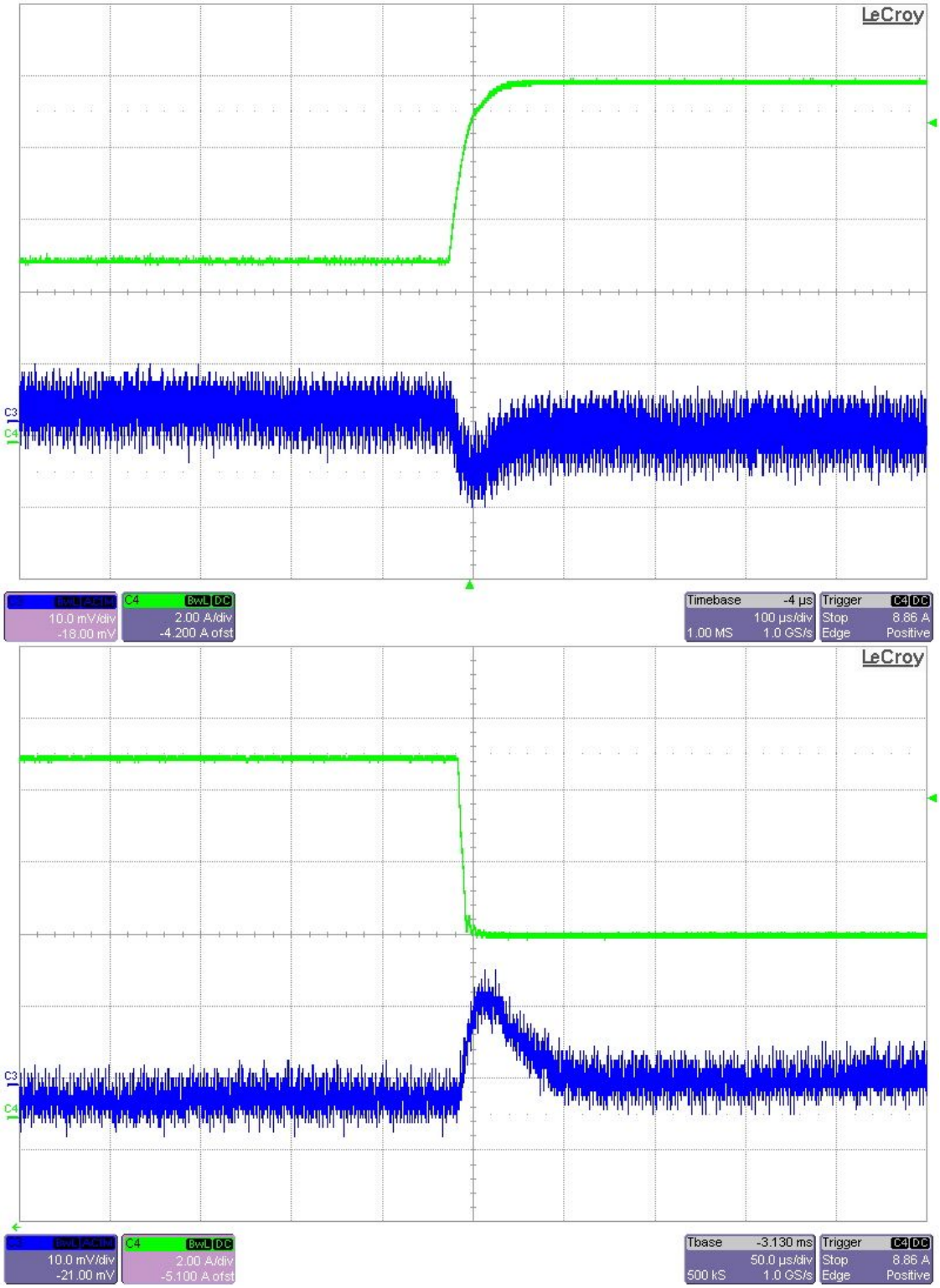


5 Load Transients

The figures below show output response to load transients. The input voltage was set to 12V.

Channel 1 : Vout (AC coupled)
Channel 4 : Load current

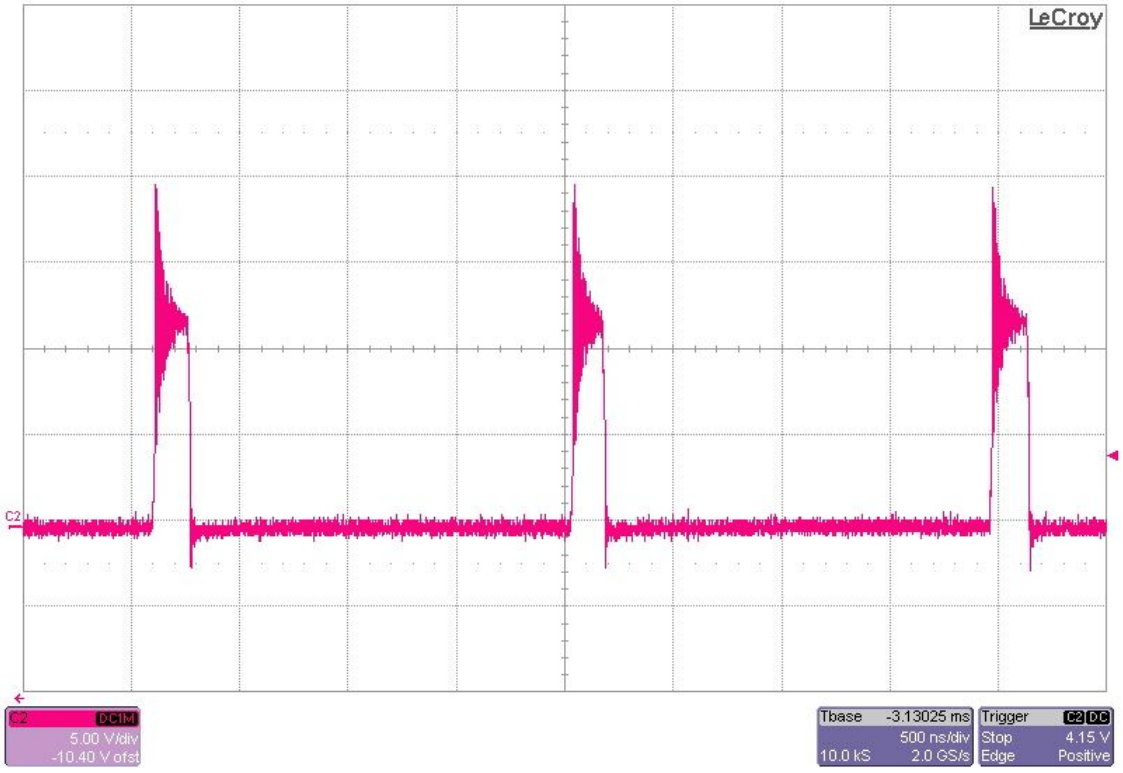



LeCroy
C3
C4
10.0 mV/div
-18.00 mV
C4 BwL DC
2.00 A/div
-4.200 A ofst
Timebase -4 µs
100 µs/div
1.00 MS 1.0 GS/s
Trigger C4 DC
Stop 8.86 A
Edge Positive
LeCroy
C3
C4
10.0 mV/div
-21.00 mV
C4 BwL DC
2.00 A/div
-5.100 A ofst
Tbase -3.130 ms
50.0 µs/div
500 kS 1.0 GS/s
Trigger C4 DC
Stop 8.86 A
Edge Positive

6 Switch Node Waveforms

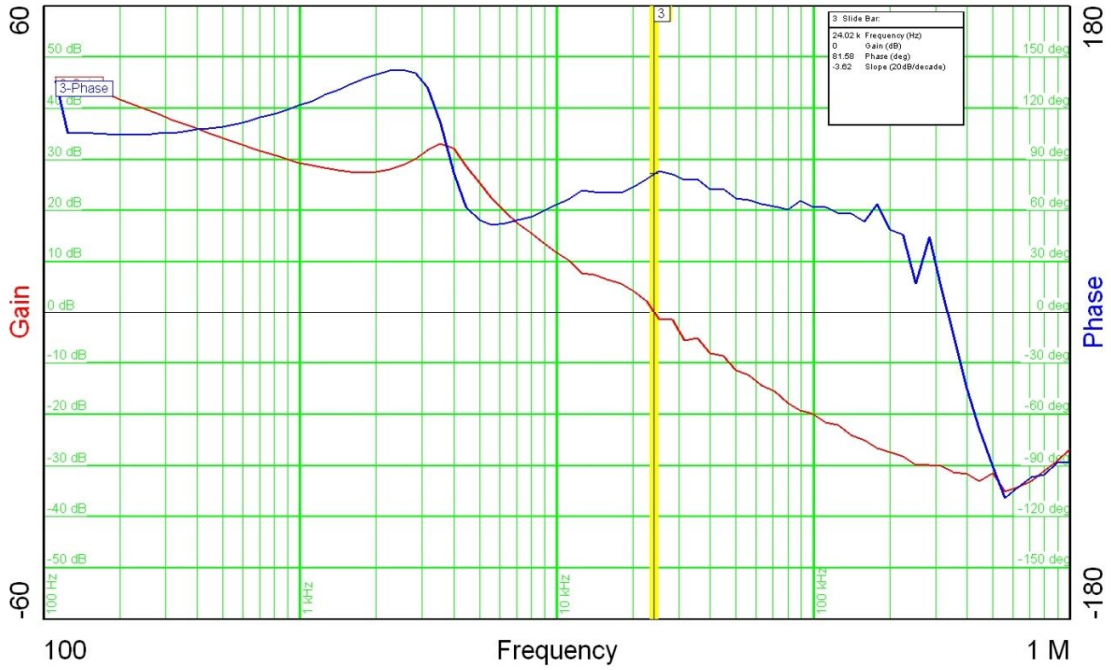
The following figures show the full bandwidth switch node waveforms at:

Input voltage = 12V
Output voltage = 1V
Load current = 15A(full BW)



7 Control Loop Frequency Response

Input voltage = 12VDC
Output voltage = 1V
Load current = 15A
Phase margin = 81.58°
Bandwidth = 24.02kHz



8 Thermal Analysis

The images below show the infrared images taken from the FlexCam after 10min at full load (1.1V@15A). Input voltage = 12 VDC

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