Analog Application Note

AAN-16

CEB1307/CEB1308 Evaluation Board User Guide for CDK1307/CDK1308 Analog-to-Digital Converters

A New Direction in Mixed-Signal

REQUIRED EQUIPMENT

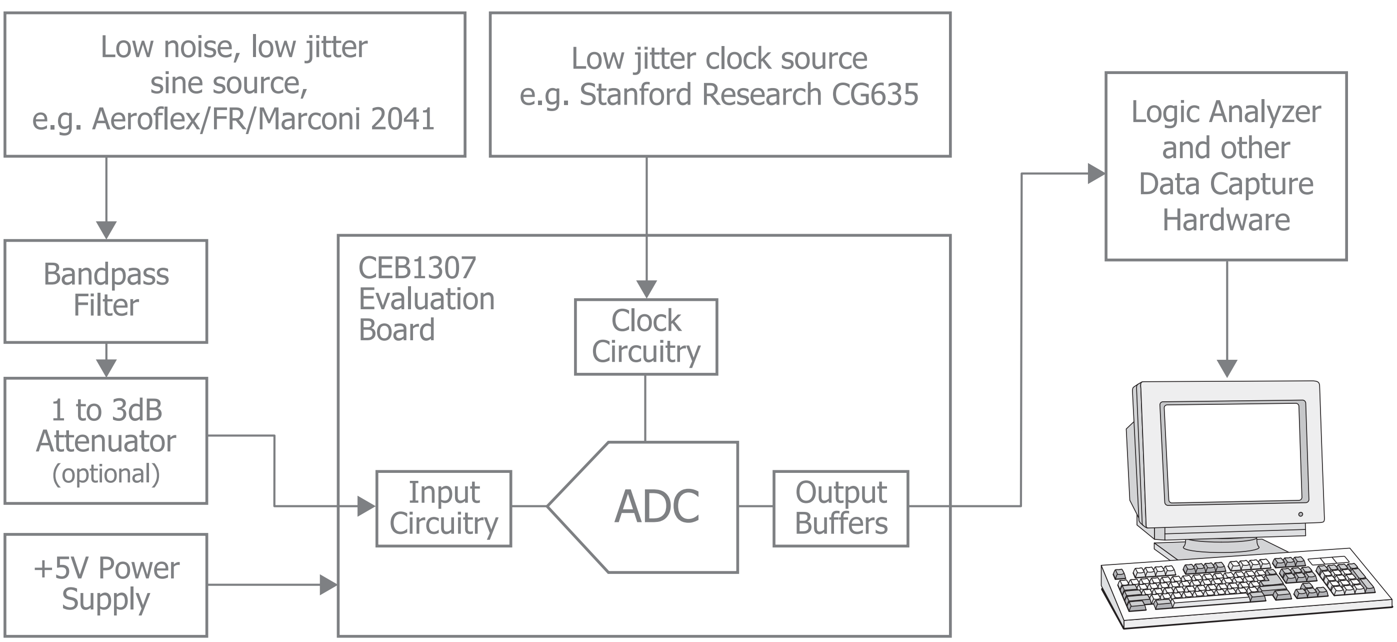
- CDK1307 or CDK1308 datasheet
- Analog high performance signal source
- Antialiasing filter
- Logic analyzer or other data capture hardware
- Lab power supply, +5V fixed or adjustable
- Low jitter clock source

Product Description

The CEB1307 / CEB1308 Evaluation Board is an evaluation platform for the CDK1307x and CDK1308x families of Analog-to-Digital converters (ADC). The board contains The ADC chip, clock circuitry, output signal buffering, control signal interface, and input signal conditioning circuitry. The board is easily set up for standard ADC performance tests.

The evaluation board is configured to interface with commonly used test equipment. Several options are implemented for clock, input signal, and output signal formatting. These options can be selected by replacing some components on the PCB.

Test Setup Block Diagram



This device can be damaged by ESD. Even though this product is protected with state-of-the-art ESD protection circuitry, damage may occur if the device is not handled with appropriate precautions. ESD damage may range from device failure to performance degradation. Analog circuitry may be more susceptible to damage as very small parametric changes can result in specification incompliance.

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Quick Start Guide

The Evaluation Board is configured and tested for the following conditions during manufacturing.

- CMOS clock input
- Transformer coupled input signal. Optimized for 8MHz input signal frequency
- 2.5V CMOS output data format
- Single +5V supply with on-board regulators for each power domain

The following procedure describes how to initialize measurements for these conditions. Details on how the board can be modified for other conditions are described in later sections of this document.

1. Find the ADC data sheet and check functionality and description of each pin.
2. Connect +5V and ground to JP10 (upper left corner as indicated on the PCB. (The other pins on JP10 are used only if external supply is selected with JP3.)
3. Measure supply voltage on the wide pin of U1 (typ 2.5V), U11 (typ 1.8V) and U4 (typ 2.5V). Adjust with adjacent potmeters if necessary or if other voltages are desired. The voltages at U1 and U4 should be equal.
4. Check that a jumper is present at JP2 in the "rightmost" position.
5. Check that a jumper is present at JP12 in the "leftmost" position enabling debouncer circuits for the control bits.
6. Check that jumpers are applied to JP1 (not JP3) to select power supply from regulators.
7. Check that jumpers are applied to JP8 and JP9 to set ADC control signals. A jumper on JP8 corresponds to "0". A jumper on JP9 corresponds to "1". Apply jumpers on JP8 for all bits except 1, 2 and 6 where jumpers should be on JP9. Each bit corresponds to ADC control signals as shown in the list on the PCB.
8. Check that jumper is applied to JP11 in "top" position (INT_VDD) to select power supply from regulators.
9. Apply clock signal to input X6 ("CLK"). Use CMOS levels. Max voltage should be equal to the supply voltage set on U1. See detailed instructions in the Clock Generation section if other logic formats are desired.
10. Perform "reset" of the ADC by placing it in Power Down. This is done by moving jumper JP9 bit 1 from JP9 to JP8 and back to JP9. This corresponds to applying a "1-0-1" sequence on the PD_N pin
11. Apply input signals to X1. Note that high performance (low noise and low phase noise) sources must be used together with bandpass filters. This is necessary to obtain sufficiently low noise and harmonic distortion. 1 to 3dB attenuators can also be used between the filter and the evaluation board. This will reduce the problem of impedance mismatch between the evaluation board and the cable. Such mismatch will result in reflections and would significantly impact both harmonic distortion and noise.
12. It is necessary to mount the filter as close to X1 and X2 as possible. Use maximum 5cm/2 inch cable length. See the Analog Inputs section for details.

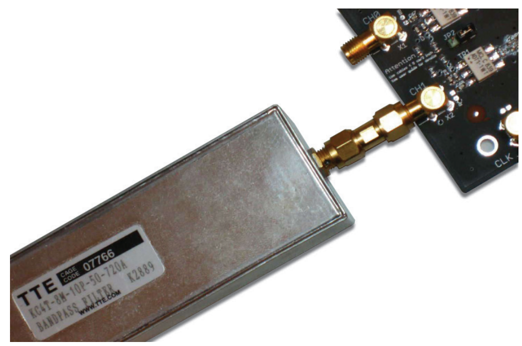

Figure 1: Recommended Connection of Filter

13. Connect a data capture unit to JP5 to capture ADC output data. Output data are in CMOS format with high-level determined by the voltage set by U4. The voltage of U1 and U4 should be set relatively equal to avoid translation problems between the ADC chip and output buffers. The pinout of JP5 is shown in section Digital Outputs. For 10-bit ADCs (CDK1308) the data will be aligned with MSB and the 3 LSB bits are tied low.

Analog Input

The quality of the input signals is the most important criterion to obtain good measurement results. The following points must be taken into consideration.

- Select a signal source with low noise and low phase noise. Excellent results are obtained with the Aeroflex/IFR/Marconi 2041.
- Apply bandpass filters between the signal source and

the Evaluation Board. This is required to obtain sufficiently low white noise levels and to reduce harmonic components from the signal source. Excellent results have been obtained with the TTE (www.tte.com) filter series Q56T or KC4T. Make sure that large magnetic cores are used in the filters to avoid nonlinearity due to core saturation. Alternative vendors are K&L Microwave (www.klmicrowave.com) and Allen Avionics Inc. (www.allenavionics.com). The input signal after filtering could be checked with a spectrum analyzer to ensure that noise and harmonic levels are significantly better than the theoretical contribution from the ADC.

- Make sure that the bandpass filter is mounted as close to the input connectors as possible. Using the connection in Figure 1 has proven to yield the best results over a wide range of sampling rates and input signal frequencies. However, when configuring the evaluation board to use the amplifier input option to drive the ADC, the cable length is not critical, and consistent performance is much easier obtainable.
- The input network on this PCB is optimized for fast settling. Hence there are no capacitors to attenuate the kickback from the ADC input. This has proven to yield the best results over a wide range of input and sampling frequencies as long as the filter is mounted close to the input connector. However, if a cable is used between the board and filter, the kickback will travel over the cable, be reflected in the filter and add an error component to the signal causing severe harmonic distortion.
- The input of the Evaluation Board assumes a 50Ω source. However, with filters, transformers and cables it is hard to ensure impedances of 50Ω for a wide frequency range. In addition, the sampling capacitor of the ADC must be charged for each clock cycle. This results in a kickback into the transformer that will propagate back into the filter. Such reflections may severely impact performance.
- The input network can be optimized if a long cable is required between the filter and the board input. The configuration in Figure 2 is designed to attenuate the kickback from the ADC and to provide an input impedance that looks as resistive as possible for frequencies below Nyquist. Values of the series inductor will however depend on board design and conversion rate. In some instances a shunt capacitor in parallel with the termination resistor (e.g. 33pF) may improve results. However, the impedance match may become worse.

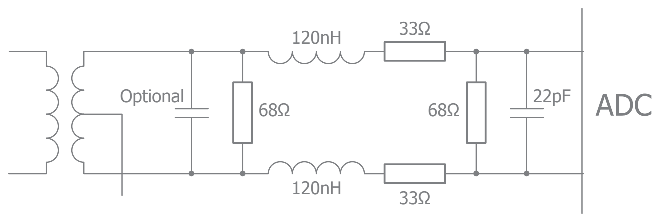

Figure 2: Alternative Input Network

- To reduce the problems of reflections, an attenuator can be added between the filter and the Evaluation Board. Best performance is obtained with 3 to 6dB attenuators (or even a 50Ω termination). It might however be hard to get sufficient signal level into the ADC in such case. Using 1 to 3dB attenuators may be a good tradeoff.

The ADC performance is optimized by applying a differential signal to the analog inputs. The Evaluation Board has two options to convert the input signal to differential. The transformer TR0 is configured to convert the input signal to differential with the common mode voltage set by the center tap. In addition a differential amplifier can be selected by re-configuring resistors on the board. The amplifier allows for good performance from DC to approximately 20MHz depending on linearity requirements. The transformer can be used for frequencies from 2MHz and up.

To change from transformer to amplifier (located at the back of the board) the following modifications must be performed. Note that the SNR and SNDR will be slightly reduced when using an amplifier due to the noise contribution from the amplifier

- Remove RINP0 and RINN0
- Remove C67
- Mount a 33pF capacitor at C1 to limit the noise bandwidth of the amplifier (improves total SNR significantly)
- Mount 39Ω resistors, R56 and R57 on the back side of the PCB. Note that high quality linear resistors must be used not affect linearity.
- Mount a high quality 50Ω resistor at R5
- Mount a high quality 510Ω resistor at R44 (back

side of PCB)

- Add a buffer amplifier according to schematics
- Apply -5V on JP10 pin 7

The common mode voltage of the input signals are controlled by the common mode output voltage pin of the ADC when the jumper is applied at the "rightmost" position of JP2. Other voltage levels can be applied from an external source if the jumper is applied at the "leftmost" position of JP2. The terminal for the external voltage can be found at the connector in the top left corner of the board labeled "Common Mode". The common mode voltage can also be provided by the voltage divider RCM0 and RCM1. Remove resistor RCM2, mount appropriate resistors at RCM0 and RCM1 and apply a jumper at JP2 in the "leftmost" position.

Clock Generation

The clock input to the ADC accepts CMOS, LVDS, LVPECL and sine wave inputs, and can be provided via SMA connectors trough either a transformer, TR4, or directly. An on-board crystal oscillator (not mounted) can also be used. The board is configured to use the external SMA connector, X6, with CMOS format.

It is of utmost importance to supply a clock with low jitter. Poor jitter performance will directly result in reduced SNR. The SNR contribution from jitter is given by equation (1) assuming a full scale input signal at frequency, F_{IN}, and RMS-jitter, ε_{RMS}, measured in seconds.

$$SNR = -20\log(2 * \pi * F_{IN} * \varepsilon_{RMS})$$

One can see that a 1ps clock jitter with a 25MHz full scale input signal results in an additional SNR component of 76dBc. Due to this the clock signal should be treated with the same care as the analog inputs to the ADC.

Jitter numbers in the order of 1ps RMS has been achieved with the Stanford Research CG635 clock source. It provides CMOS, LVDS and LVPECL signals with adjustable amplitude.

To improve the performance even further the Evaluation Board supports crystal oscillator clocking. Low jitter crystal oscillators can be obtained from Wenzel (www.wenzel.com), Techtrol Cyclonetics Inc (TCI) (www.tci-ant.com) and Valpey Fisher (www.valpeyfisher.com). To obtain the lowest possible jitter, differential signaling should be used when connecting LVDS and LVPECL clock sources

The following modifications are necessary to convert the Evaluation Board clock input to other formats than CMOS:

Convert from CMOS to LVDS:

- Remove R37
- Mount a 100Ω resistor at R49
- Check if the clock source requires decoupling to ground and, if necessary, add suitable resistors at R46 and R52 (the CG635 requires 50Ω to ground on each output **instead** of 100Ω differential)

Convert from CMOS to LVPECL:

- Remove R37
- Mount suitable resistors at R46 and R52 and, if required, by the driver at R39 and R40 between each signal and supply. CG635 requires 50Ω load to ground on each input

Convert from CMOS to Sine Wave Input:

- Remove R37
- Mount a suitable transformer on TR4. The Mini-Circuits TC1-1T is suitable.
- Mount a 50Ω resistor at R46
- Mount 5kΩ resistors at R50 and R51
- Add a schottky diode at U3 (The HSMS2812 from Avago Technologies is recommended)
- Apply a sine wave with no DC offset and at least ±800mV_{pp} signal amplitude to X5

Convert from External Input to Oscillator:

- Mount a suitable oscillator at XO2. The board is built for LVPECL and LVDS oscillators from Valpey-Fisher (VFX0301). Oscillators from different vendors may be usable if the footprint and pinout are correct. It is also possible to use CMOS oscillators, (eg. VFX0321). In that case a 0Ω resistor should be mounted at R37 to ensure a low input on CKN.
- Remove the 0Ω resistor at R37 unless a CMOS oscillator is used
- Remove R53 and R54
- Mount resistors at R37, R38, R39 and R40 according to crystal oscillator specifications

- Add a jumper on JP13 in "topmost" position to connect power supply to the oscillator, doing this will connect the oscillator power supply to the same supply as the CMOS outputs of the ADC. Follow the guideline in the next bullet point to obtain a more silent power supply to the ADC
- Supplying a silent power to the oscillator: Move the jumper for OVDD from JP1 to JP3 and supply the output driver supply (2.5V) on JP10. This will disconnect the ADC output drivers from the regulator U1, and the oscillator only will be connected to the regulated supply.

Digital Control Signals

The digital control signals are applied to the ADC through JP8 and JP9. Debouncer circuit DB1 remove possible glitches from the signals when operating jumpers. The debouncer circuit is enabled when JP12 is in the "leftmost" position. The control signals can also be supplied by any pattern generator providing CMOS signals with appropriate voltage levels. In this case the debouncer circuit should be disabled by moving the jumper at JP12 to the "rightmost" position. The numbered list on the PCB describes which signal each pin in JP8/JP9 corresponds to. Refer to the datasheet for the functionality of each control signal and to table 1 for default settings.

Digital Outputs

The digital outputs are buffered versions of the ADC outputs. Consult the datasheet for description of data output formats and options. The outputs are buffered with LVCMOS buffers running from a 0.8 to 2.7V power supply. The buffer inputs are 3.6V tolerant. For ADC I/O power supply (OVDD, set by voltage regulator U11) below 2.7V it is advantageous to keep the buffer supply voltage (set by voltage regulator U4) at a similar level. For ADC I/O voltage above 2.7V, the buffer supply voltage can be kept at 2.7V

Data from the ADC, and the ADC clock is presented on JP5. The clock is a buffered version of the CK_EXT ADC output signal. Make sure that this output is enabled to use this clock to trigger the data capture device. The pinout of JP5 is designed to interface directly with Agilent Logic Analyzer Termination Adapter (model 01650-63203). The pinout is shown in Figure 3. MSB corresponds to 12 and LSB to 0. ORNG is the out-ofrange flag.

For 10-bit ADCs the LSB bit will be present on pin 3. Pin 0, 1 and 2 will be tied to ground.

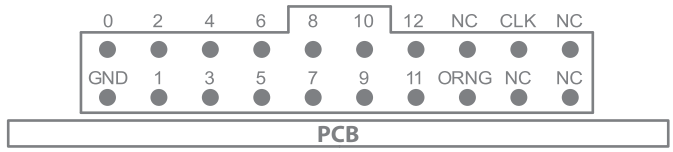

Figure 3. JP5 Pinout (Front View)

Jumper Descriptions

Jumper #	Default setting	Corresponding ADC pin	Description
JP8/JP9			0: Jumper Applied on JP8, 1: Jumper Applied on JP9
1	1	PD_N	Power Down (Active Low)
2	1	SLP_N	Sleep Mode Control (Active Low)
3	0	OE_N	Output Enable (Active Low)
4	0	CLK_EXT_EN	External Clock Enable (Active Low)
5	0	DFRMT	Data Format Select
6	1	CM_EXTBC_0	CM_EXT Bias Control
7	0	CM_EXTBC_1	CM_EXT Bias Control
JP11			
1	Top Position		Select supply to digital buffers from U4 (default) or external source connected to JP10
JP12			
1	Left Position		Enable (default)/disable debouncer circuits
JP2			
1	Right Position		Select common mode voltage from ADC chip (default) or external source
JP1/JP3			
All Pins	Top Position		Select supply voltage to power domains on ADC chip from U1 and U11 or from external sources connected to JP10. Connect amp meter instead of jumper to measure supply current per power domain.

CEB1307 / CEB1308 Evaluation Board Bill of Materials (BOM)

Qty	Value	Device	Parts	Package	Maufacturer	Part #
1	CDK130x QFN	CDK130x QFN	CDK130x	QFN64	Exar	CDK1307xILP64 or CDK1308xILP64
1	NC	AD8139	BUFIN0	SOIC_N_EP	Analog Devices	AD8139
1	ADT1-1WT	ADT1-1WT	TR0	CD542	Mini-Circuits	ADT1-1WT
1	MAX6818EAP	MAX6818	DB1	SSOP	Maxim	MAX6818
1	74LVC573A	74LVC573ADBR	BUF1	SSOP	Texas Instruments	SN74LVC573ADBR
1	SN74AUC16244	SN74AUC16244	BF0	TVSOP	Texas Instruments	SN74AUC16244DGVR
3	BU-SMA-H	BU-SMA-H	X1, X5, X6	BU-SMA-H		
3	LM317	LM317	U1, U4, U11	SOT-223	National Semiconductor	LM317AEMP/NOPB
4	YC248	YC248	RZ1, RZ2, RZ5, RZ6	0603 x 8 (Convex)	Yageo	YC248-JR-0722RL
3	500	3296W	R_POT0, R_POT1, R_POT2	3296W	BOURNS	3296W-1-203LF
3	150uF	CPOL-EUD/7343-31R	C27, C38, C42	7343-31	Kemet	B45197A1157K409
1	HSMS-2812	HSMS-2812	U2	SOT-23	Avago Technologies	HSMS-2812-TR1G
1	PINHD-1X10	PINHD-1X10	JP4	PINHEAD 2.54 mm		

CEB1307 / CEB1308 Evaluation Board Bill of Materials (BOM) Continued

Qty	Value	Device	Parts	Package	Maufacturer	Part #
4	PINHD-1X3	PINHD-1X3	JP2, JP11, JP12, JP13	PINHEAD 2.54 mm		
1	PINHD-1X5	PINHD-1X5	JP3	PINHEAD 2.54 mm		
1	PINHD-1X7	PINHD-1X7	JP9	PINHEAD 2.54 mm		
1	PINHD-2X10/90	PINHD-2X10/90	JP5	PINHEAD 2.54 mm		
1	PINHD-2X5	PINHD-2X5	JP1	PINHEAD 2.54 mm		
1	PINHD-2X7	PINHD-2X7	JP8	PINHEAD 2.54 mm		
1	PINHD-1X9	MPT-9	JP10	Term Block 2.54 mm	Phoenix Contact	
13	47nF	C04020402_SLIM*	C10, C11, C12, C13, C15, C16, C18, C19, C20, C21, C22, C23, C24	0402		
10	100nF	C0603	C7, C33, C36, C39, C43, C46, C47, C48, C51, C67	0603		
1	1nF	C0603	C49	0603		
2	100pF	C0603	C57, C58	0603		
7	2.2uF	C1206	C14, C25, C28, C37, C40, C41, C44	1206		
5	0	R0603	R38, R53, R54, R64, RCM2	0603		
2	100k	R0603	R7, R8	0603		
1	270	R0603	R26	0603		
4	33	R0603	R47, R48, RINN0, RINP0	0603		
2	120	R0603	R30, R33	0603		
1	1.2k	R0603	R27	0603		
2	330	R0603	R31, R35	0603		
1	39	R0603	R1	0603		
3	510	R0603	R60, R61, R41	0603		
1	100	R0603	R2			
2	NC	C0603	C61, C62	0603		
1	NC	PINHD-1X7	JP6	PINHEAD 2.54 mm		
23	NC	R0603	R5, R14, R15, R16, R25, R28, R29, R32, R34, R36, R37, R39, R40, R44, R46, R49, R50, R51, R52, R56, R57, RCM0, RCM1	0603		
1	NC	TC4-1W	TR4	AT224	Mini-Circuits	TC4-1W
1	NC	VFXO301	XO2			

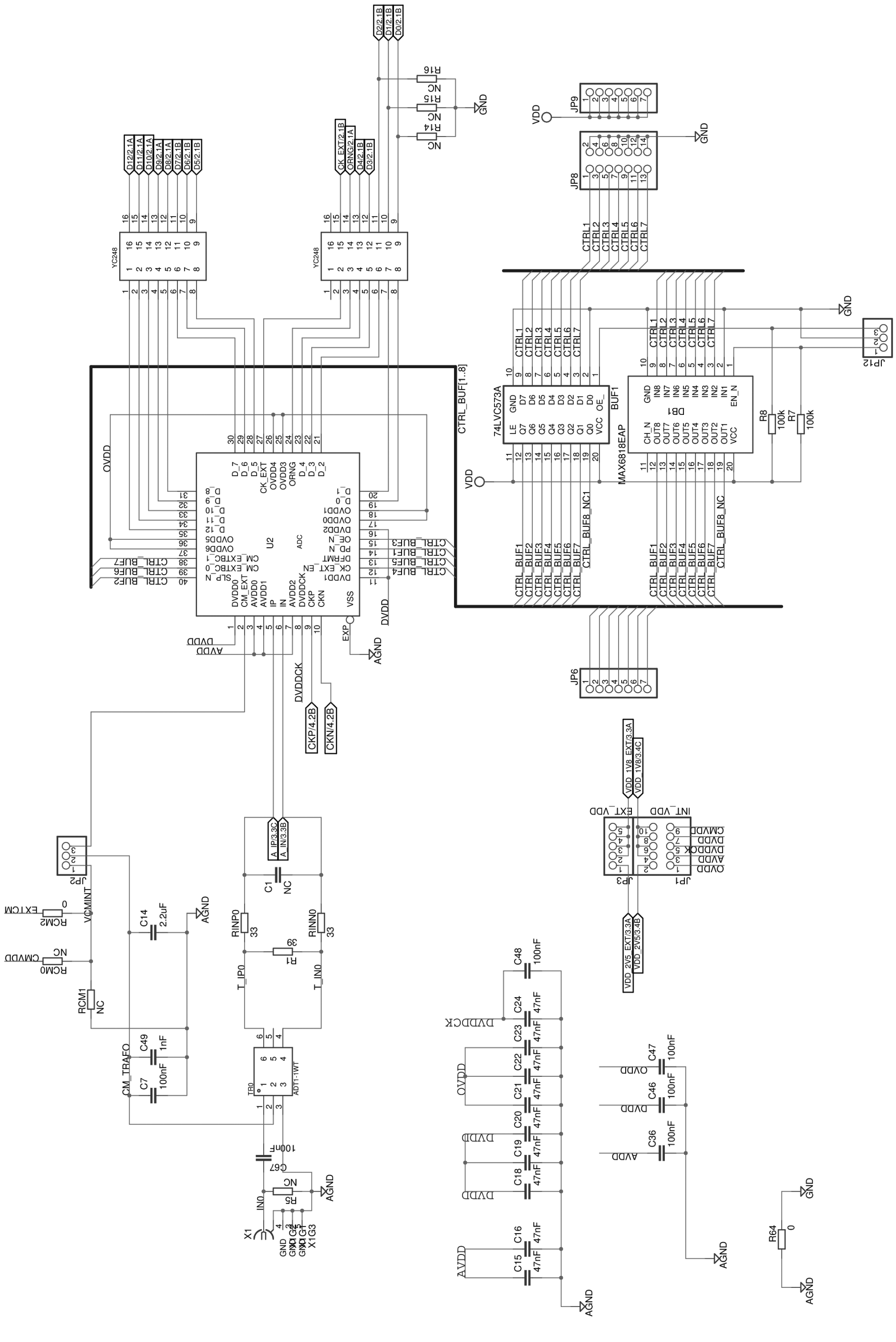

Figure 4. CEB1307 / CEB1308 Schematic Diagram (1 of 4)

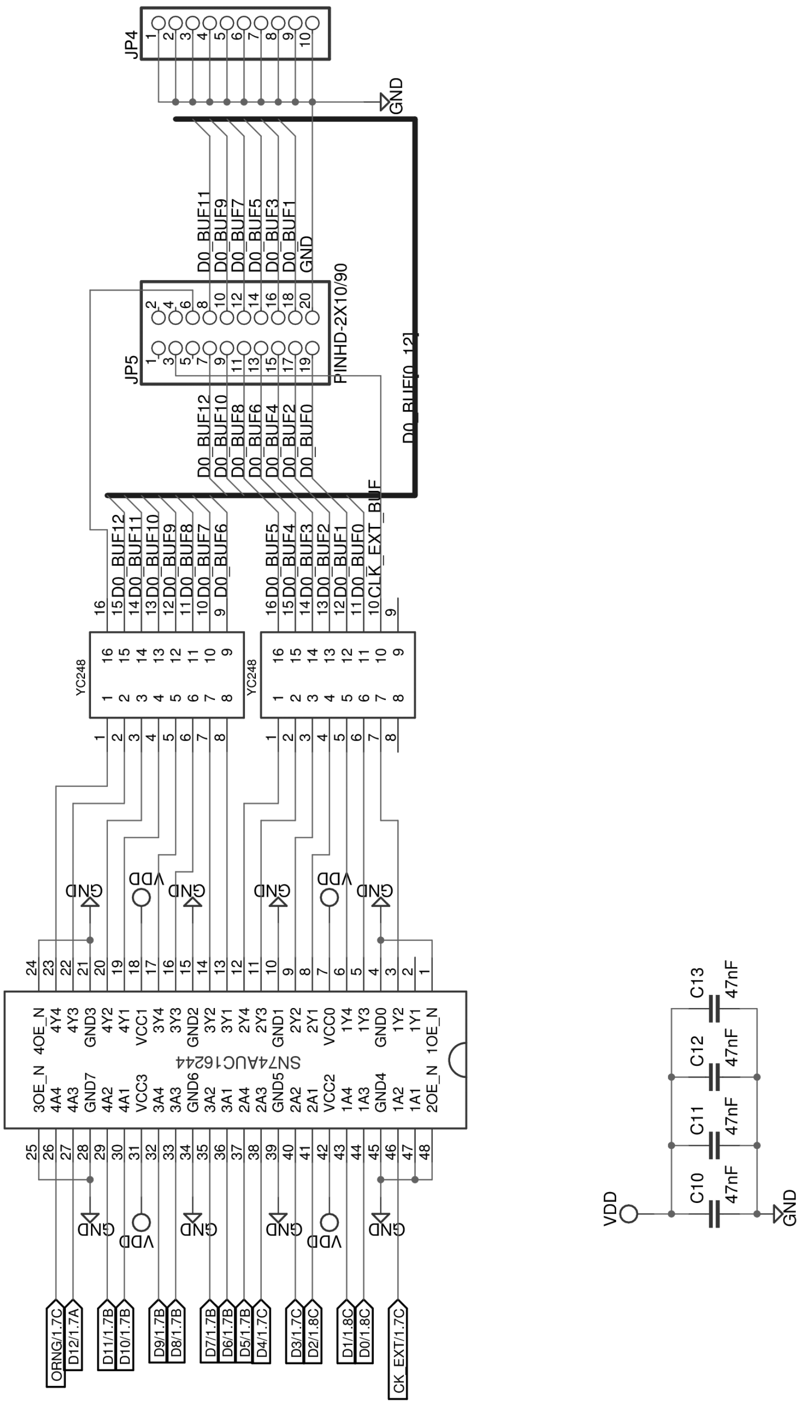

Figure 5. CEB1307 / CEB1308 Schematic Diagram (2 of 4)

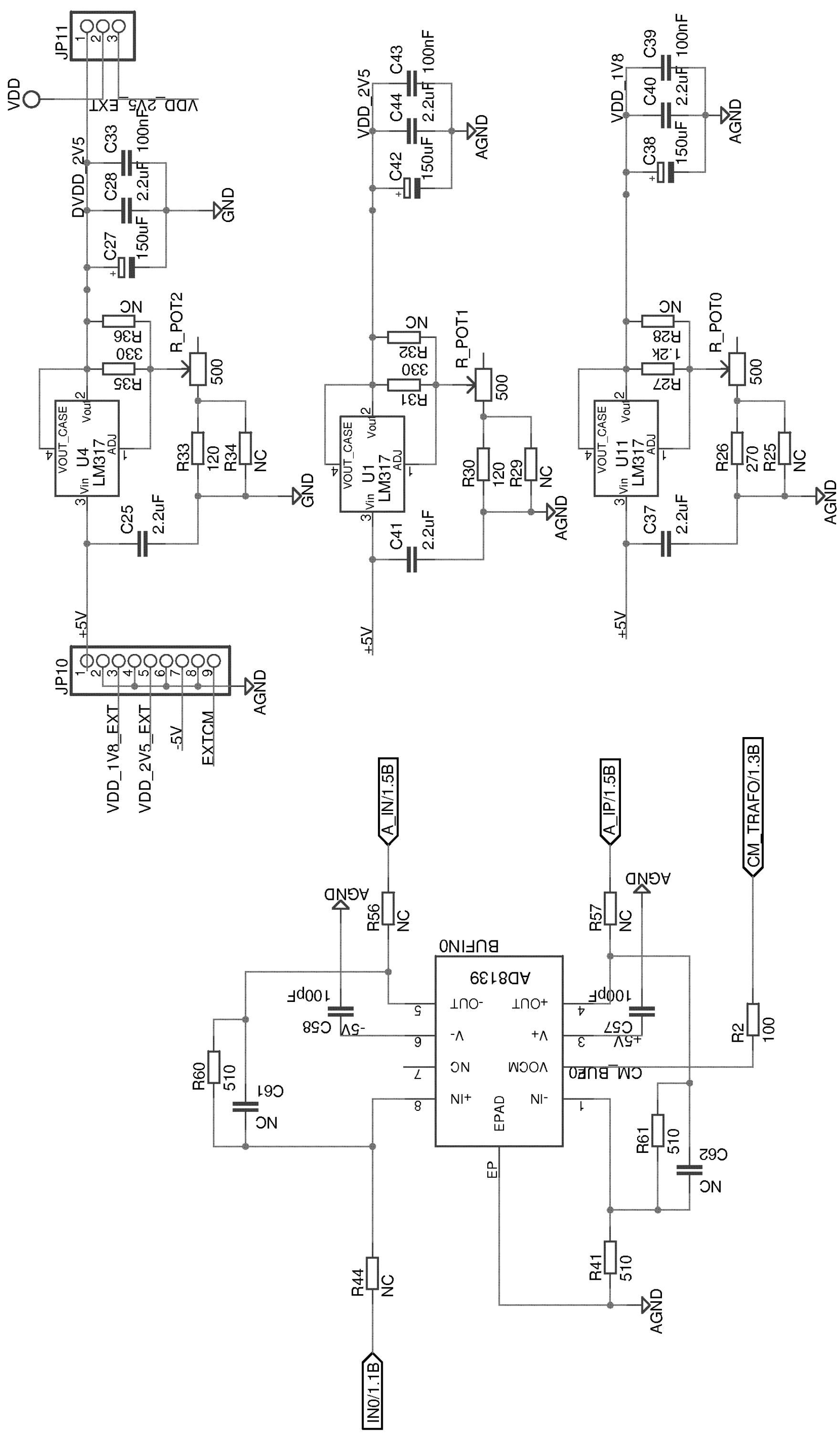

Figure 6. CEB1307 / CEB1308 Schematic Diagram (3 of 4)

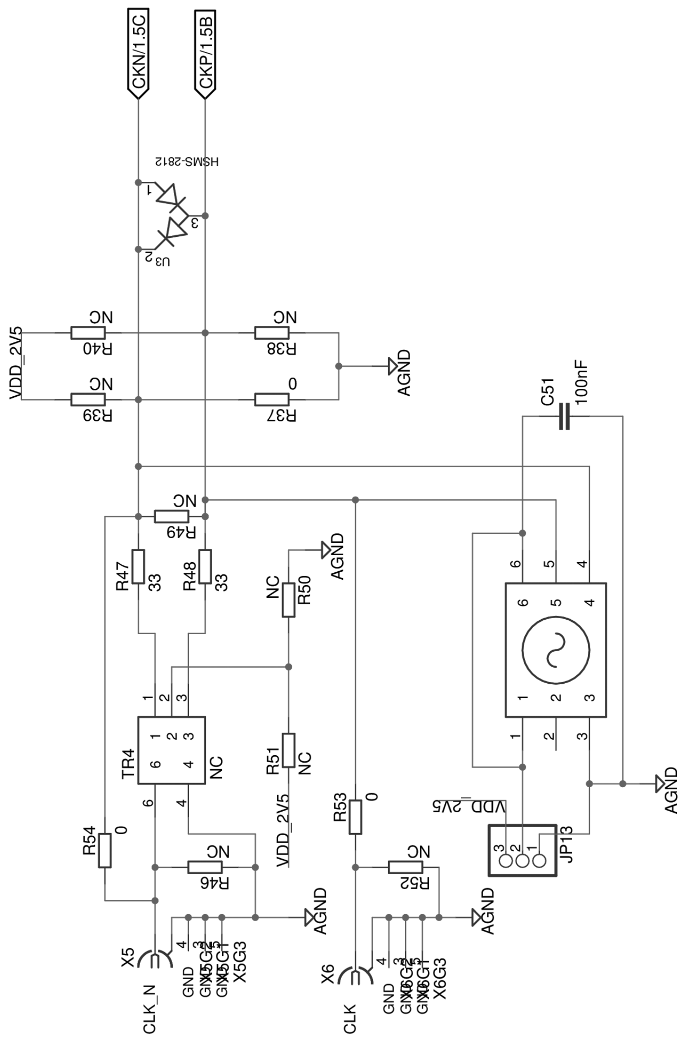

Figure 7. CEB1307 / CEB1308 Schematic Diagram (4 of 4)

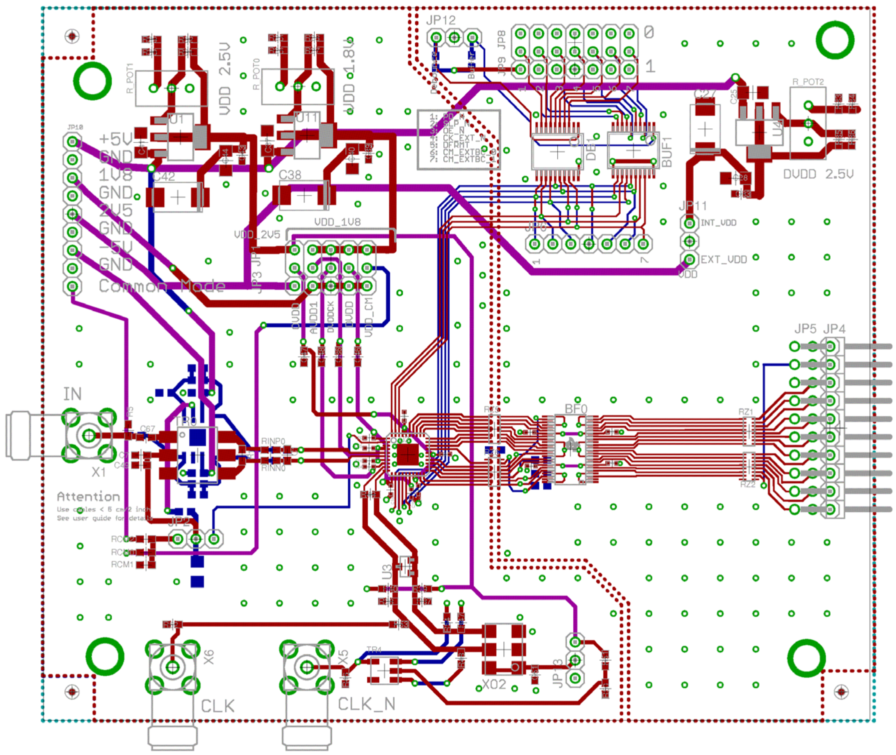

Figure 8. All Routing Layers

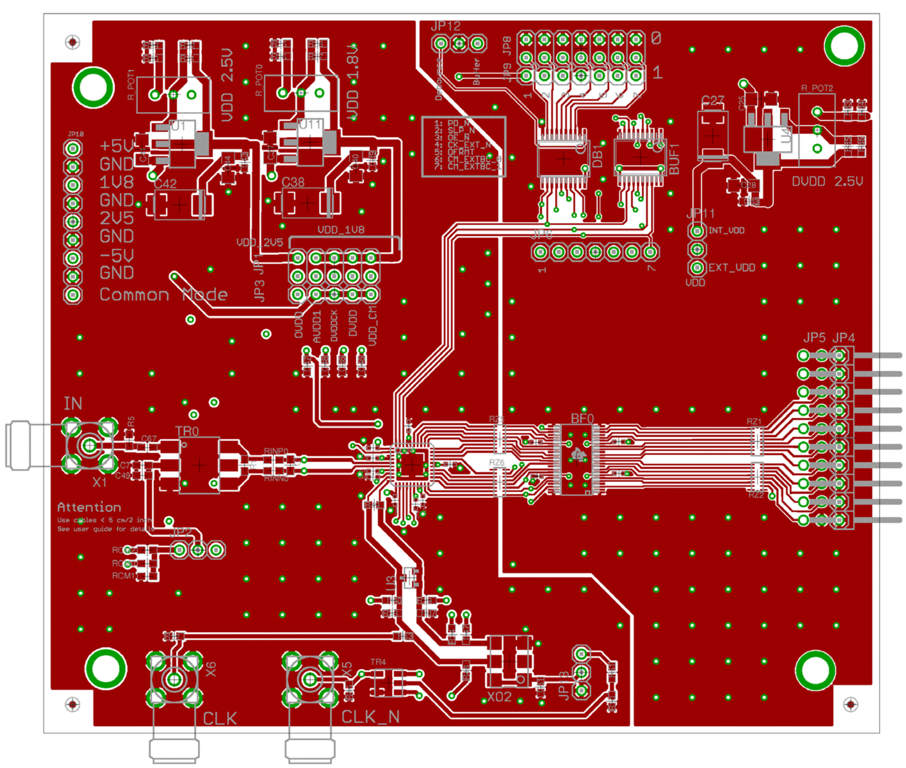

Figure 9. Component Side (Top View)

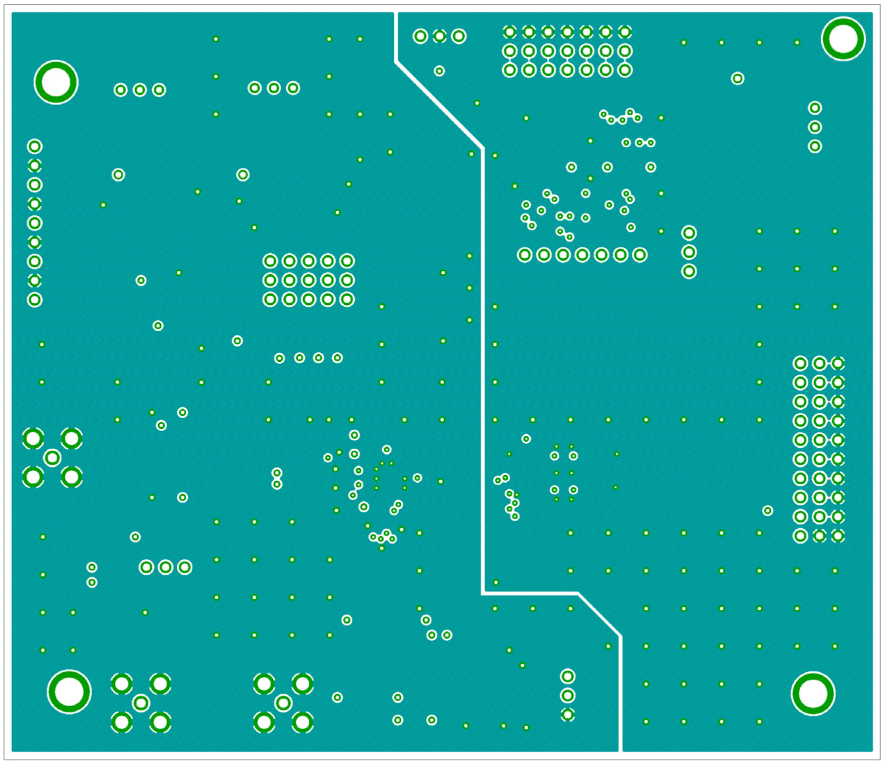

Figure 10. Internal Layer 1 (Top View)

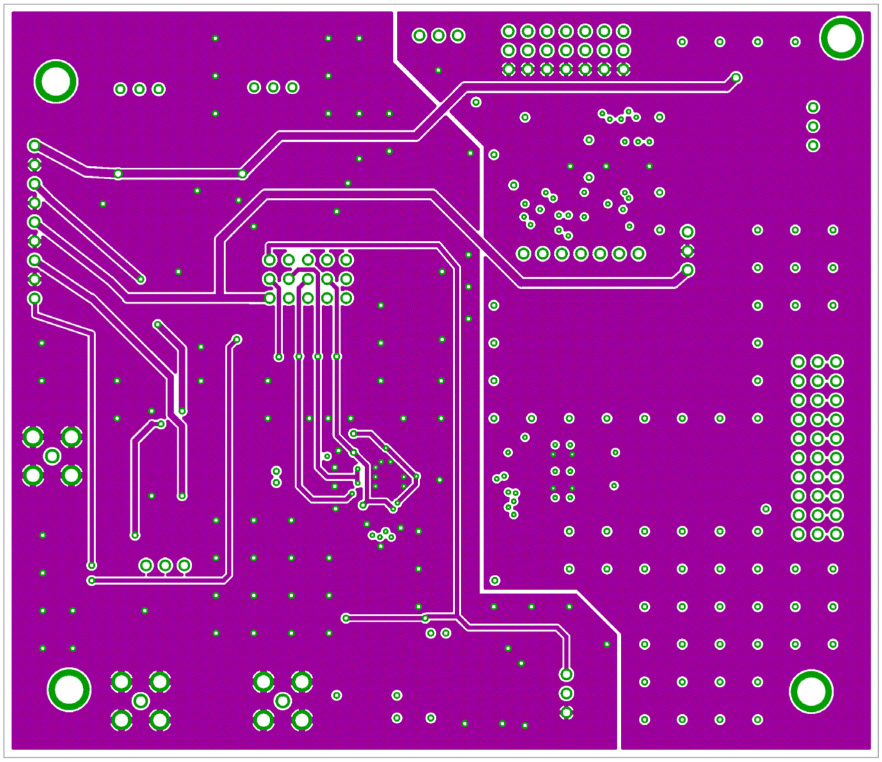

Figure 11. Internal Layer 2 (Top View)

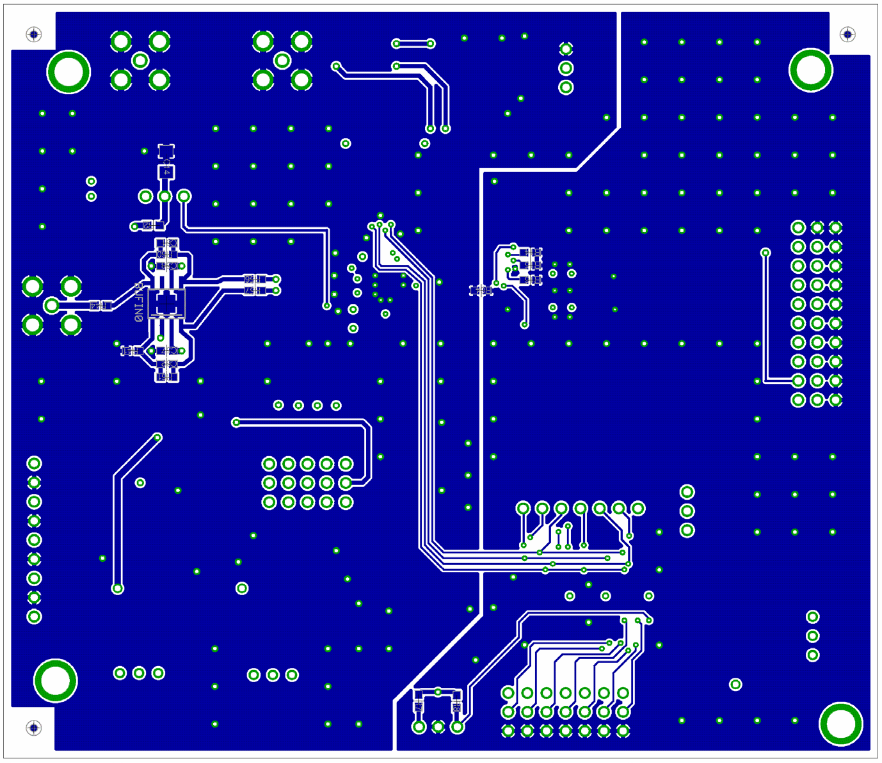

Figure 12. Solder Side (Bottom View)

For Further Assistance:

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