12/6/2010



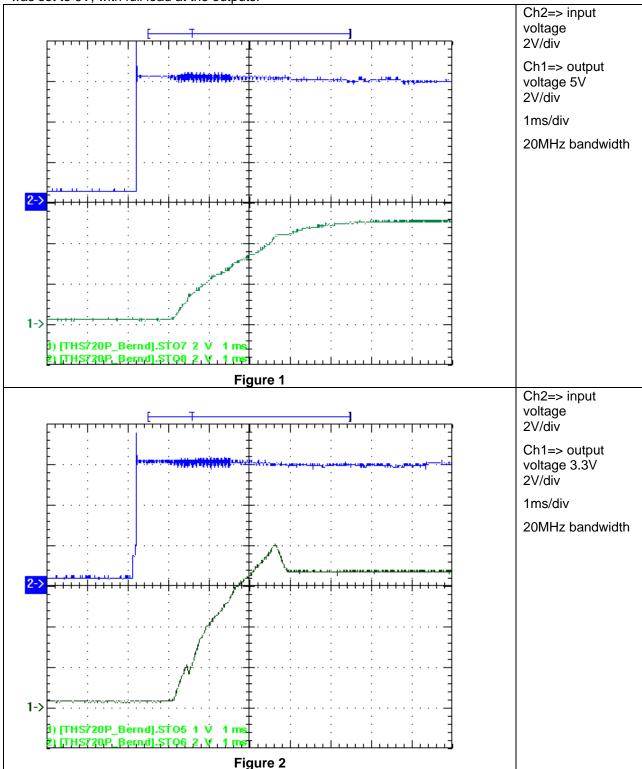


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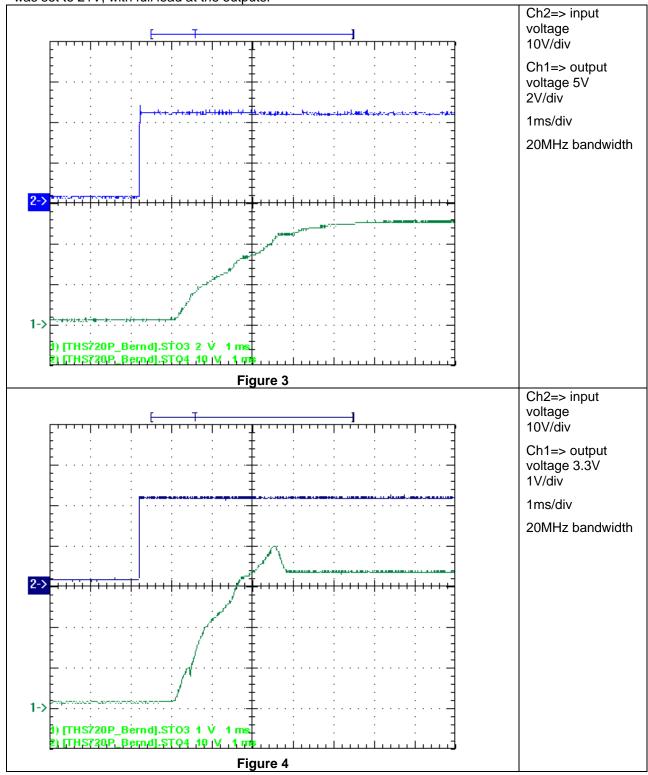
1 Startup

The startup waveform is shown in the Figure 1 (5V out) and Figure 2 (3.3V out). The input voltage was set to 6V, with full load at the outputs.



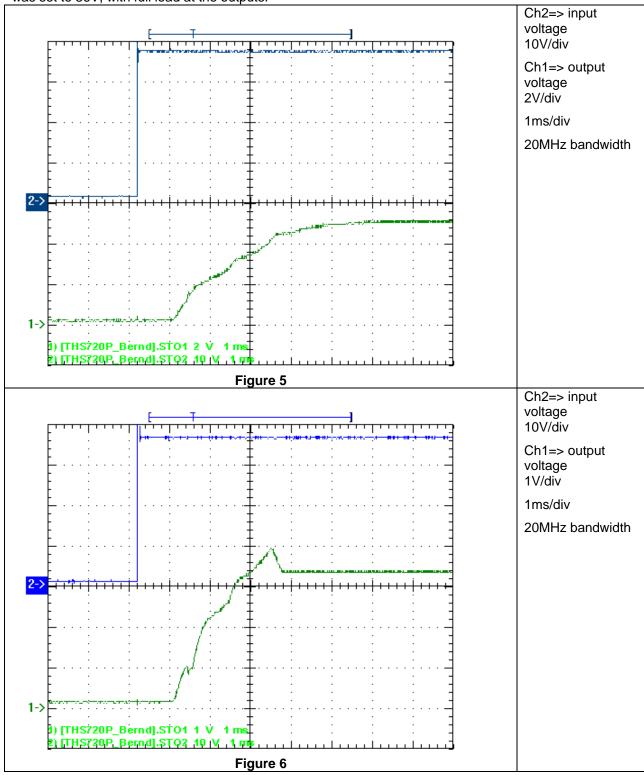


The startup waveform is shown in the Figure 3 (5V out) and Figure 4 (3.3V out). The input voltage was set to 21V, with full load at the outputs.





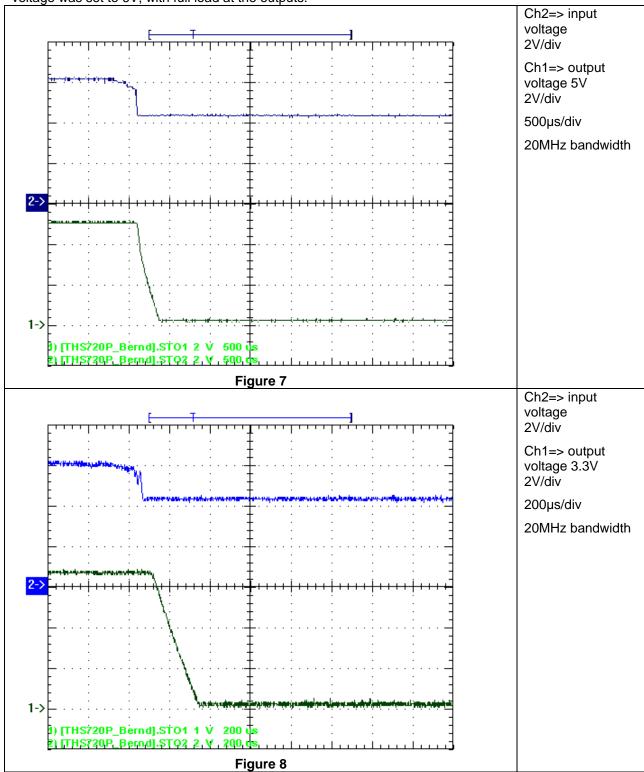
The startup waveform is shown in the Figure 5 (5V out) and Figure 6 (3.3V out). The input voltage was set to 36V, with full load at the outputs.





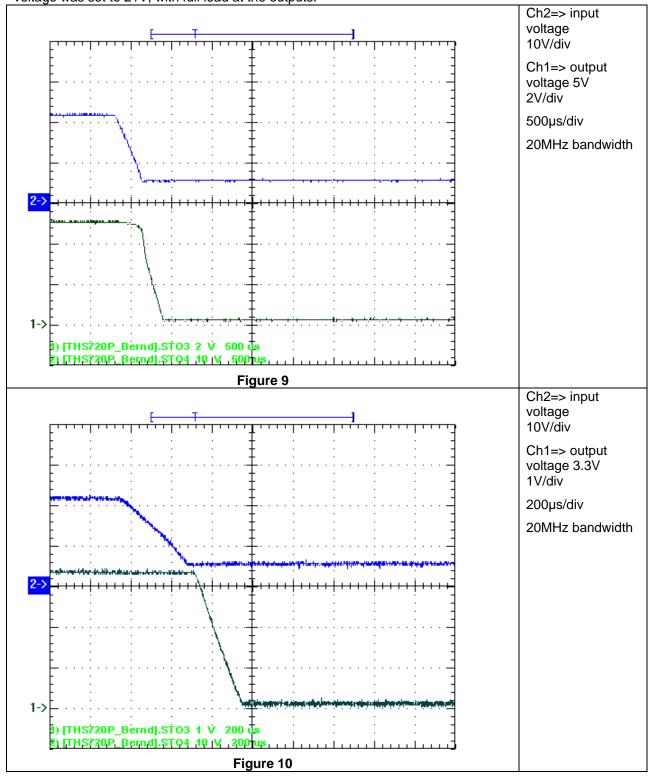
2 Shutdown

The shutdown waveform is shown in the Figure 7 (5V out) and Figure 8 (3.3V out). The input voltage was set to 6V, with full load at the outputs.



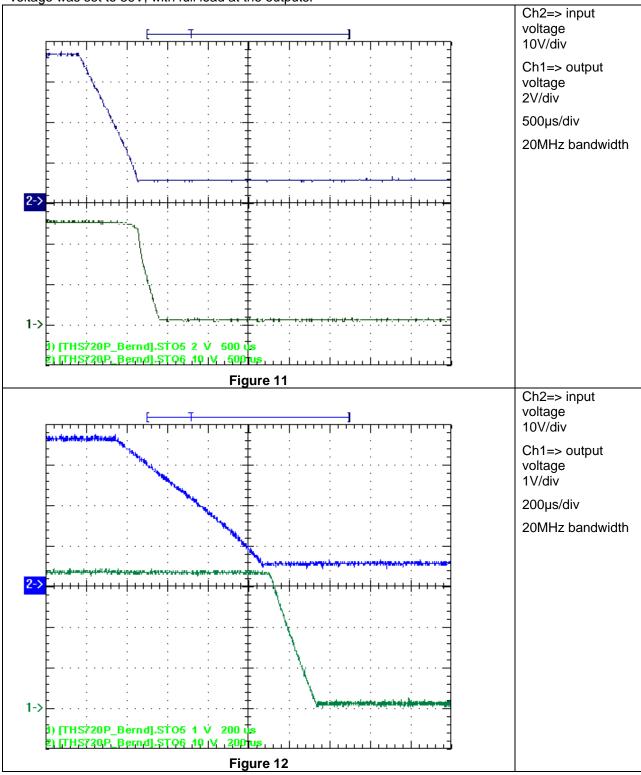


The shutdown waveform is shown in the Figure 9 (5V out) and Figure 10 (3.3V out). The input voltage was set to 21V, with full load at the outputs.





The shutdown waveform is shown in the Figure 11 (5V out) and Figure 12 (3.3V out). The input voltage was set to 36V, with full load at the outputs.





3 Efficiency

The efficiencies with different input voltages are shown in the Figure 13 below.

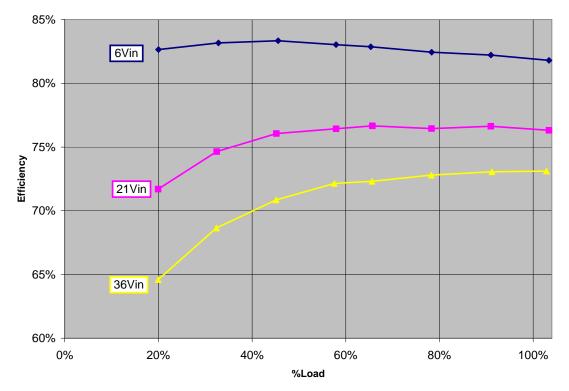


Figure 13



4 Load regulation

The load regulation for the 5V output at different input voltages are shown in Figure 14.

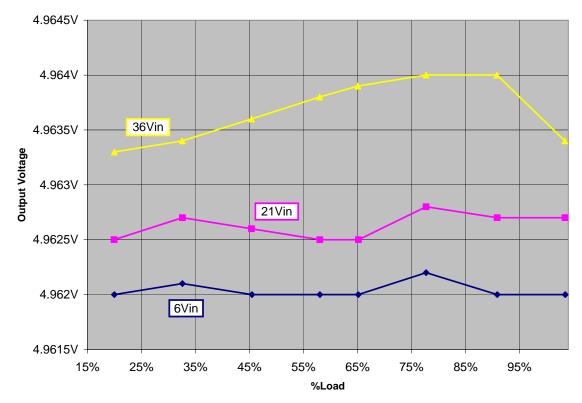


Figure 14



The load regulation for the 3.3V output at different input voltages are shown in Figure 15.

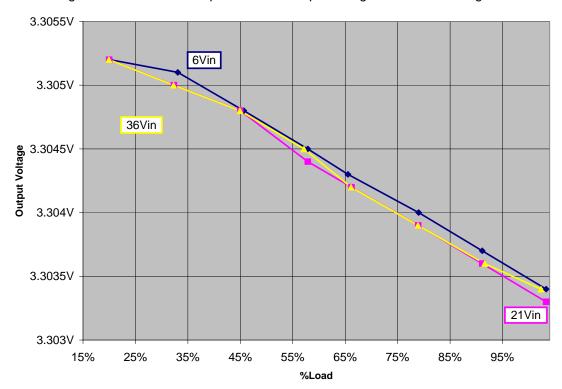


Figure 15



5 Line Regulation

The line regulation for the 5V output at full output current is shown in Figure 16

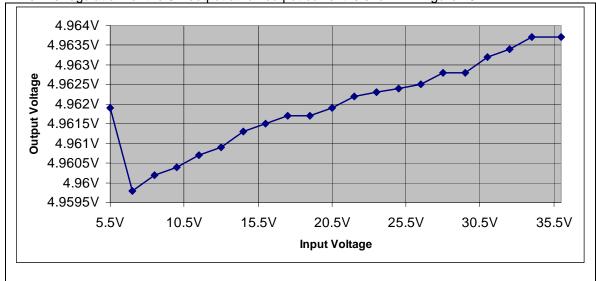


Figure 16

The line regulation for the 5V output at full output current is shown in Figure 17

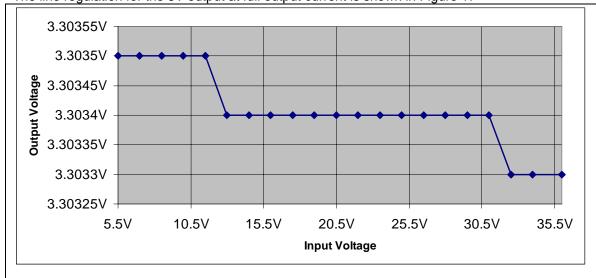


Figure 17



With the same measurement setup the efficiencies at 100% load are shown in Figure 18.

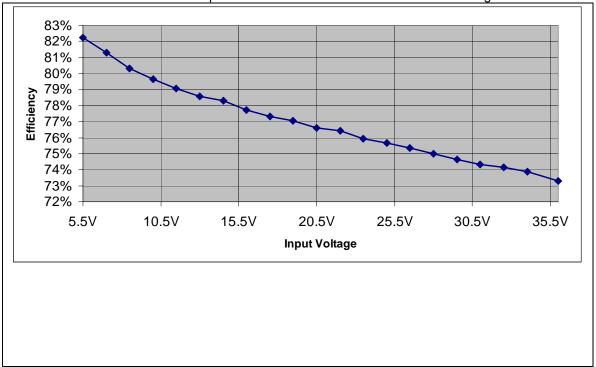
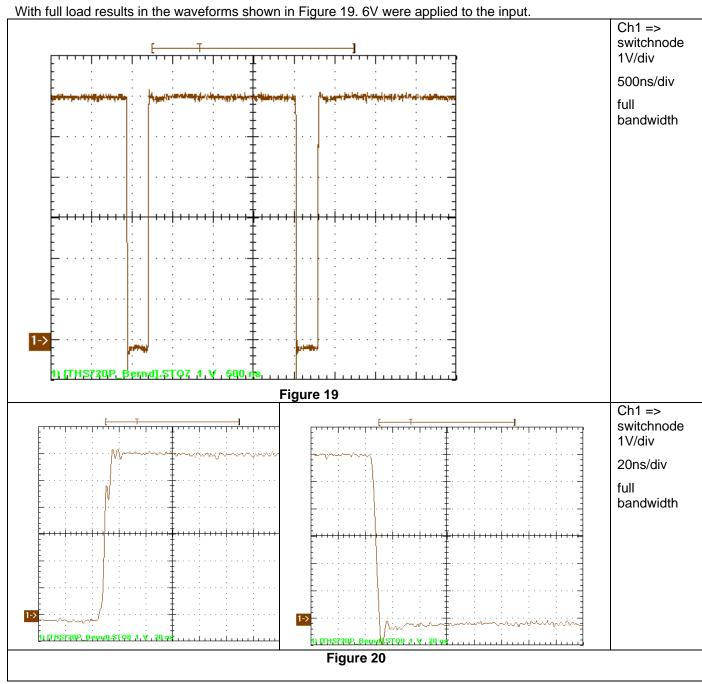


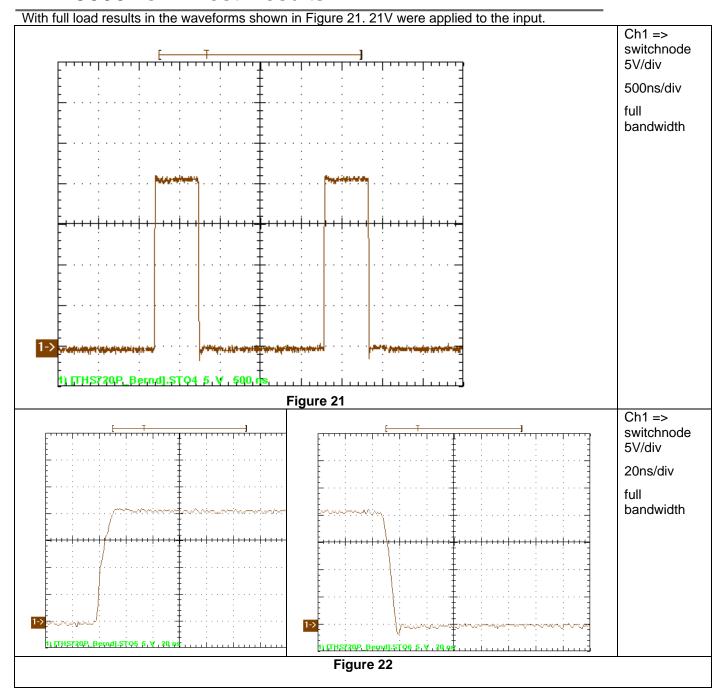
Figure 18



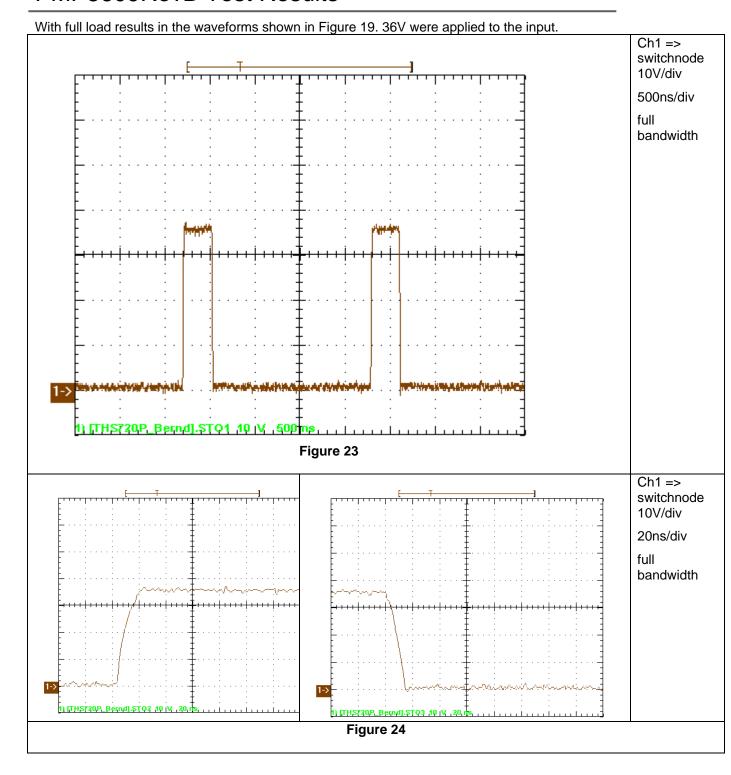
6 Switch Node Waveform













7 Input Ripple

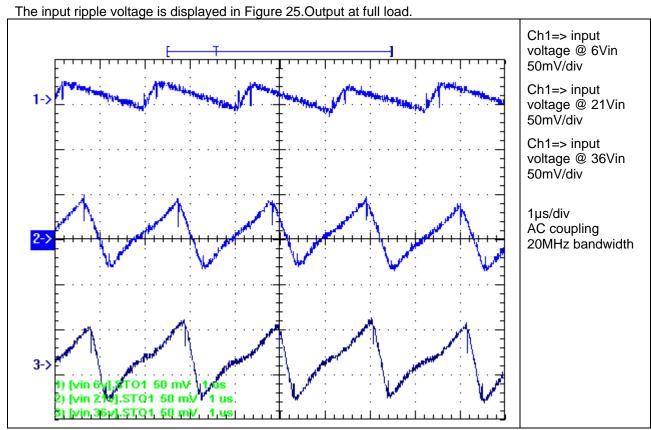


Figure 25

8 Output Ripple

With the resolution 50mV/div no ripple detectable



9 Control Loop Frequency Response

The control loop frequency response with full load and 6V input voltage is shown in Figure 26

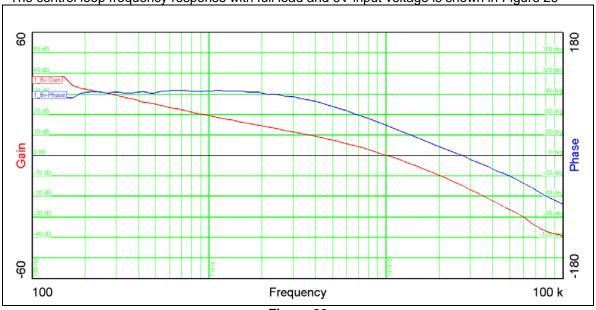


Figure 26

The control loop frequency response with full load and 21V input voltage is shown in Figure 27

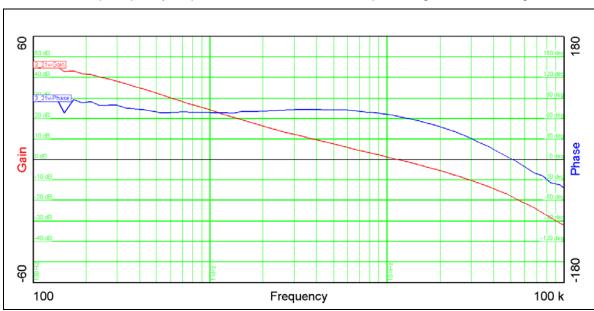


Figure 27



The control loop frequency response with full load and 36V input voltage is shown in Figure 28

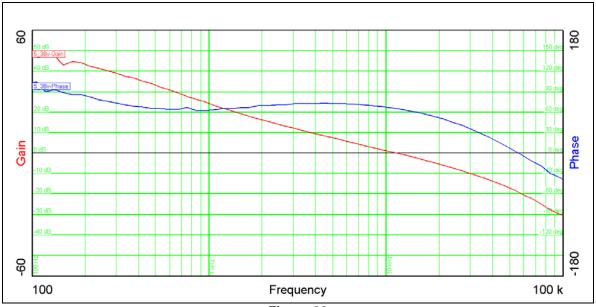


Figure 28

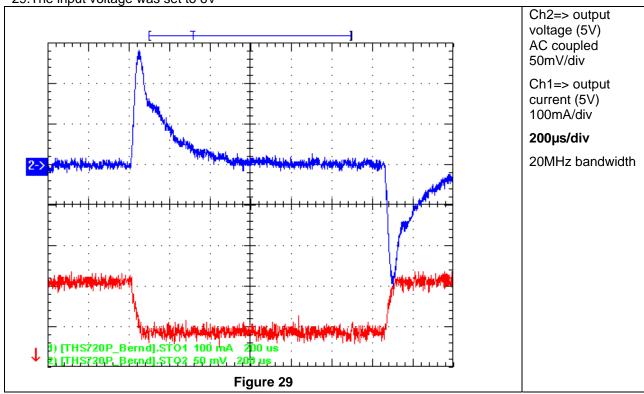
Table 1 summarizes the resu	uits.
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Vin	6V	21V	36V			
Bandwidth (kHz)	10.2	11.5	11.4			
Phase margin	43.6°	63.4°	65.5°			
slope (20dB/decade)	-1.46	-1.08	-1.06			
gain margin (dB)	-14.8	-18.3	-19.1			
slope (20dB/decade)	-2.04	-2	-2.25			
freq (kHz)	26.9	51.3	55.8			
Table 1						

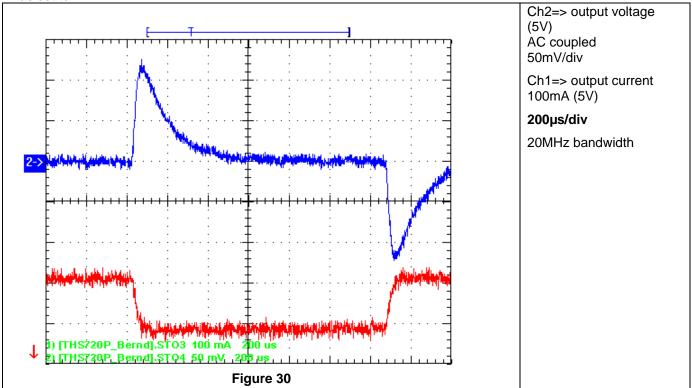


10 Load Transients

A output current change from 125mA to 250mA of the 5V output results in following Figure 29.The input voltage was set to 6V



A output current change from 125mA to 250mA results in following Figure 30.The input voltage was set to 21V





A output current change from 125mA to 250mA results in following Figure 31.The input voltage was set to 36V

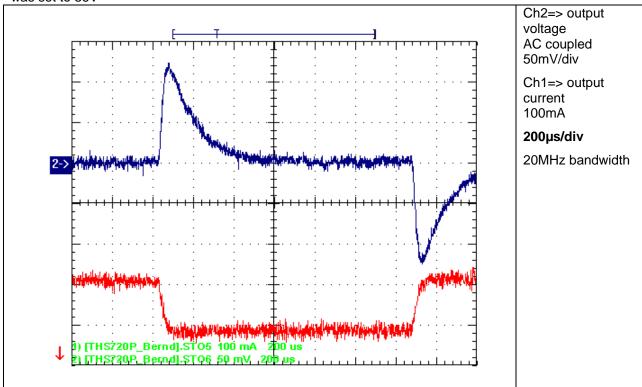
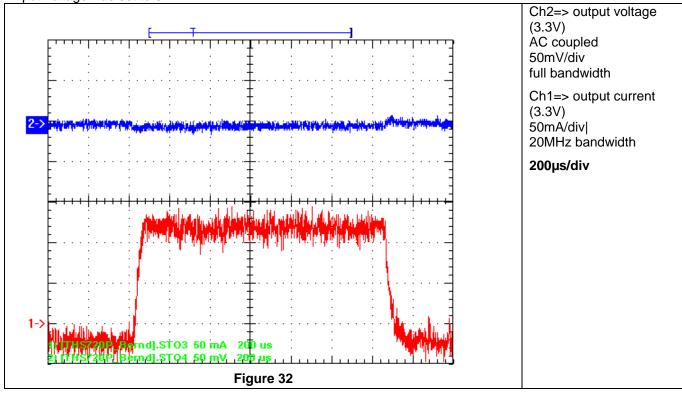


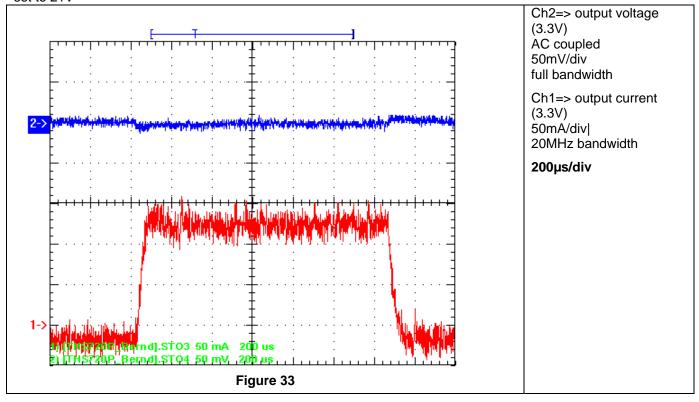
Figure 31



A output current change from 0mA to 150mA of the 3.3V output results in following Figure 32.The input voltage was set to 6V

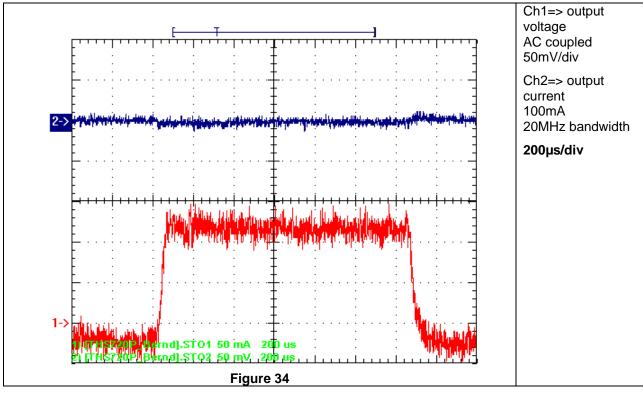


A output current change from 0mA to 150mA results in following Figure 33. The input voltage was set to 21V





A output current change from 0mA to 250mA results in following Figure 34. The input voltage was set to 36V





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