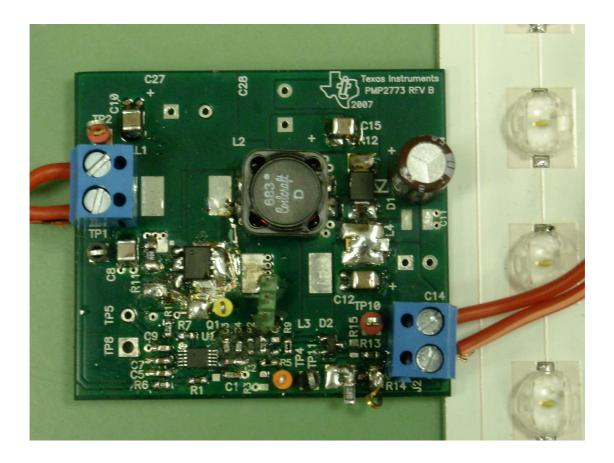


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1 Picture of the Converter: specifications



Design (RevA) was made according to the customer initial schematic and BOM, with customer LED specifications (two different sets), 6XLXML-PD01-0030 (Red) @ 0.24A and 0.35A, and 6XLXML-PB01-0013 (Blue) @ 0.24A and 0.35A, to solve his instability problems. Calculations come from MathCad sheets, SEPIC_LED_PMP4586+Loop(0030) and SEPIC_LED_PMP4586+Loop(0013).

Customer switching frequency was 130kHz (actual is 300kHz), so calculations have been performed also for this case, and results are inside the two MathCad sheets, "SEPIC_LED_PMP4586+Loop(0013)_csmr", "SEPIC_LED_PMP4586 +Loop(0030)_csmr".

Prototype was built (RevB) with an optimized BOM we proposed, and with the available LEDs 6XLUW W5JM @ the two specified currents SEPIC_LED_PMP4586+Loop(LWW5JM)

In the MathCad two power stage models are considered. First a simplified power with first order (current mode) effect, that typically is enough accurate at low power levels (RHP zero, power stage pole, ESR zero). After a second model including some second order effects present even in current mode operations, in particular the resonances effect of the LC elements in the circuit that create two double poles (in addition to the one of the first model) and two complex RHP-zeros, almost cancelling each other, but with very high Q, therefore introducing a glitch in the frequency response at a frequency value depending on duty cycle.



The background theoretical analysis (developed by Vorperian) is synthesized in the MathCad Sheet, in the ideal hypothesis of not considering the parasitic elements of the reactive components (R series especially).

Typically the parasitics (series resistances of the inductances, ESR of Capacitors) naturally dump these oscillations, so in the actual loop glitch effects are still present but with small amplitude, so if bandwidth is closed enough before this events, the glitch effect becomes not effective.

In other cases, it's necessary to provide an external dumping (typically in parallel to the transfer capacitor) with an RC network. The dimensioning criteria is to put the smaller resistance possible compatible with its dissipation, and in series the biggest capacitance to have its impedance much lower that the value of R.

2 Loop measurements

The measured open loop Gain and Phase are displayed in the following pictures, for the two different LED current values. Different loop has been implemented for the two LED current conditions.

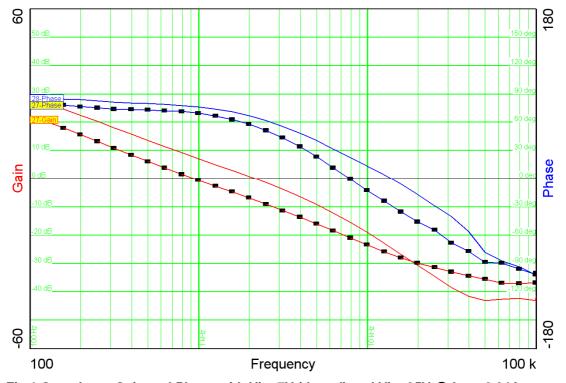


Fig.1 Open Loop Gain and Phase with Vin=7V (dotted) and Vin=35V @ lout=0.34A



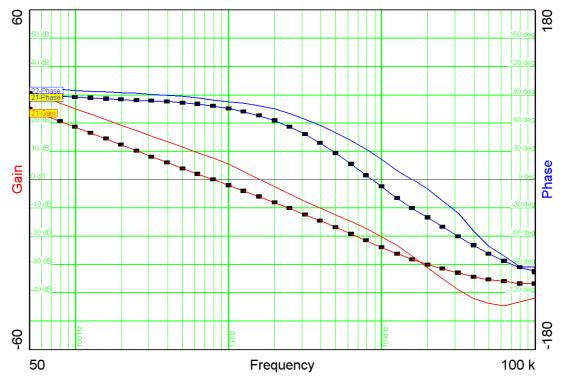


Fig.2 Open Loop Gain and Phase with Vin=7V (dotted) and Vin=35V @ lout=0.25A

3 Efficiency and output Open Circuit Protection

The efficiency has been measured for minimum and maximum input voltage in the two conditions of LED current. Results are displayed in the following table.

I_LED[A]	Vin[V]	lin[A]	Vout[V]	lout[mA]	η%
0.25	7.112	0.833	20.31	255	87.4
0.25	35.43	0.169	20.29	255	86.4
0.34	7.17	1.124	20.81	337	87.0
0.34	35.37	0.23	20.79	337	86.1

Protection in the output clamps the voltage to 27.84V.



4 Thermal measurements

Thermal picture of the converter has been taken for the highest output current of 0.34A and maximum input voltage (lowest efficiency).

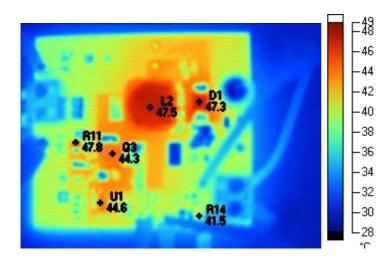


Fig.3 Vin=35V @ I_LED=0.34A



5 Warning

<u>For Feasibility Evaluation Only, in Laboratory/Development Environments.</u> The EVM is not a complete product. It is intended solely for use for preliminary feasibility evaluation in laboratory / development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical / mechanical components, systems and subsystems. It should not be used as all or part of a production unit.

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