UCC25710 LIPS Solution for LED TV Backlighting

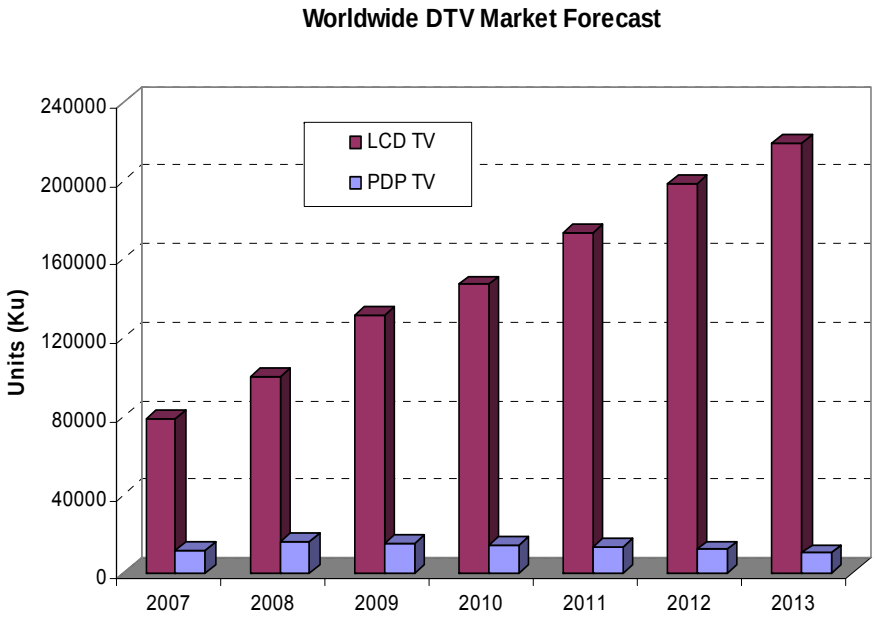
Mar 10th, 2010

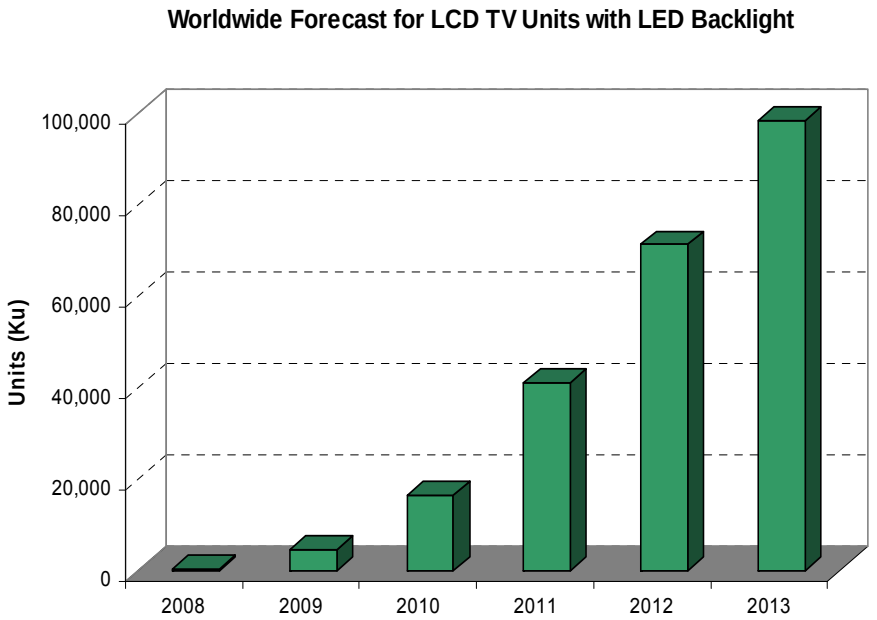
Anderson Hsiao

Outline

- DTV Market Trend
- Multi-Transformer Design
- UCC25710 Introducing
- Reference Design Performance
- IC Introducing

DTV Market Trend





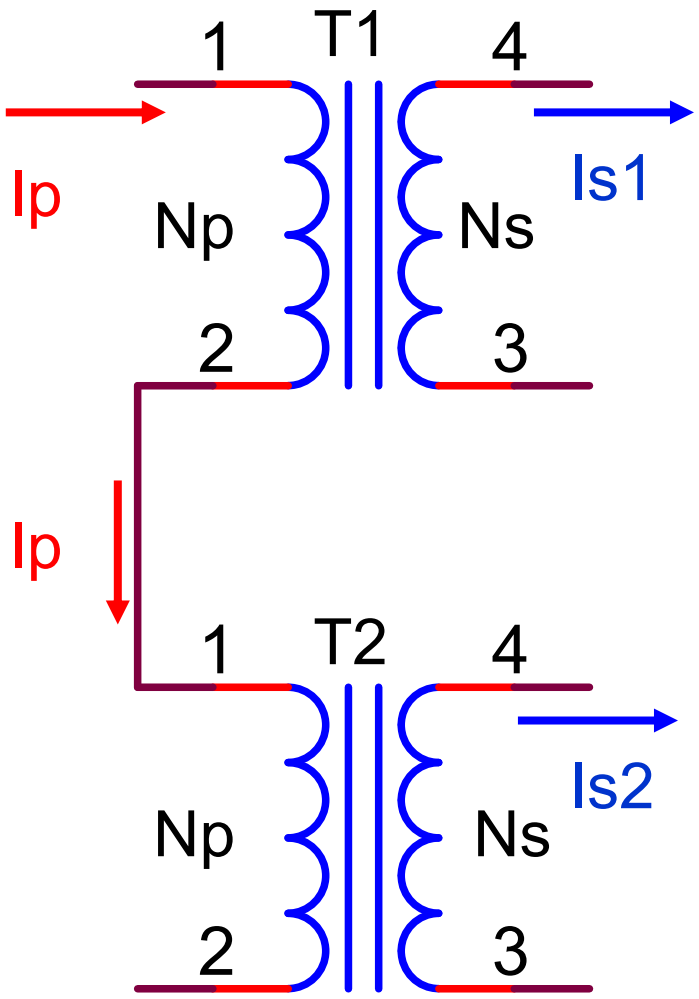
Source: iSuppli *"Worldwide TV Market Tracker Q3 2009"*

- DTV market forecasted to grow at 15% CAGR with LCD-TV expected to account for ~90% of total TV market by 2013
- LED backlighting application is hot; 5 year CAGR of 141%
- Edge lit LED TV dominates (90%) market – simpler, enable slim designs & cost effective
- CIP team strategy to support WLED TV backlighting applications; RGB will be supported by C2000 & DCP groups

Multi-Transformer Current Balancing

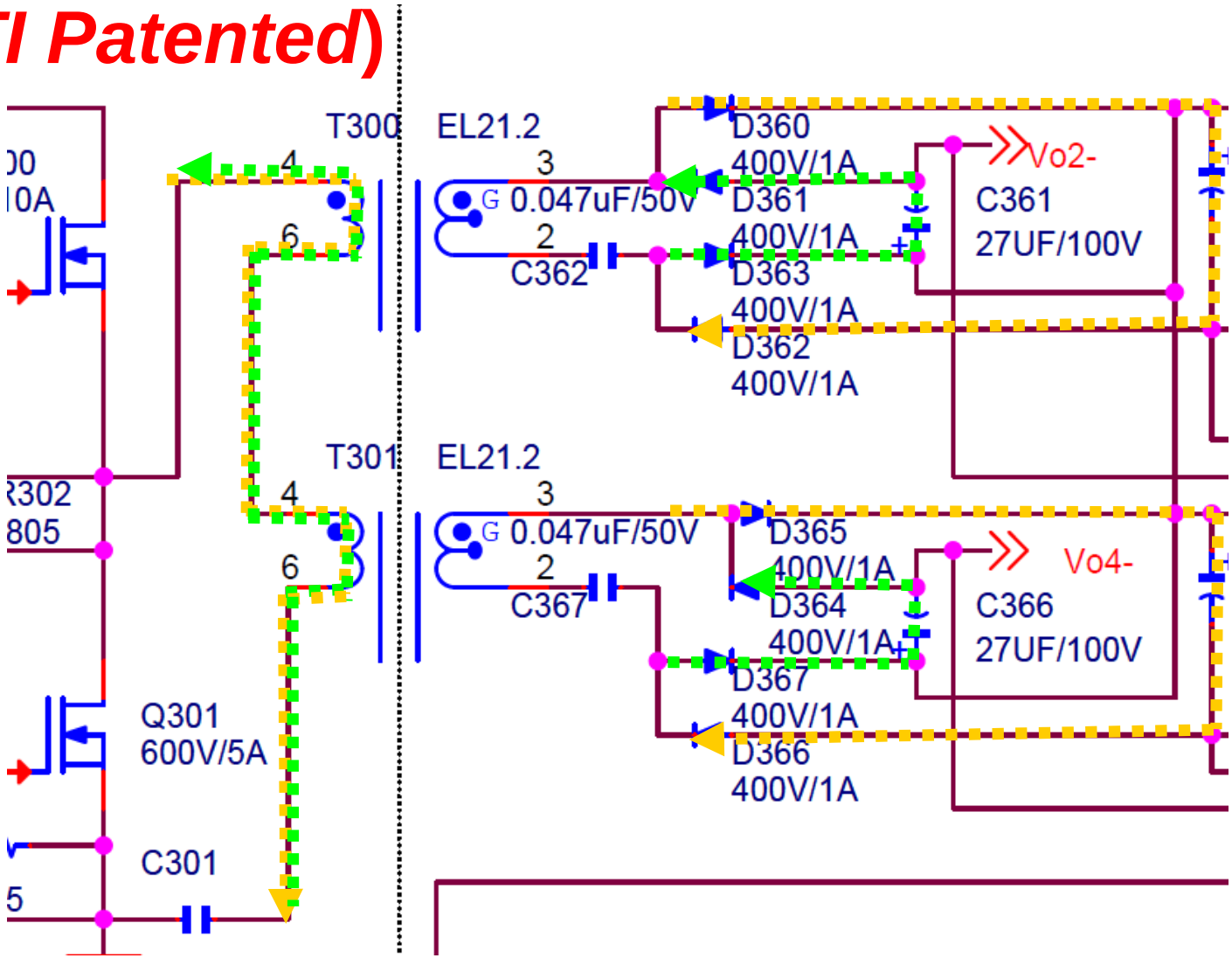
- Why transformer can Balancing Current
- Multi-Transformer Architecture
- Why Current is not serious Influenced by Inductance

Why Transformer Can Balance Current

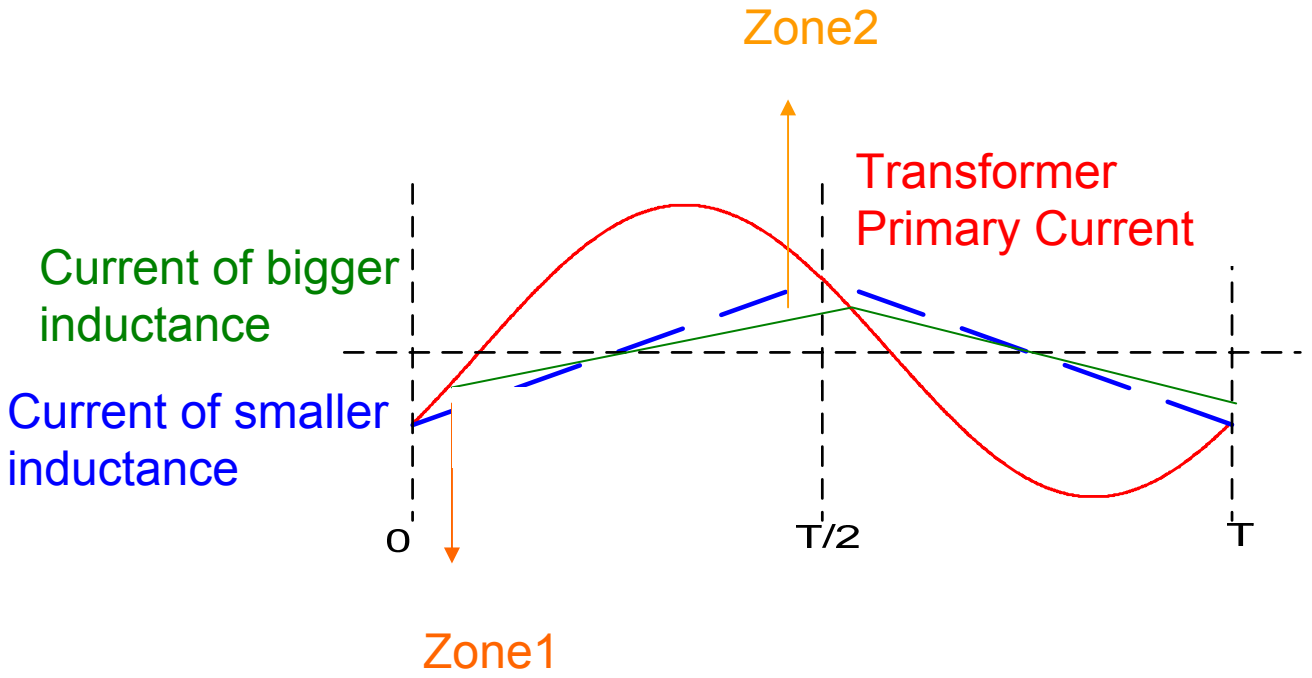


- Transformer current is in reverse proportion to turn ratio
- Ip/Np = Is/Ns; Is=Ns*Ip/Np
- When transformer primary is connected together, their primary current must be the same
- When T1 is the same as T2 because of transformer operation principle their secondary current is the same
- Is1=Ns*Ip/Np=Is2

Multi-Transformer Architecture (*TI Patented*)



Why Current is not serious Influenced by Inductance



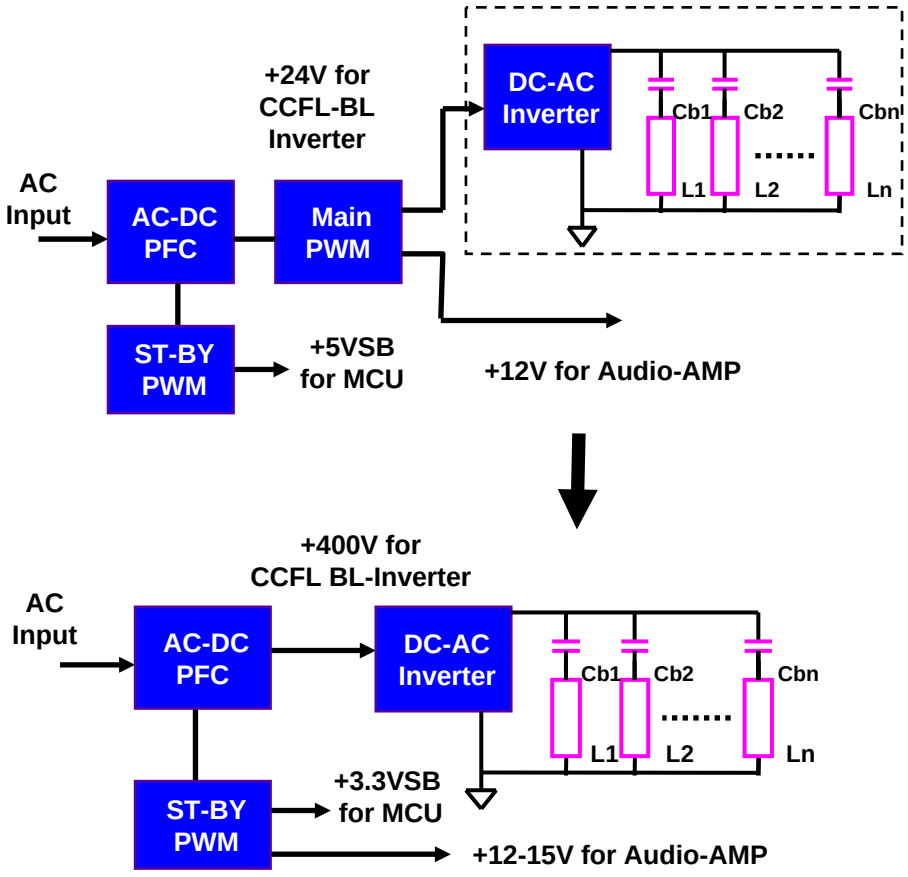
Because Zone1 is almost same as Zone2, inductance not series influence output current

Advantage **Compare to Traditional Driver**

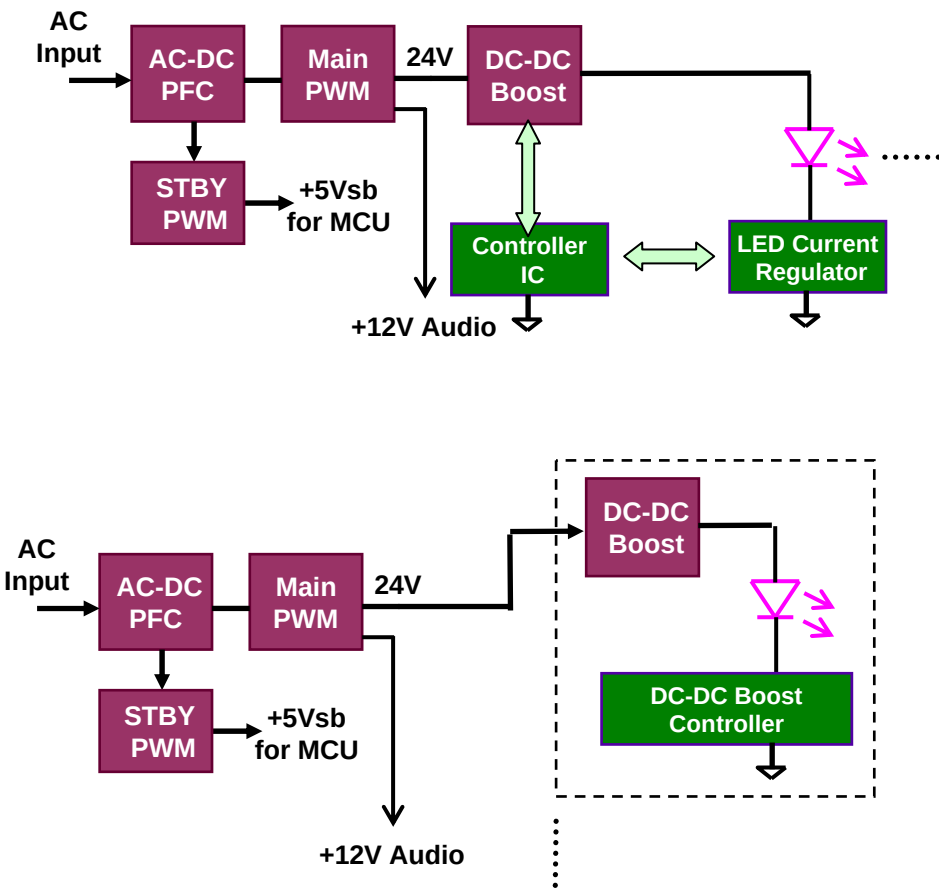
- **Solutions for Back Light Driver**
- **LED Back Light Comparison**

Solutions **for Back Light Driver**

Power Supply Unit/ LIPS Architecture for LCD-TV

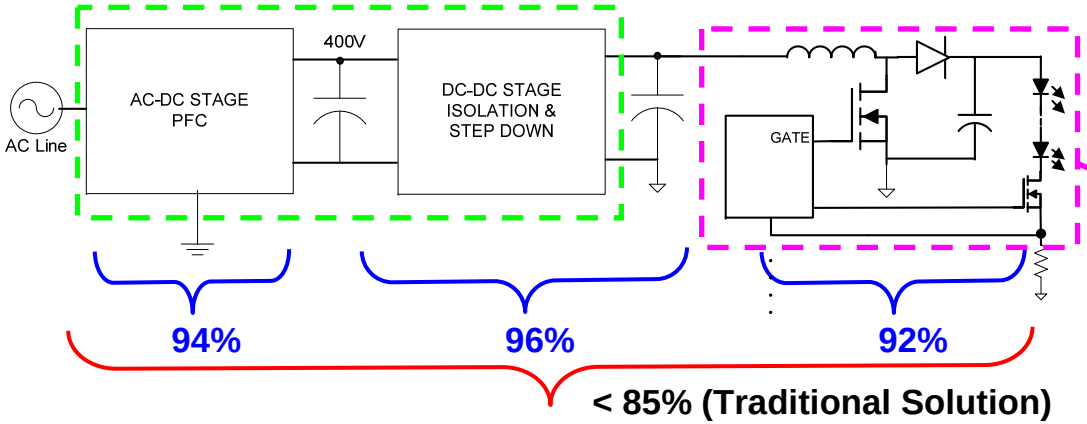


Power Supply Architecture for LED Backlighting TV Today

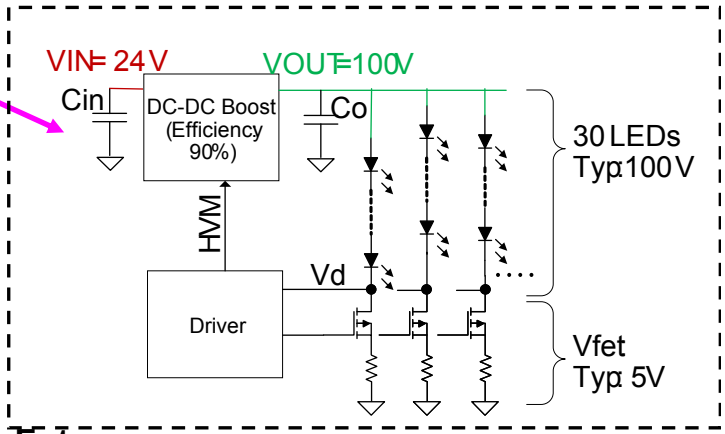


LED **Back Lingt Comparison**

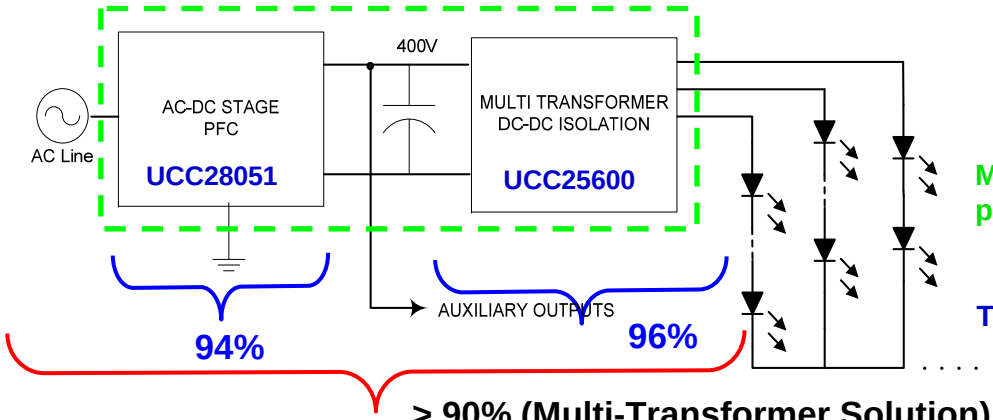
Power Supply Architecture for LED Backlighting TV Today



1* DC Boost + 8-16 LED Current Regulators



Power Supply Architecture for LED Backlighting TV in the Future



Multi-transformer outputs designed on AC/DC LIPS power module (higher efficiency & low cost) inside DTV.

Today- UCC25600

Advantage Compare to Traditional Driver

- Transformer Design
- Key Component selection
- Feedback and Dimming
- Protection

Transformer Design

For LLC transformer design, firstly we should transfer all parameter into the same unit. In this case we transfer all parameter into primary resistance.
Considering 88V, 120mA load and two outputs for each transformer means each transformer output power is $P_{out} = 2 * V_{out} * I_{out} = 22.2316W$

Because there are four transformers in series and half-bridge topology, we got following equation.

$R_L = P_{out} / (V_{in})^2$ $V_{in} = 400V / 4(inseries) / 2(halfbridge) = 50V$ $R_L = 112.453\Omega$

To analyze LLC behavior easily we set $Q = \frac{\omega L_k}{R_L}$ $K = \frac{L_m}{L_k}$

L_k means leakage inductance, L_m means magnetizing inductance.

In normal design we set frequency to 110K Hz to avoid 150K EMI conduction issue and also minimize transformer size.
Also set Q to 0.2 and K to 5 for better efficiency and enough hold up time.

From the equation of Q we got

$$L_m = K \times L_K = 163.225\mu H \qquad L_k = \frac{Q \times R_L}{\omega} = \frac{0.2 \times 112.453}{2 \times \pi \times 110000} = 32.645\mu H$$

Transformer Design

DC gain of LLC converter $M = \frac{V_0}{V_i}$ and $\omega_n = \frac{f}{f_o}$

f_o is the resonant frequency and it is equal to 110K Hz

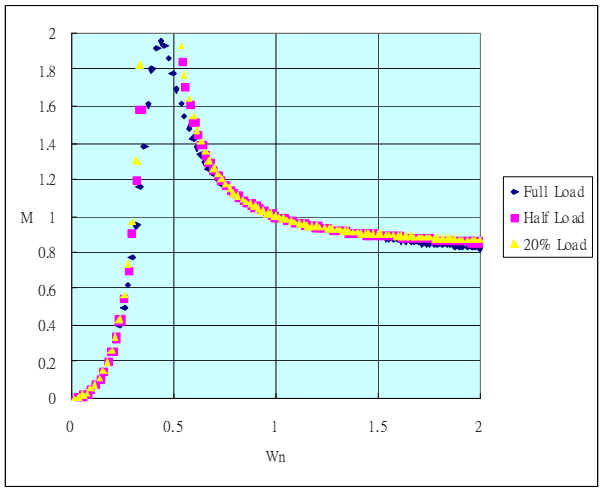
ω_n means normalized frequency

According the graph, maximum DC gain happens when $\omega_n = 0.44$

Minimum switching frequency is set as $\omega_n = 0.51$

to keep enough margin.

So the Minimum switching frequency is $f_{\min} = 110K \times 0.51 = 56.1KHz$



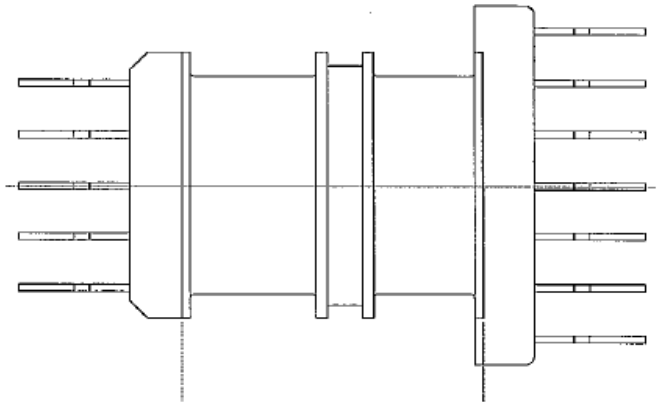
$V_{in} = 50V$ same as calculated above, maximum switching cycle can be calculated as $t = \frac{1}{2 \times f_{\min}} = 8.913\mu s$

Flux density B set as 0.5T because the flux can be both negative and positive. Cross-section area A is 30.1mm^2 according to the transformer we choose

According to transformer basic operation rule $V_{in} \times t \le N \times B \times A$

$N \ge \frac{V_{in} \times t}{B \times A} = 30turns$ to avoid saturated.

Transformer Design



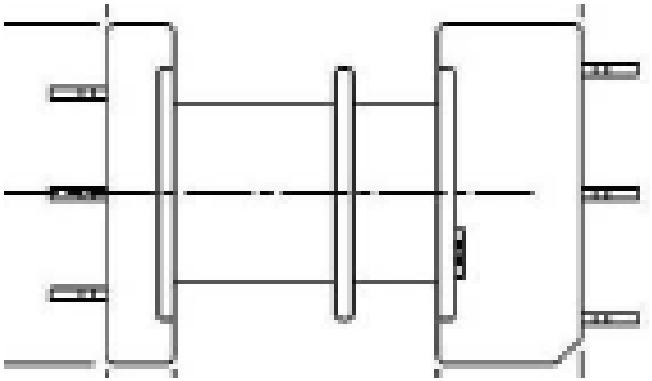
Leakage Inductance is high

Use additional cap to isolate

Can not assemble automatically

Litz wire to avoid eddy current

Fit for higher output power



Leakage Inductance is low

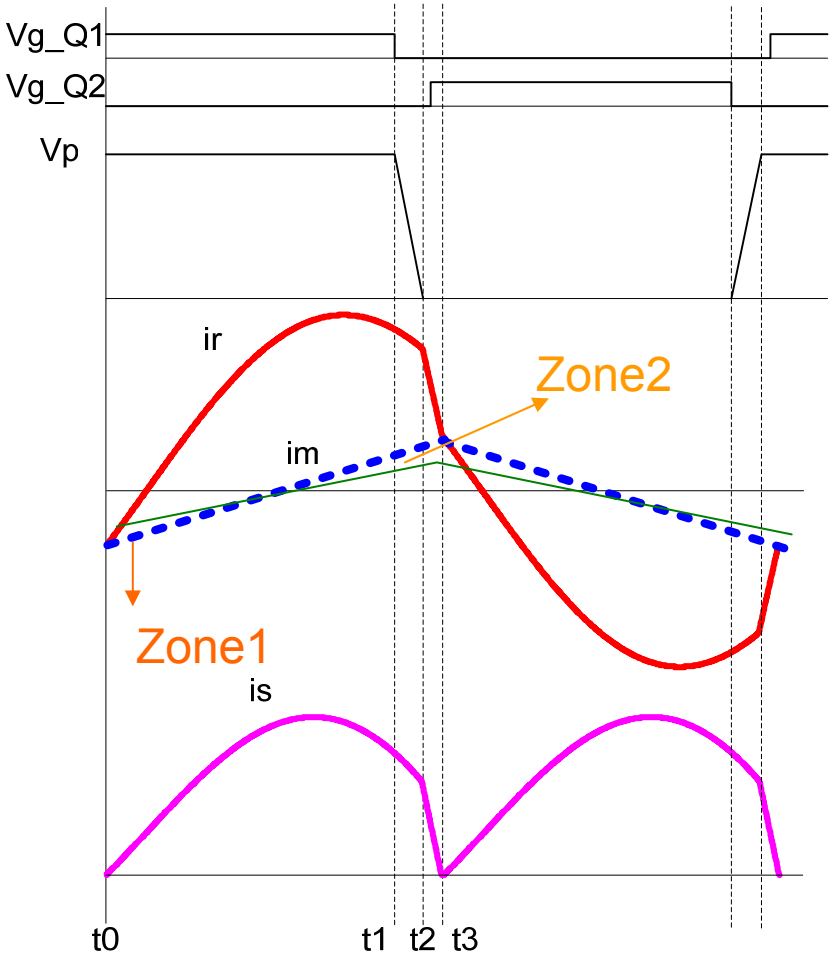
Use isolated wire to isolate

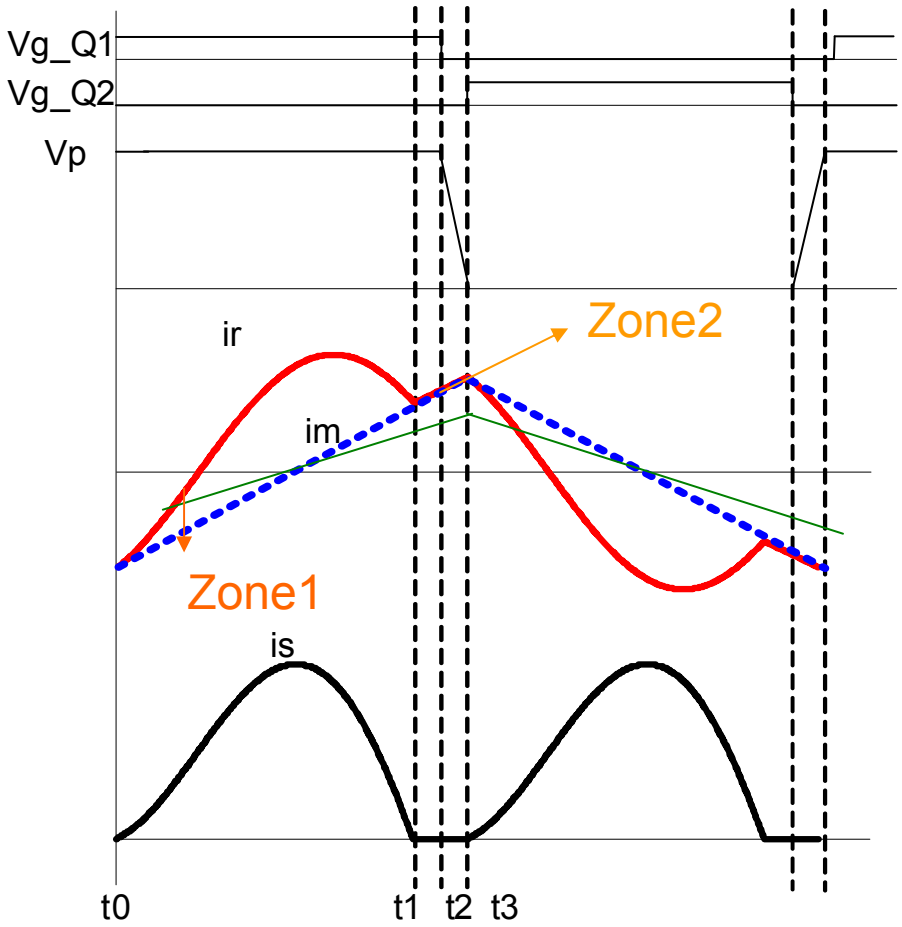
Assemble automatically

Thin line to avoid eddy current

Fit for smaller output power

Transformer Design





While CCM Zone1 and Zone2 is still almost the same but while DCM Zone1 and Zone2 with obvious different that is why current is more unbalance when DCM.

Transformer Design

1. B1 PFC Vout maximum

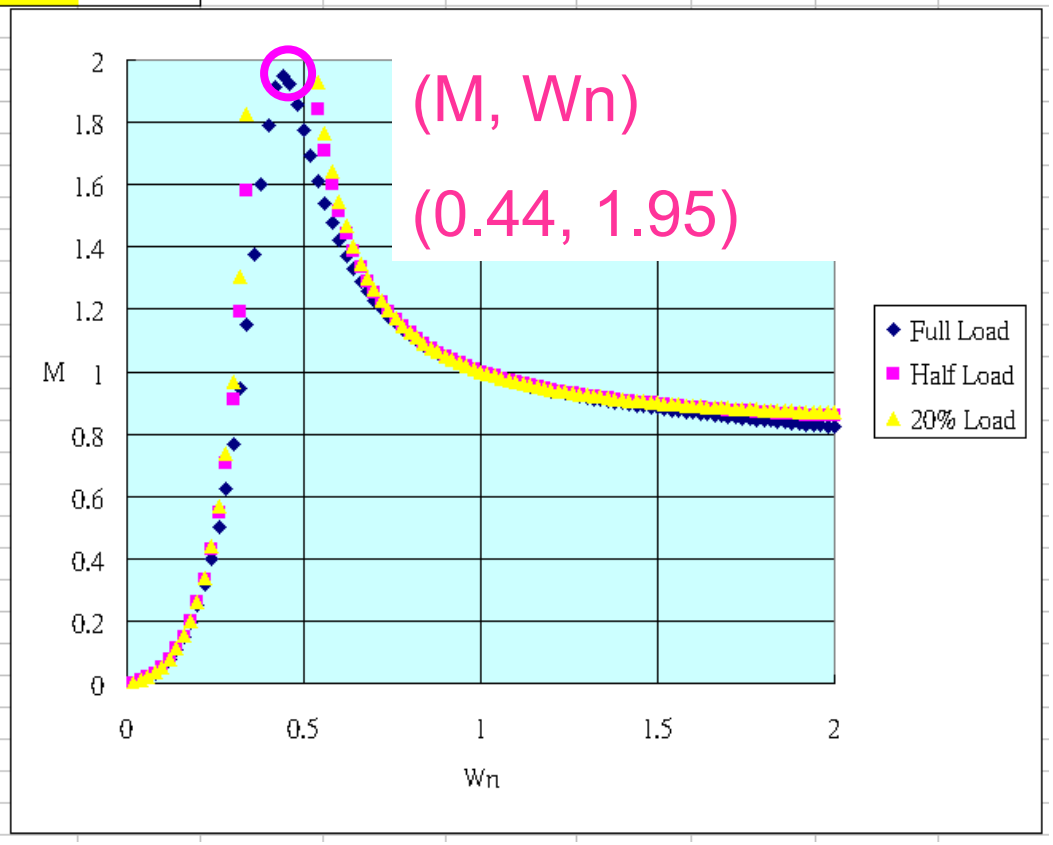
2. C1 How many transformer in series

3. A3 output voltage

4. B3 output current per transformer for dual output design it should be doubled

5. A5 output diode Vf for there are 2 diodes in series it should be doubled

	A	B	C	D	E	F	G
1	Vin_max	400	4	Transformers		Each	100 V
2	Vo1	Io1	Vo2	Io2	Vo3	I	
3	88	0.24	0	0			
4	Vf1		Vf2		Vf3		
5	2						
6	Pout	21					
7	Pin	22.2316					
8	RL	112.453	Ω				
9	F	110	KHz				
10	Q	0.2145	(wL/RL)		Lk	35.01128	uH
11	K	5	Lm/Lk		Lm	175.0564	uH
12							nF
13	Wn_						
14	M_m						V
15	B=	0.3	T				
16	Ae=	30.1	mm*mm				
17	V=	50	V				
18	t=	8.91266	uS	fmin=	56.1	k	
19	N>	29.6102					
20	Primary turns		30	turns			
21	Winding turns			Winding RMS current			
22	Output1	54	turns	Output1	0.2664	A	
23	Output2	0	turns	Output2	0	A	
24	Output3	0	turns	Output3	0	A	
25	Output4	0	turns	Output4	0	A	
26							
27	Bulk Cap	78	uF				
28	Bulk Cap minima voltage			385	V		
29	other output		60	W			
30	Hold up time		24.8548	mS			
31							



Transformer Design

	A	B	C	D	E	F	G	H
1	Vin_max	400	4	Transformers		Each	100	V
2	Vo1	Io1	Vo2	Io2	Vo3	Io3	Vo4	Io4
3	88	0.24	0	0				
4	Vf1		Vf2		Vf3			
5	2		0					
6	Pout	21.12		Eff	0.95			
7	Pin	22.2316						
8	RL	112.453	Ω					
9	F	110	KHz					
10	Q	0.2145	(wL/RL)		Lk			
11	K	5	Lm/Lk		Lm			
12					C			
13	Wn_min	0.51						
14	M_max	1.73237		Min working voltage				
15	B=	0.5	T					
16	Ae=	30.1	mm*mm					
17	V=	50	V					
18	t=	8.91266	uS	fmin=				
19	N>	29.6102						
20	Primary turns		30	turns				
21	Winding turns			Winding RMS				
22	Output1	54	turns	Output1				
23	Output2	0	turns	Output2				
24	Output3	0	turns	Output3				
25	Output4	0	turns	Output4				
26								
27	Bulk Cap	78	uF					
28	Bulk Cap minima voltage			385				
29	other output		60	W				
30	Hold up time		24.8548	mS				
31								

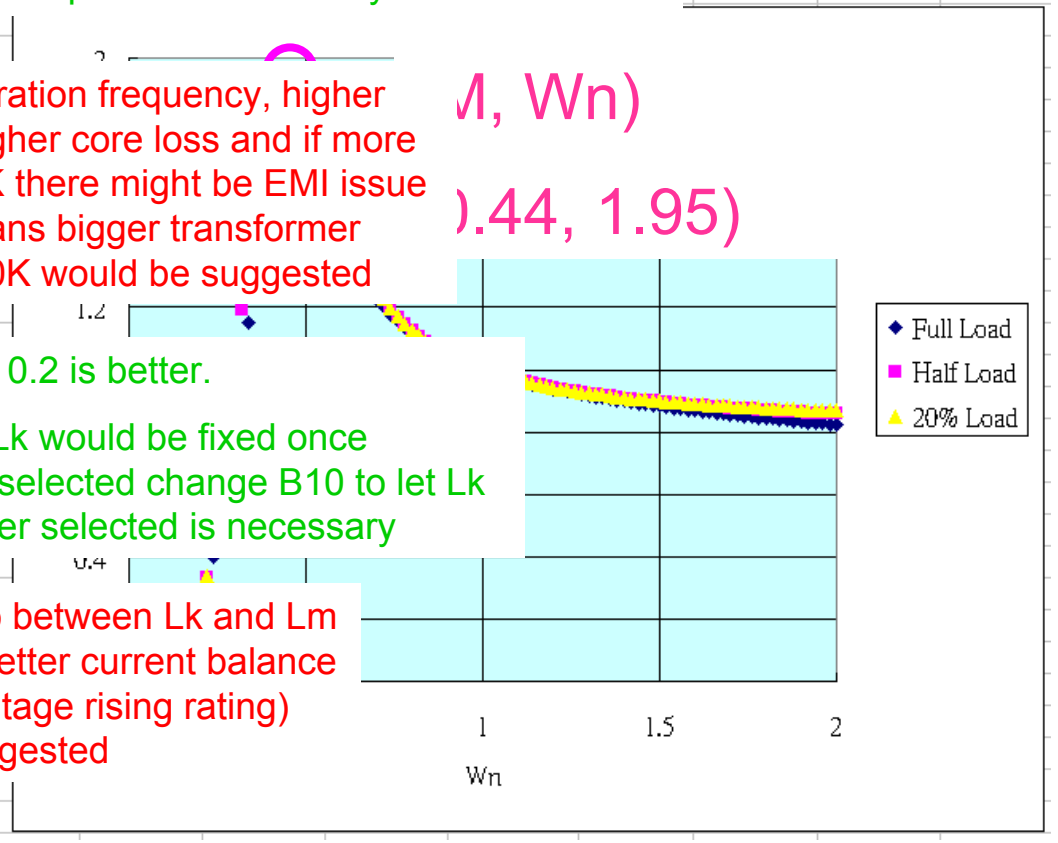
6. E6 is predicted efficiency

7. B9 operation frequency, higher means higher core loss and if more than 150K there might be EMI issue lower means bigger transformer 100K~120K would be suggested

8. B10 choose 0.2 is better.

Because F10 Lk would be fixed once transformer is selected change B10 to let Lk fit to transformer selected is necessary

9. B11 K is ratio between Lk and Lm bigger means better current balance but lower M (voltage rising rating) choose 5 is suggested



Transformer Design

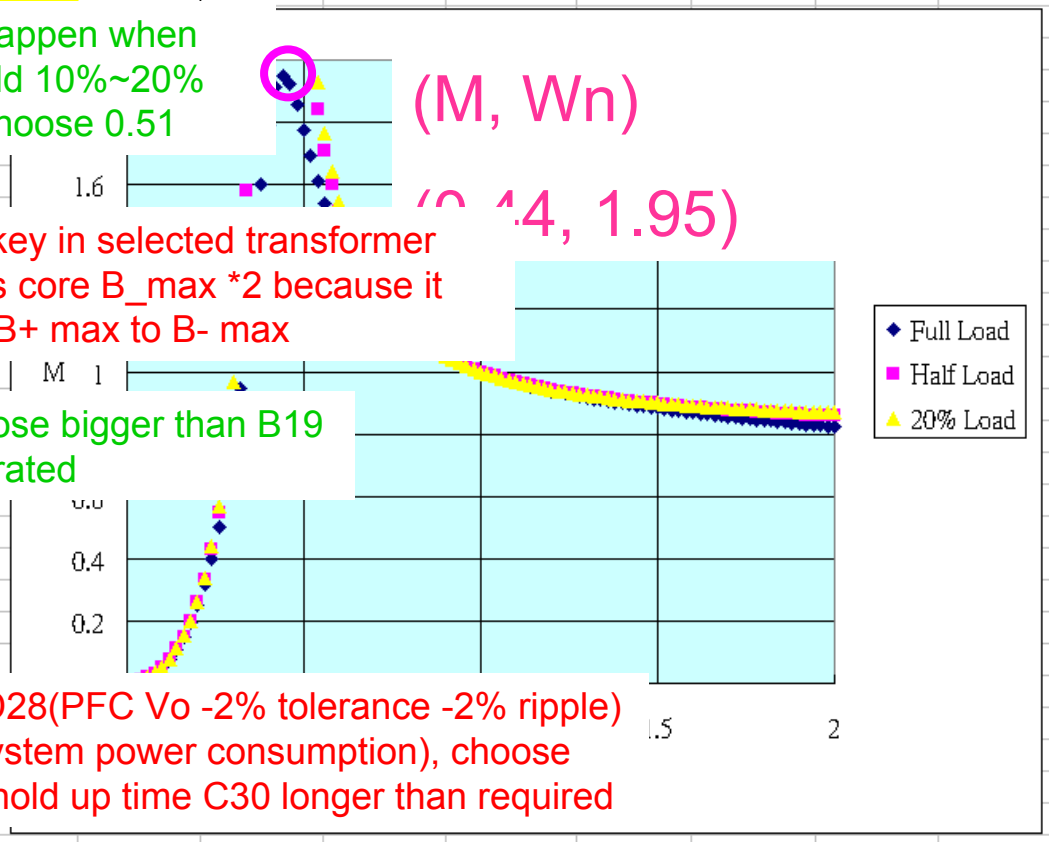
	A	B	C	D	E	F	G	H
1	Vin_max	400	4	Transformers		Each	100	V
2	Vo1	Io1	Vo2	Io2	Vo3	Io3	Vo4	Io4
3	88	0.24	0	0				
4	Vf1		Vf2		Vf3		Vf4	
5	2		0					
6	Pout	21.12		Eff				
7	Pin	22.2316						
8	RL	112.453	Ω					
9	F	110	KHz					
10	Q	0.2145	(wL/RL)					
11	K	5	Lm/Lk		Lm	175.0564	uH	
12								
13	Wn_min	0.51						
14	M_max	1.73237		Min work				
15	B=	0.5	T					
16	Ae=	30.1	mm*mm					
17	V=	50	V					
18	t=	8.91266	uS	fmin=				
19	N>	29.6102						
20	Primary turns		30	turns				
21	Winding turns			Winding RMS current				
22	Output1	54	turns	Output1	0.2664	A		
23	Output2	0	turns	Output2	0	A		
24	Output3	0	turns	Output3	0	A		
25	Output4	0	turns	Output4	0	A		
26								
27	Bulk Cap	78	uF					
28	Bulk Cap minima voltage			385	V			
29	other output		60	W				
30	Hold up time		24.8548	mS				
31								

10. B13 M_max happen when Wn is 0.44 and add 10%~20% for de-rating, so choose 0.51

11. B15 and B16 key in selected transformer data, notice B15 is core B_max *2 because it can operate from B+ max to B- max

12. C20 Choose bigger than B19 to avoid saturated

13. Key in D28(PFC Vo -2% tolerance -2% ripple) and C29 (system power consumption), choose B27 to key hold up time C30 longer than required



Resonant Capacitor Selection

- Capacitance calculated by transformer design tool
- Voltage rating should be 1.2* maxima voltage on resonant capacitor.
- Ripple current rating should over (output watts/200) * 1.5
- Arco R75, R76 or Panasonic ECWH or other capacitor with high ripple current rating is suggested.

DC Blocking Capacitors

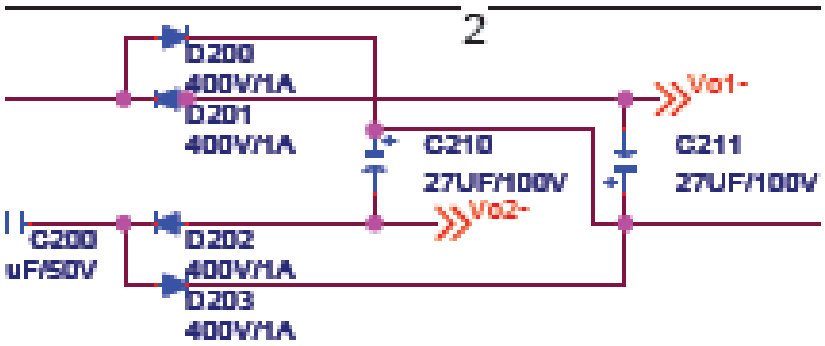
- Capacitance value ~ 1 to 3% of C_{OUT} of each channel
  - Large enough for 10% maximum ripple voltage
  - Small enough to settle quickly
- Voltage stress: Equal to VOUT to keep margin during single output short.
- Ripple current stress: 2.5* output current

Output Capacitor selection

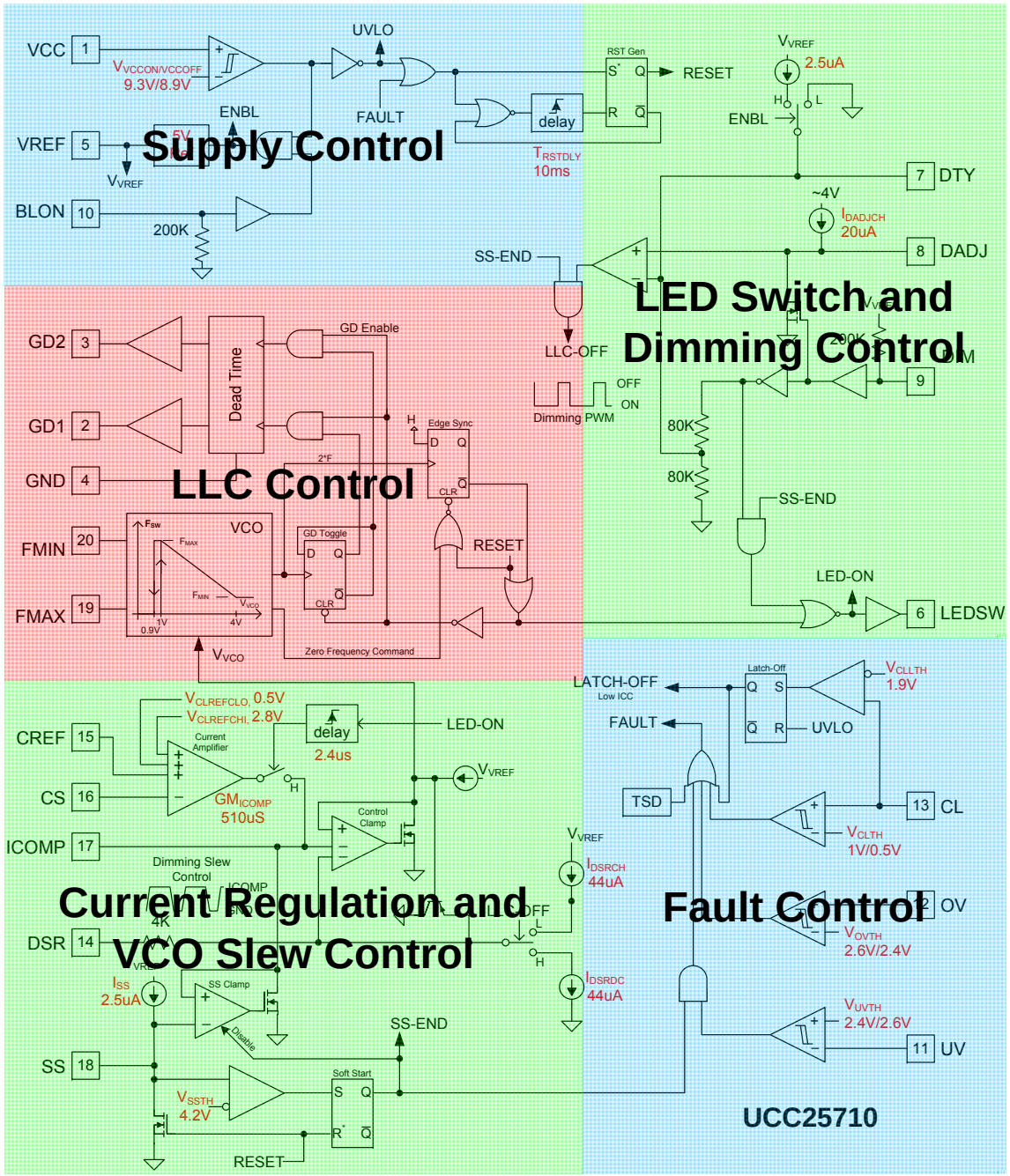
- Voltage rating should be 1.25 * output voltage to keep margin
- Ripple current on capacitor is 1.2* output current
- Use ripple current rating as 1.5* output current for margin

Output Rectifier Selection

- Reference design D200~D215
- Super-fast recovery
- 2.5* output voltage
- 1A rating above
- Trr 35ns
- Why?
  - Higher efficiency
  - Better current matching at low duty cycle dimming



UCC25710 Block Diagram



AUDIBLE NOISE REDUCTION

- It is desirable to turn the LLC controller ON and OFF during dimming to improve efficiency and allow a fast LED current loop
- This can cause audible noise during the ON and OFF transitions
- Controlled and programmable rise and fall times on the VCO control input are used to reduce any mechanical stimulation
- It is anticipated that typical slew times of 100us to 300us would be used

LOW DUTY-CYLE DIMMING

- Low duty-cycle dimming presents a problem
  - Dimming ON pulses are very short
  - Can’t deliver short full-power pulses
  - Dimming linearity falls off at the low end if power stages are ramped versus stepped
- Example:
  - 1% PWM dimming at a 240Hz rate forces an LED current pulse width of 42us (1/24KHz)
  - This would require a very fast full power ON and OFF
  - Controlling audible noise may be difficult

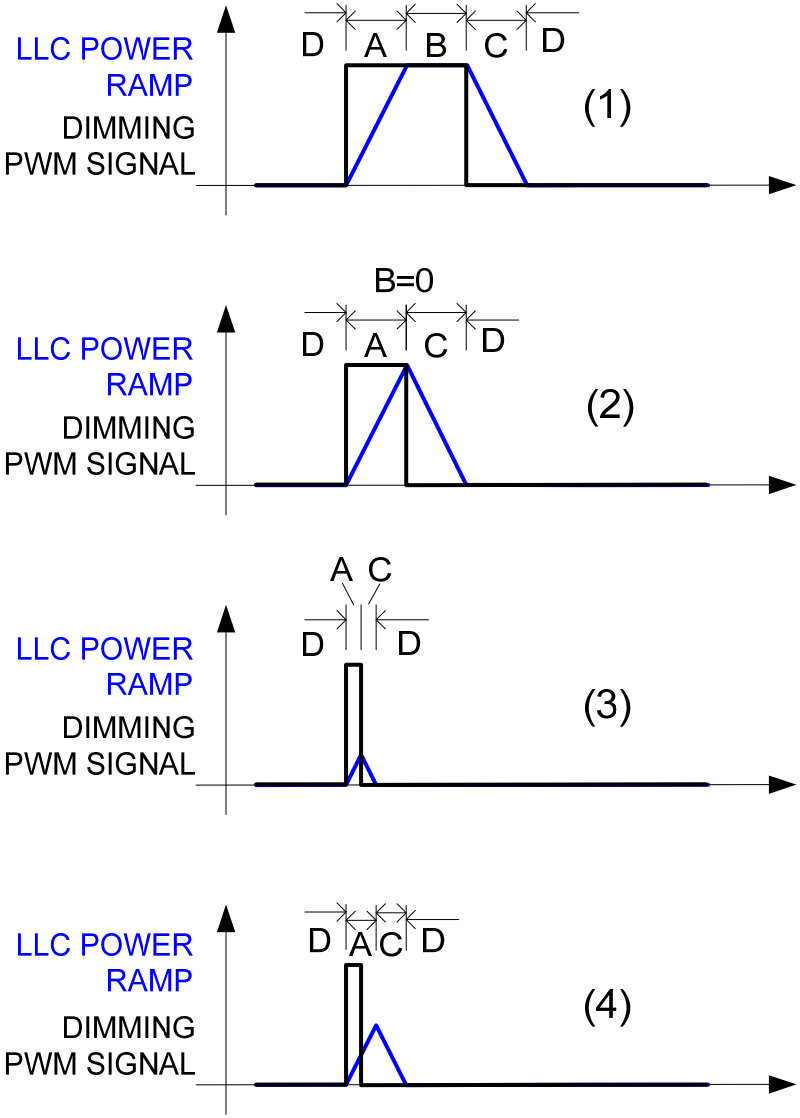
LOW DUTY-CYLE ILLUSTRATION

1. LLC reaches power level equal to pedestal LED current in region B. Power is under delivered in region A, but is compensated for in region C

2. Region B is zero, but sum of A+C still deliveries correct energy.

3. Energy delivered in region A + C is too low, loop is open and realized peak LED current will drop

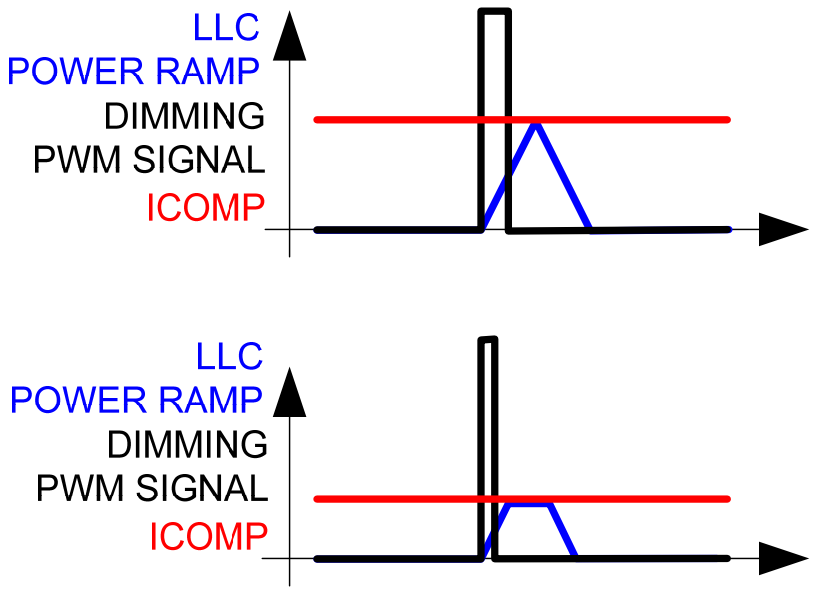
4. On-time is extended. A + C energy/pulse is correct to maintain same peak LED current



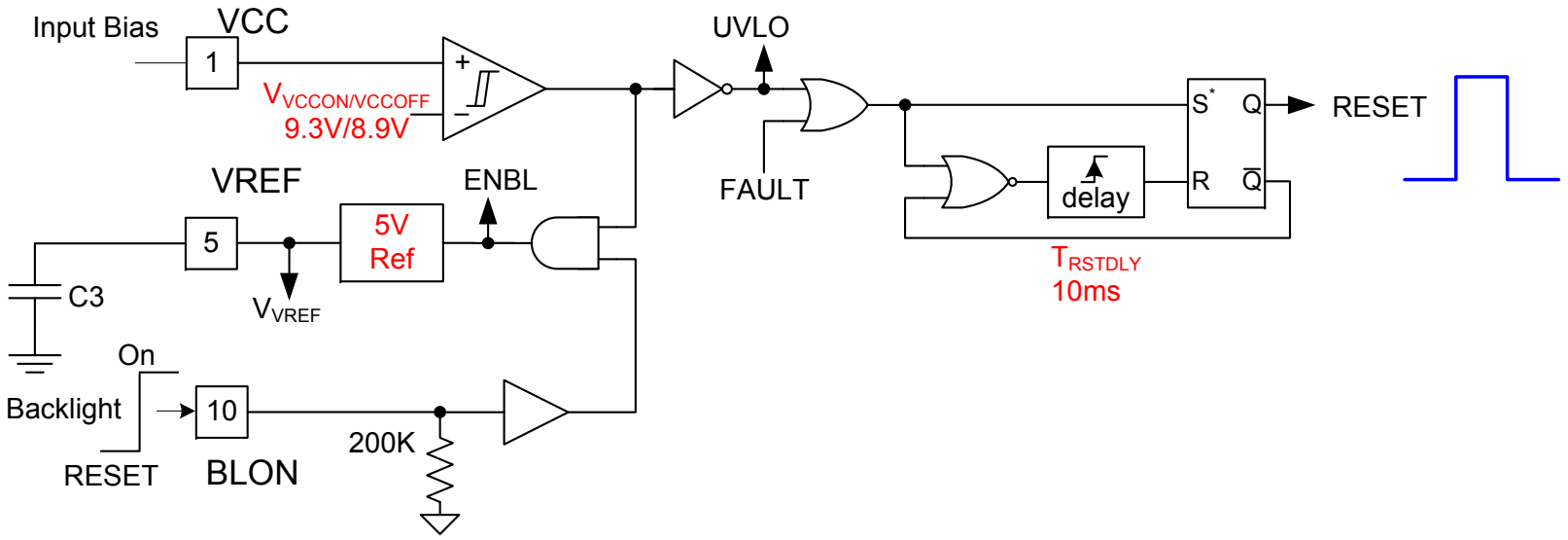
LOW DUTY-CYLE DIMMING SOLUTION

- ICOMP is the compensation node of the current loop
- ICOMP is connected to the loop amplifier during the LED on-time and floated during the LED off-time
- ICOMP responds to the error in the pedestal LED current and controls the energy delivered during a dimming pulse as long as the ramp reaches ICOMP
- By extending the LLC on-time ICOMP can still control the LLC energy per dimming cycle
- There are implications on loop bandwidth.

  Experiments/Data shows that increasing bandwidth increases the primary current peak at the beginning of the DIM cycle



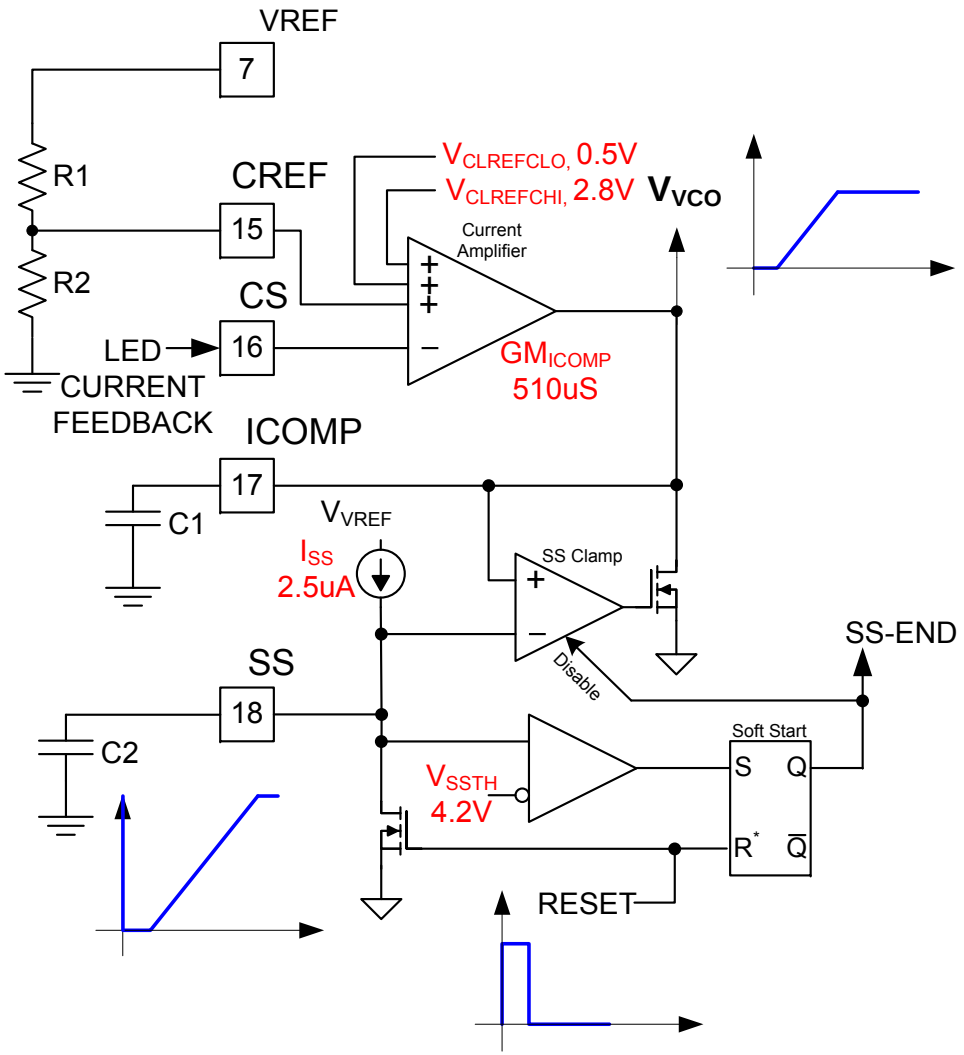
START-UP, UVLO & POR



- UVLO is high until VCC rises to 9.3V or when VCC falls to 8.9V
- Crossing the UVLO threshold L-H initiates a 10mS RESET pulse
- The BLON, backlight on, input can be used to shutdown the controller and LEDSW
- BLON low and UVLO turn OFF the 5V ref

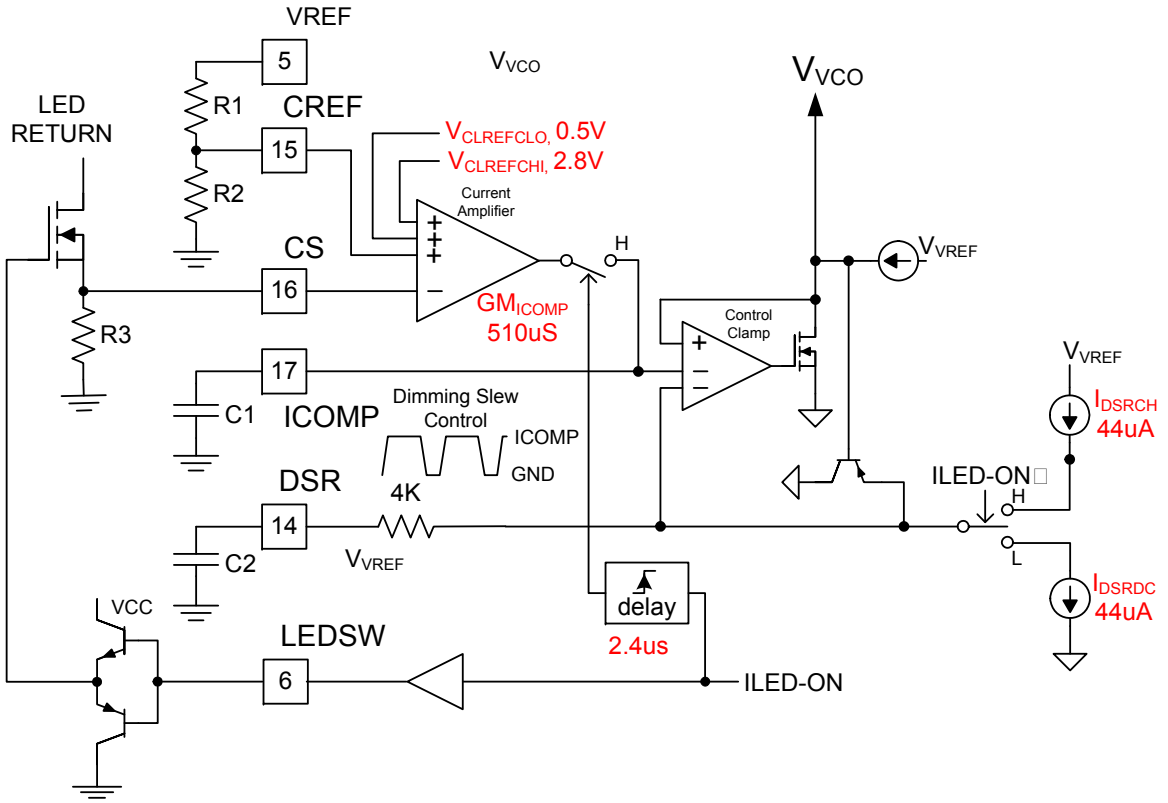
START-UP, SOFT-START

- RESET discharges SS
- SS over-rides the gm amplifier and pulls V_{VCO} low
- A 2.5uA current source charges SS after RESET
  - Resistor from VREF can shorten SS
- When SS > ICOMP, ICOMP gains control of the loop
- When SS = 4.5V, end soft-start, SS clamp is disabled



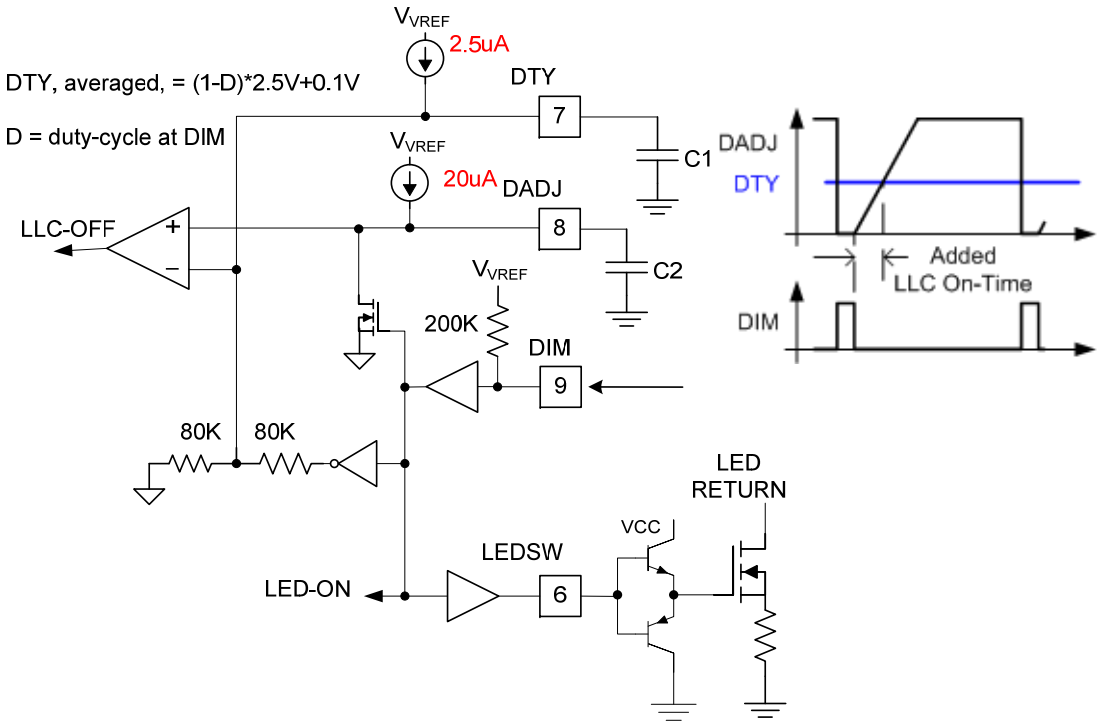
DIMMING – LLC ON/OFF TRANSITION & CURRENT CONTROL

- The DIM input controls the ILED-ON an ILED-ON` signals.
- DSR capacitor C2 and internal 44uA currents control the slew rate of V_{VCO} during dimming off and on transitions.
  - Turn-off: DSR is discharged to GND by 44uA
  - Turn-on: DSR is charged to ICOMP by 44uA. Charge level is clamped to 1Vbe above ICOMP
- Control Clamp output, V_{VCO}, tracks the lower of ICOMP and DSR
- ICOMP is only driven by GM amp during LED-ON times.
- During LED-OFF times the ICOMP voltage is held by C1



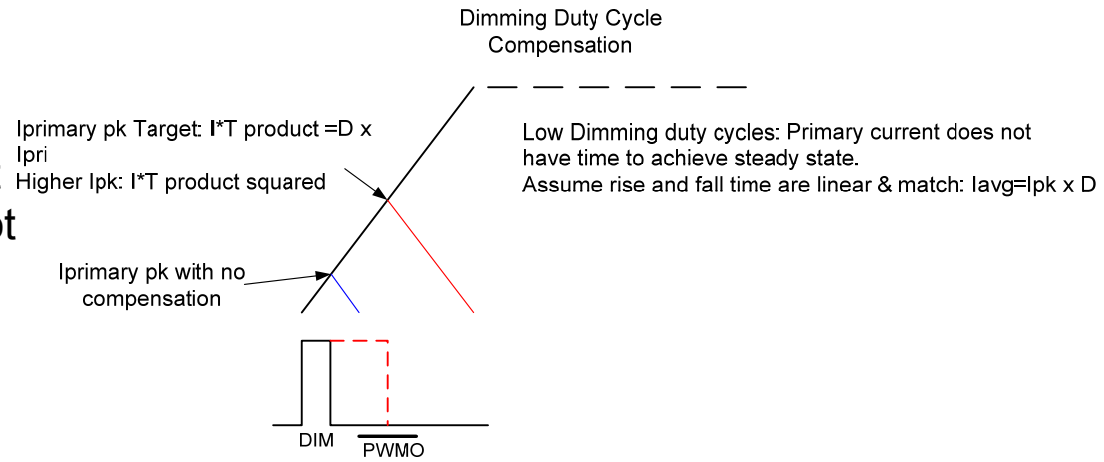
DIMMING – LLC ON-TIME EXTENSION

- DIM input controls the LEDSW output
- LEDSW output is a rail to rail signal but not is high current
- DTY is a scaled and averaged voltage proportional to 1- D, D = dimming duty-cycle
- LLC on-time is extended until ramp at DADJ exceeds DTY
- The on-time extension is proportional to 1-D, and is programmable with C2



DIMMING – LLC ON-TIME EXTENSION

- Basis of equation for DADJ capacitor value shown in drawing.
- At low dimming, assume that steady state Ipri current is not achieved
- Rise and fall time of Ipri current is the same



- The equation for DTY capacitor value is shown. Target low ripple voltage since a DC voltage is expected. Suggest ~100mV target. There is a tradeoff of low ripple on DTY and response time to large changes in DIM duty cycle.

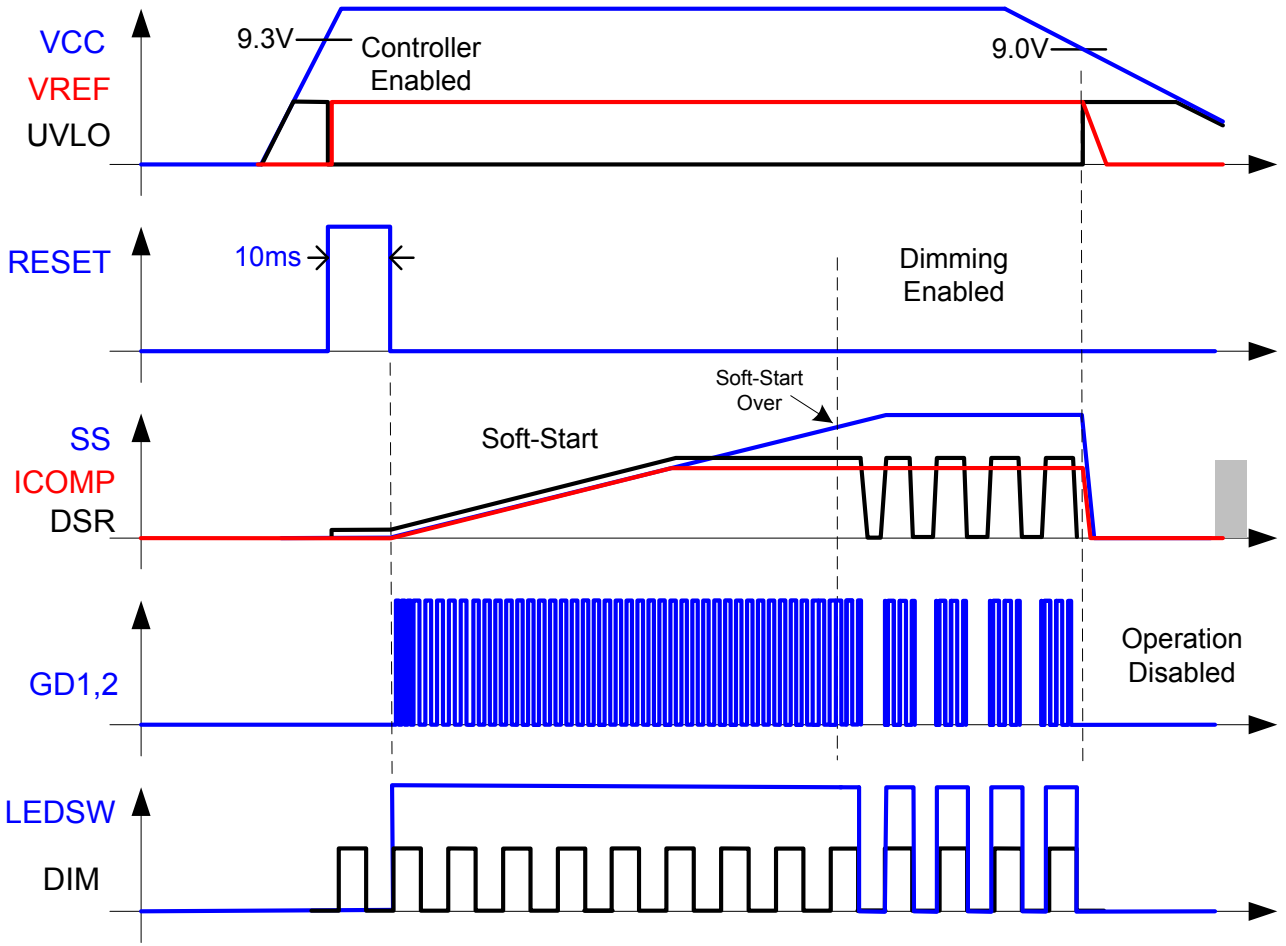
$$C_{DADJ} = \frac{20uA \times \left(\sqrt{\frac{DIM_{DMIN} \times T_{RISE}}{F_{DIM}}} - \frac{DIM_{DMIN}}{F_{DIM}} \right)}{\left[\left(1 - DIM_{DMIN}\right) \times 2.5V \right] + 0.1V}$$

$$C_{DTY} = \frac{31.3uA \times \frac{0.5}{F_{DIM}}}{V_{DTYp-p}}$$

START-UP & DIM WAVEFORMS

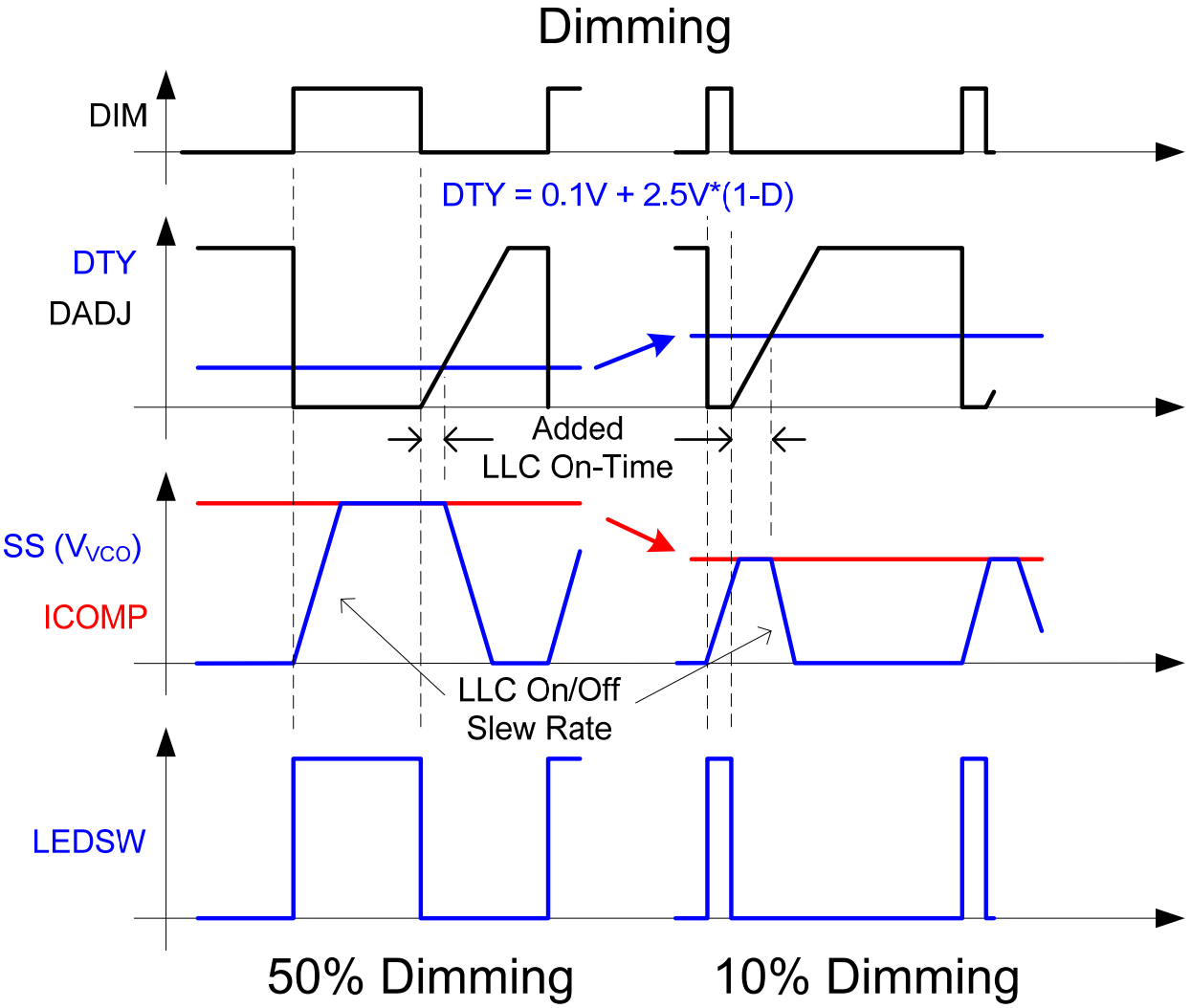
- 10ms RESET initiates Soft-Start (SS)
- LLC Soft-Start, VCO control is clamped to SS until SS > ICOMP
- Dimming is disabled during SS
- DSR cap is used to limit LLC control slew rate during dimming
- ICOMP voltage is maintained during dimming

Start-up and UVLO Shutdown



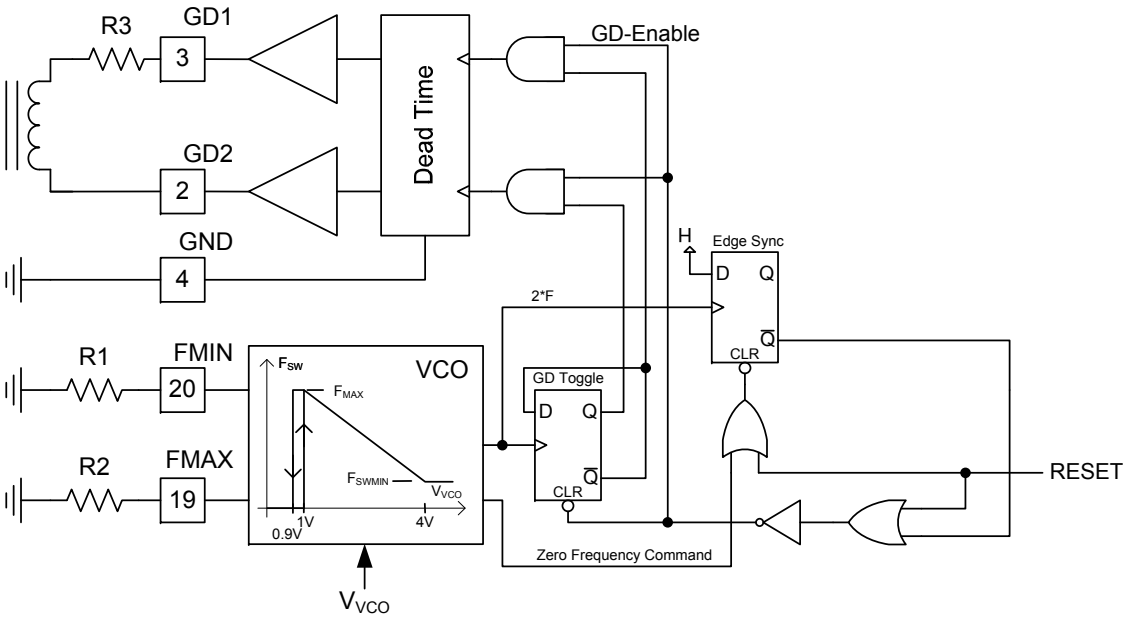
DIMMING – WAVEFORMS

- DIM input controls LEDSW
- DIM input triggers soft turn-on and turn-off of LLC converter
- LLC on-time is extended
- On-time extension is proportional to 1-D, D is dimming duty-cycle
- Extended on-time allows ICOMP to maintain current regulation at low D



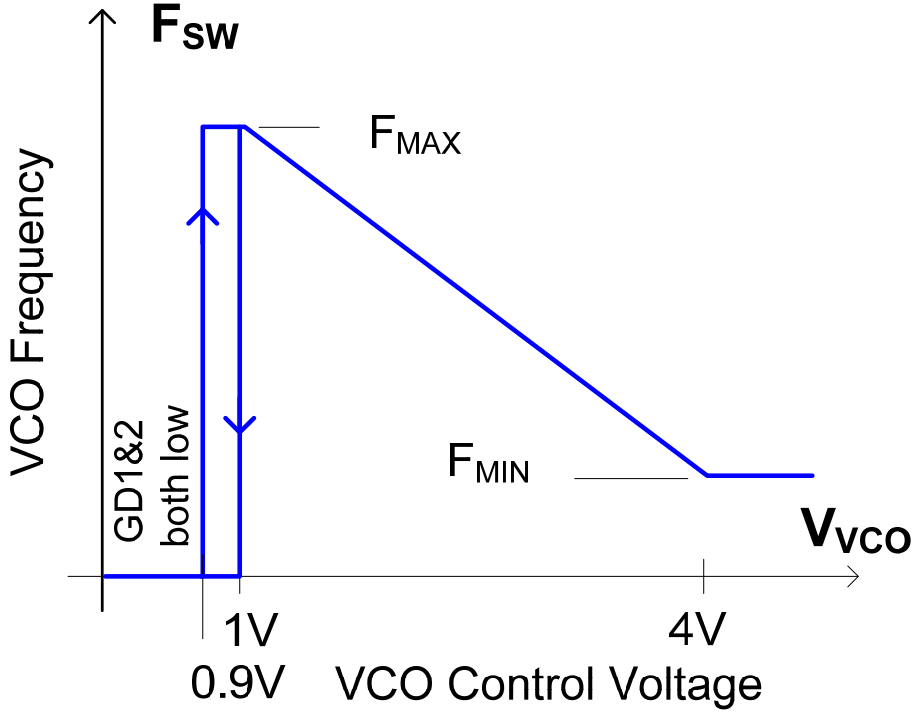
LLC DRIVE

- Programmable VCO
- 14Ω/4Ω Gate Drives
- Gate drives are shifted by 180 degrees with 500ns fixed dead-time
- Gate drives both go low on a RESET command
- GD2 will always come on first after a RESET pulse



LLC FREQUENCY CONTROL

- Linear frequency control for V_{VCO} 1V to 4V
- Programmable minimum and maximum Frequencies
  - F_{SWMIN} ~25-60KHz @ 3%
  - F_{SWMAX} ~250-450KHz @ 7.5%
- Frequency = F_{MIN} for V_{VCO} >4V
- Frequency = F_{MAX} for V_{VCO} <1V and >0.9V
- Frequency goes to Zero for V_{VCO} < 0.9V

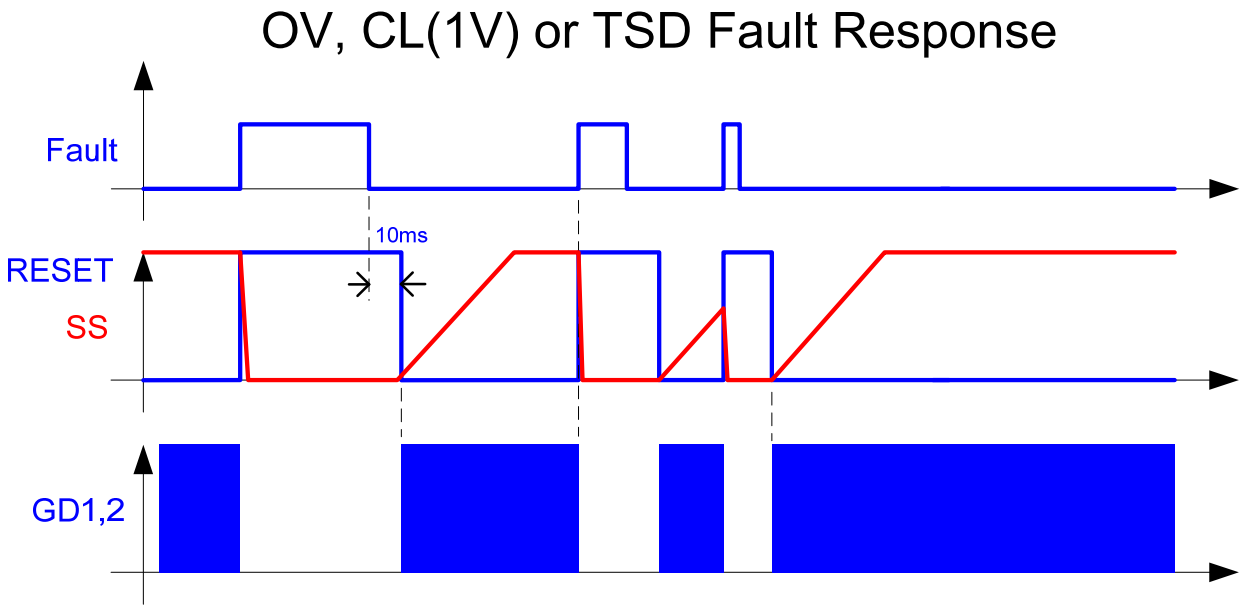


FAULT MANAGEMENT

- Faults
  - OV – highest LED string voltage
  - UV – lowest LED string voltage
  - CL(1V) – input current signal over-current
  - CL(2V) – input current signal latch-off
  - TSD – Chip thermal shutdown
- Response
  - OV, CL(1V) & TSD: The LLC converter and LEDSW are turned off. When the fault clears a RESET and SS are initiated.
  - UV: The LLC converter and LEDSW are turned off. A RESET and SS are immediately initiated, repeatedly, until fault clears.
  - CL(2V): The LLC and LEDSW are latched off until UVLO recycles.
  - During RESET the LLC converter and LEDSW are OFF
  - During SS the LLC converter and LEDSW are ON, i.e. no DIMMING

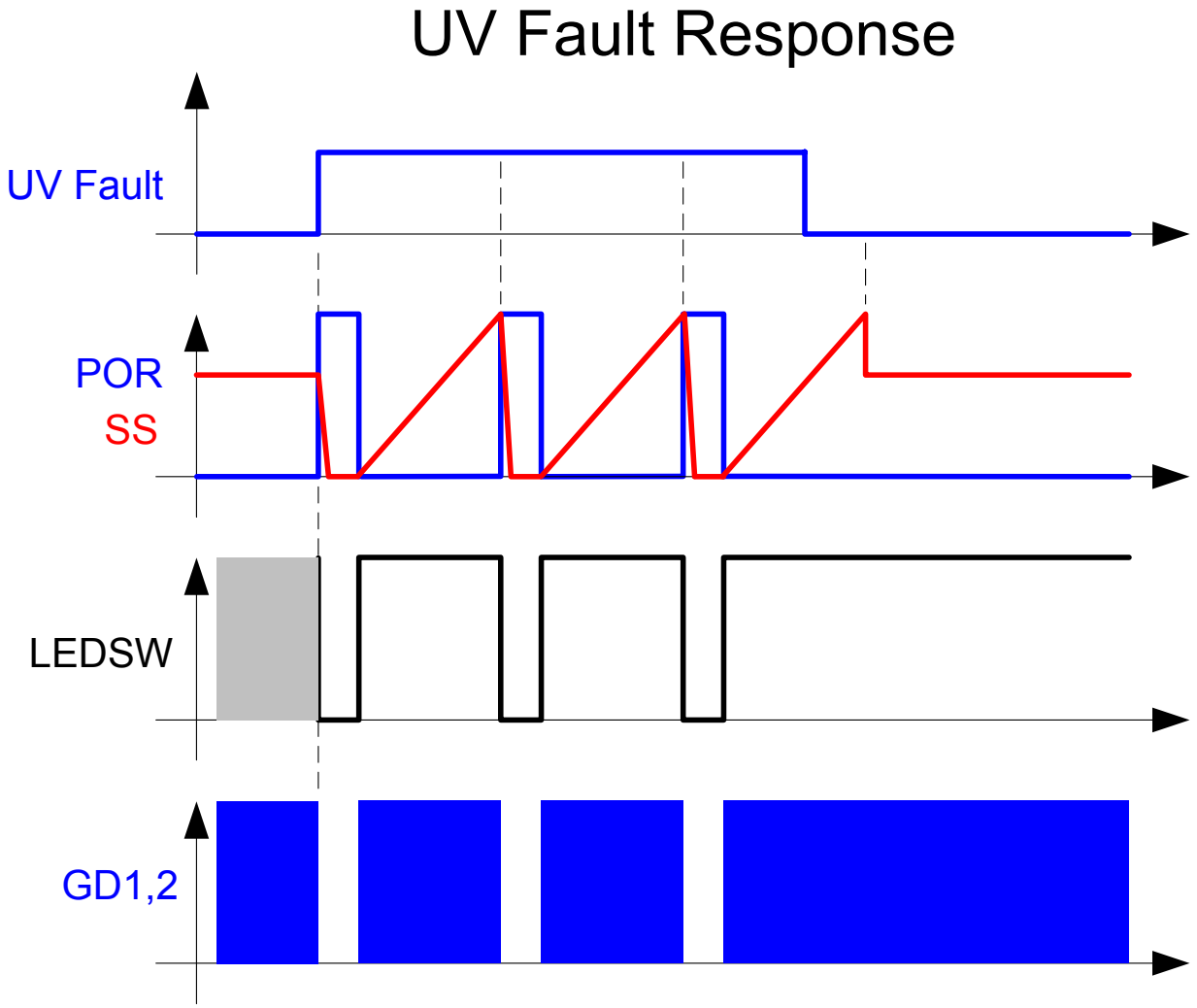
FAULT RESPONSE – OV, CL(1V) or TSD

- Fault stops LLC operation and turns off LEDSW
- SS capacitor is discharged
- Falling edge of Fault initiates RESET



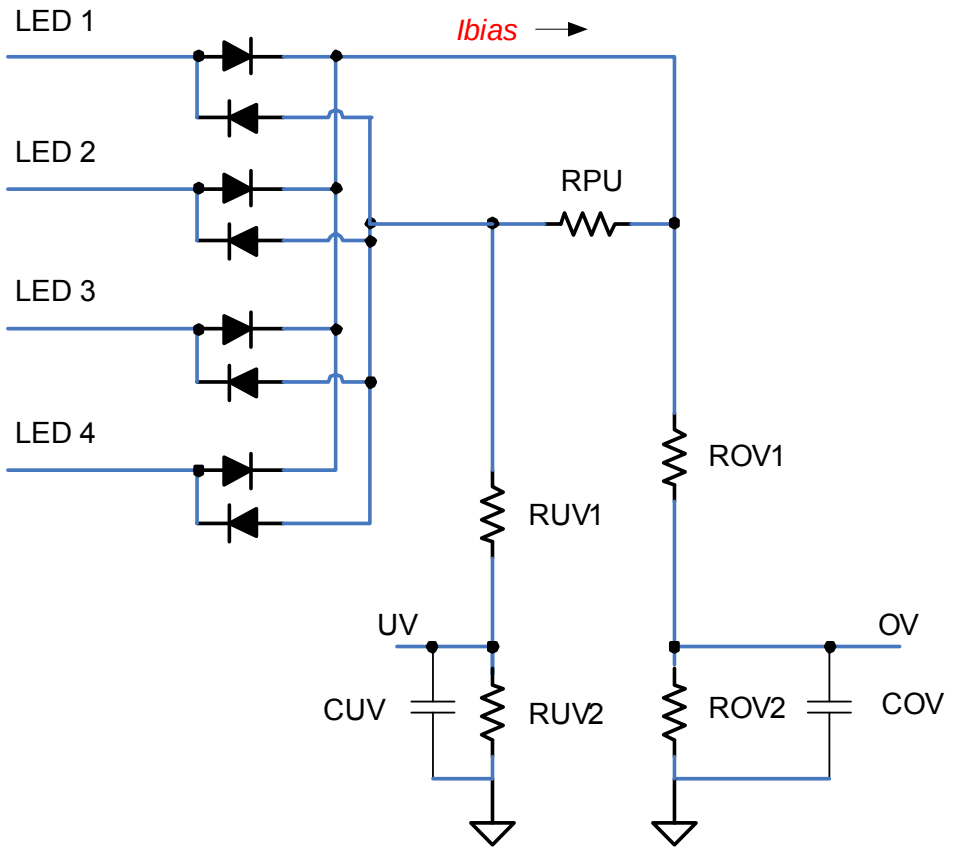
UV FAULT RESPONSE

- UV Fault initiates a POR-SS cycle
- A new POR-SS cycle is initiated if the UV Fault is still present at the end of SS
- If the UV Fault clears during a POR-SS cycle the supply will start normally



UV and OV Design Considerations

- OV and UV dividers with oring diodes shown. Positive LED votlage outputs.
- The highest voltage LED string provides the bias current for both OV and UV dividers.
- The bias current needs to be LOW so LED current matching does not degrade at low dimming.
- Example: 100mA ILED, 1% dimming, 2% LED matching spec: only 20uA delta allowed
- Another consideration: Voltage across RPU should be higher than LED string maximum delta V. A current path from VLED max to VLED min should be avoided



Other Fault Characteristics

- CL has a 1V threshold with 0.5V of hysteresis
- CL has an additional 1.9V threshold
  - When crossed the GD and LEDSW outputs are latched off
  - This is the only latching fault
  - Fault is only cleared by UVLO
- The UV and OV thresholds have ~8% of hysteresis
- Threshold tolerances of ~+/-5%

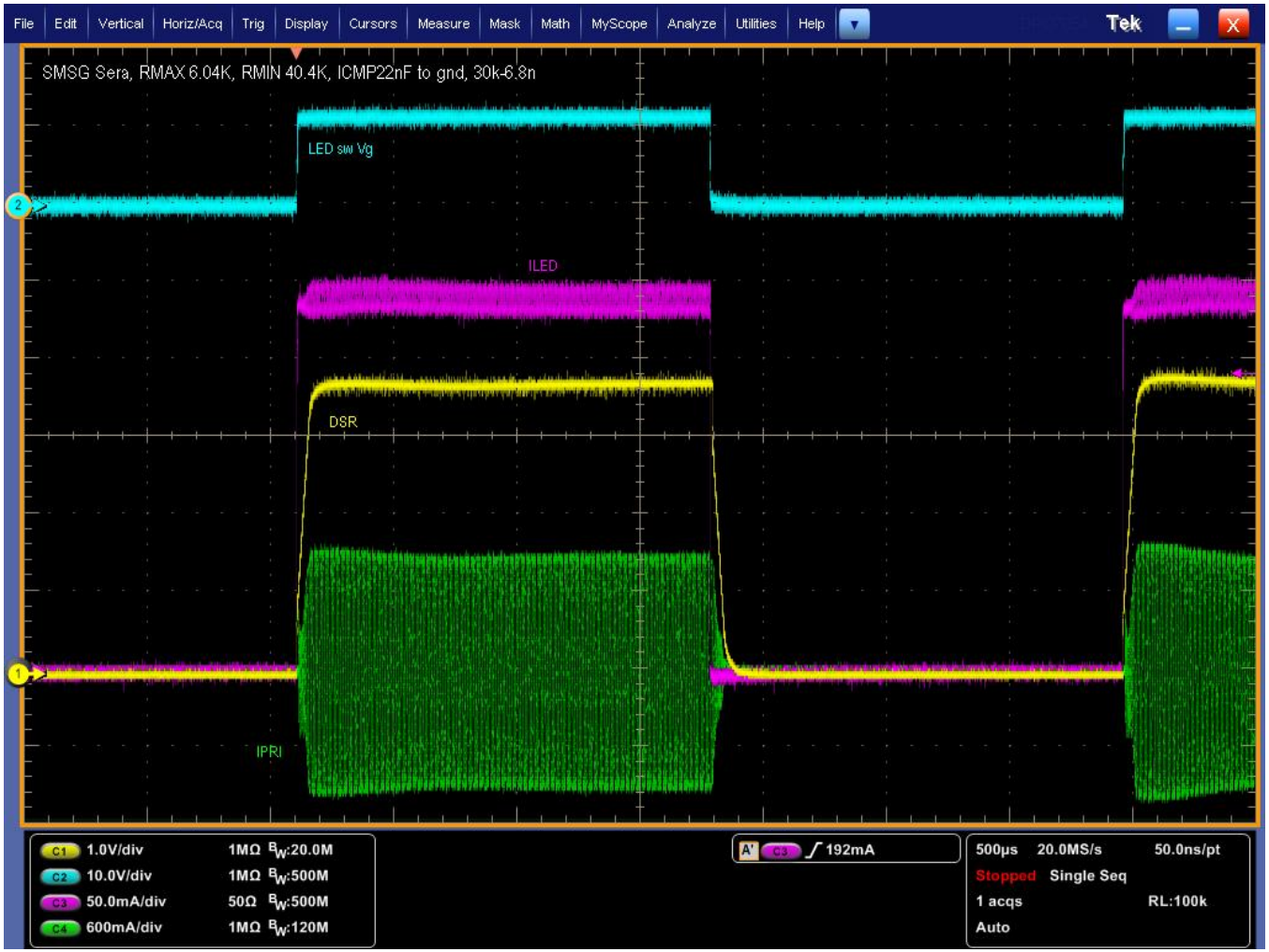
Test Data From LED Driver with UCC25710

- DIM input is disabled during Soft Start as shown below.
- DIM active during BLON enable.

- Soft Start
- LED FET Vgs
- ILED
- DSR
- Ipri

Test Data From LED Driver with UCC25710

- Almost perfect square wave LED current achievable with LED switch feature. No Ipri peaking achieved by limiting ICOMP bandwidth.



- 50% Dimming
- LED FET Vgs
- ILED

50mA/Div

- DSR

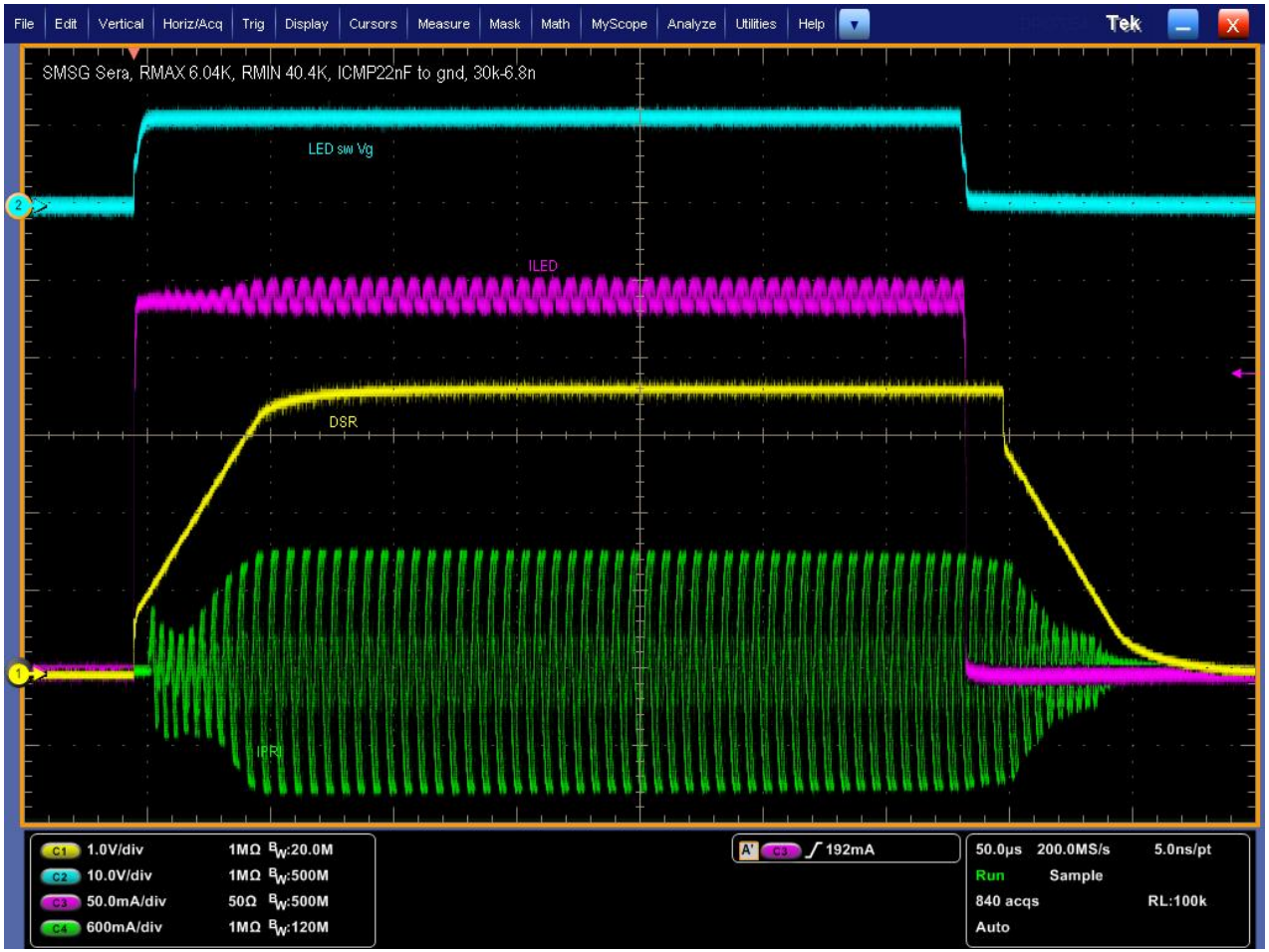
1V/Div

- Ipri

600mA/Div

Test Data From LED Driver with UCC25710

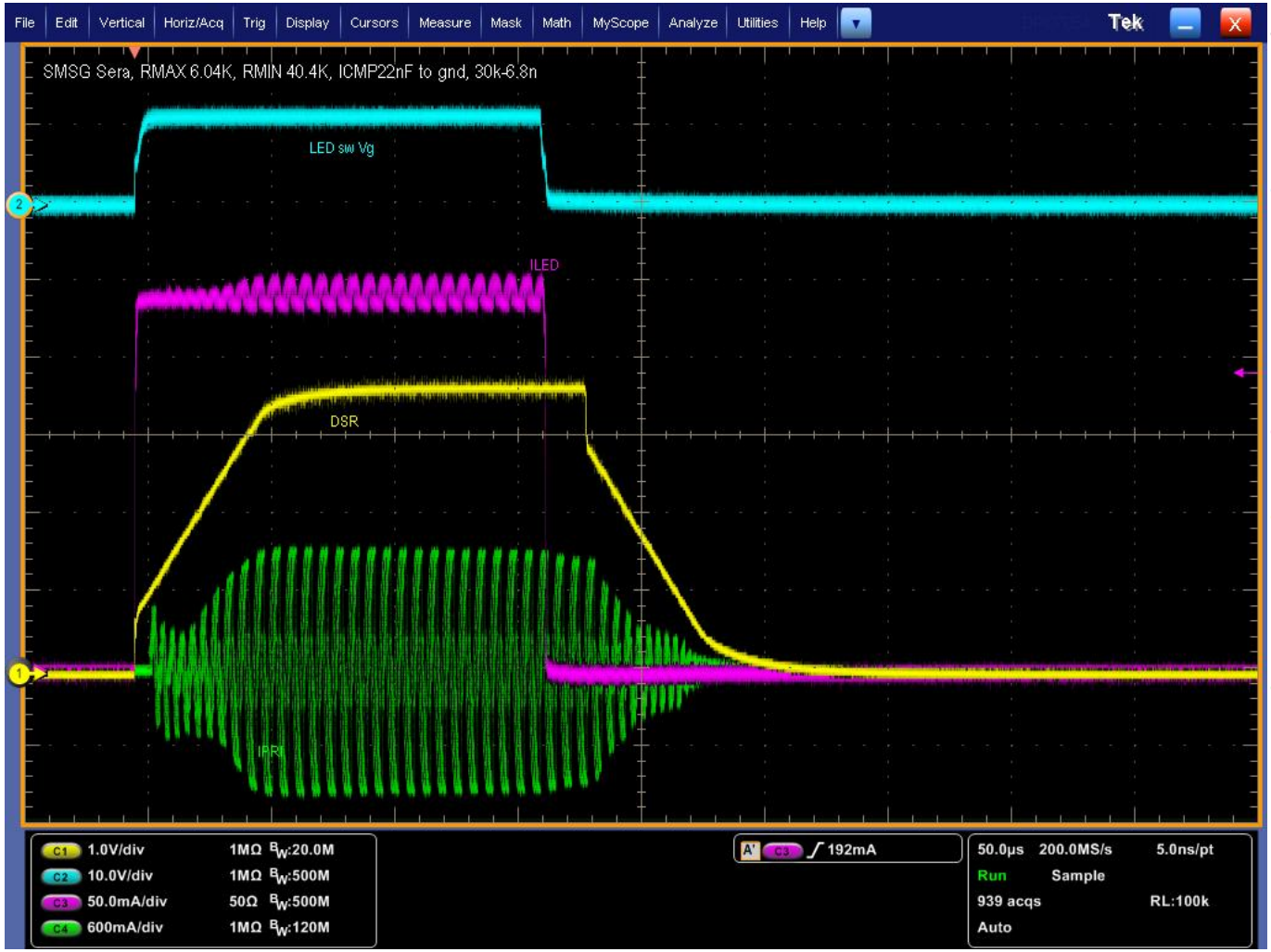
- Notice Step on DSR rising & falling edge: Adding 15k to 20K ohm resistor in series with DSR cap reduces delay time to start LLC power stage. Step on falling edge is not an issue since DSR is clamped ~0.7V above ICOMP



- 10% Dimming
- LED FET Vgs
- ILED
- DSR
- Ipri

Test Data From LED Driver with UCC25710

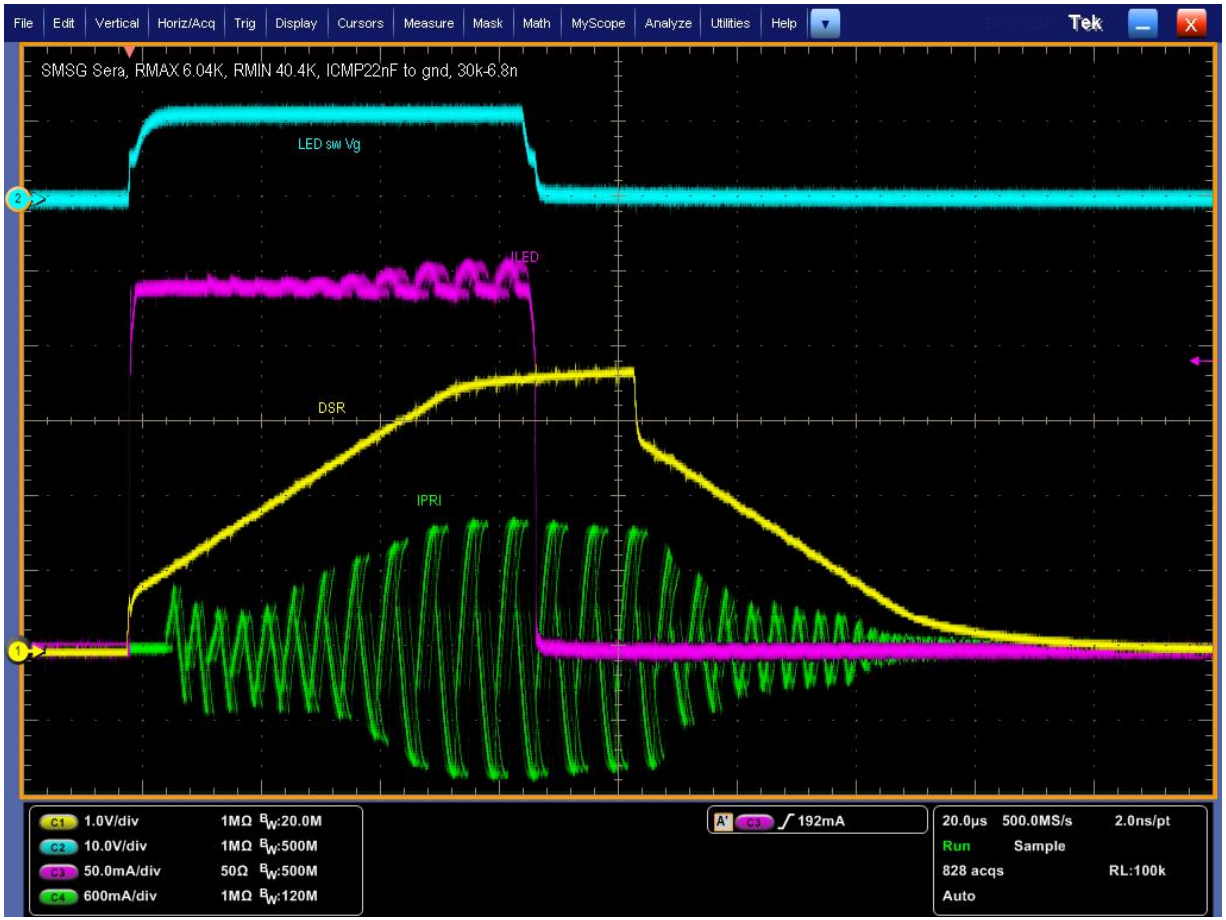
- Notice the falling edge of DSR time delay is increasing as DIM duty cycle reduces.



- 5% Dimming
- LED FET Vgs
- ILED
- DSR
- Ipri

Test Data From LED Driver with UCC25710

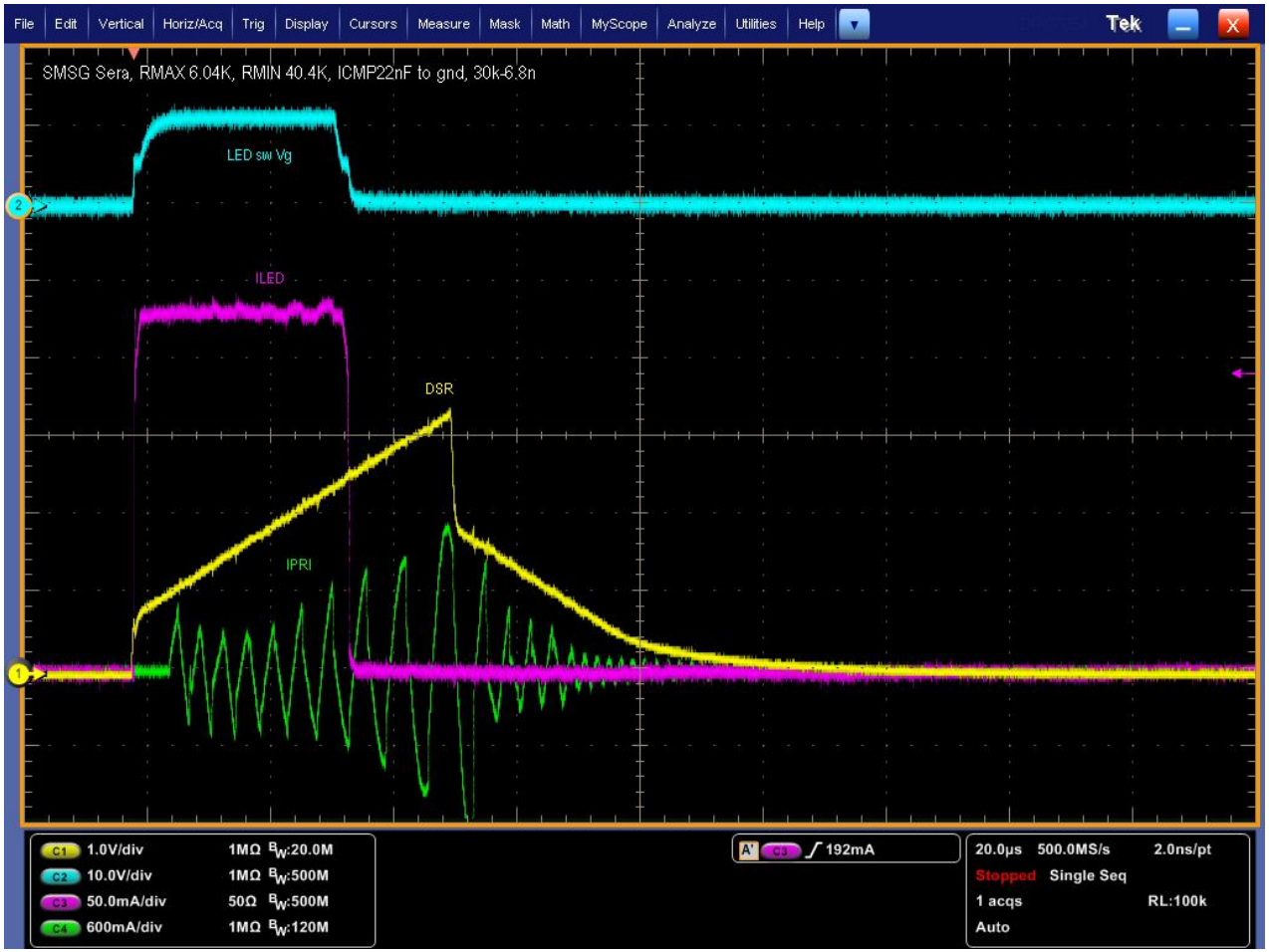
- At 2% dimming @300Hz, the DSR voltage indicates that the steady state operating point is still achieved. DSR rise & fall time is ~100us in this configuration.



- 2% Dimming
- LED FET Vgs
- ILED
- DSR
- Ipri

Test Data From LED Driver with UCC25710

- At 1% dimming @300Hz, the DSR voltage does not reach the steady state plateau.



- 1% Dimming
- LED FET Vgs
- ILED
- DSR
- Ipri

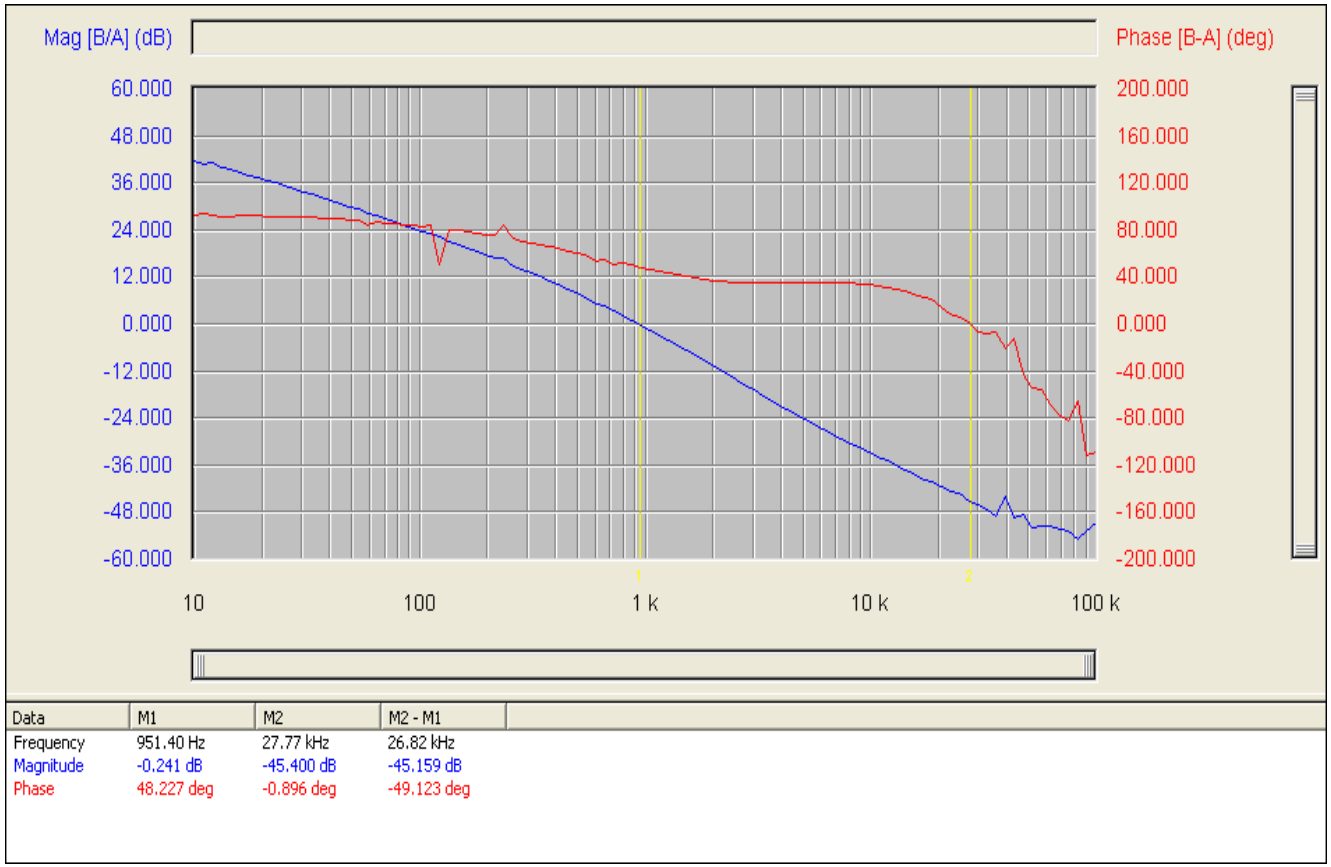
Test Data From LED Driver with UCC25710

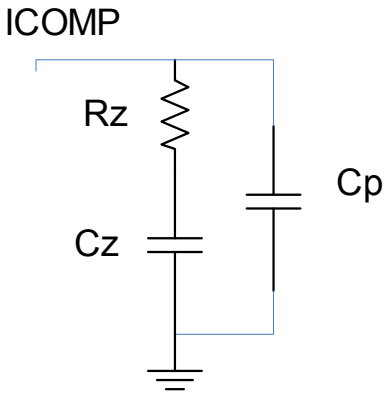
- DTY and DADJ shown to indicate method of DIM duty cycle compensation. When DADJ reaches DTY voltage, DSR fall time starts.

- 1% Dimming
- DADJ
- DTY
- ILED
- Ipri

Test Data From LED Driver with UCC25710

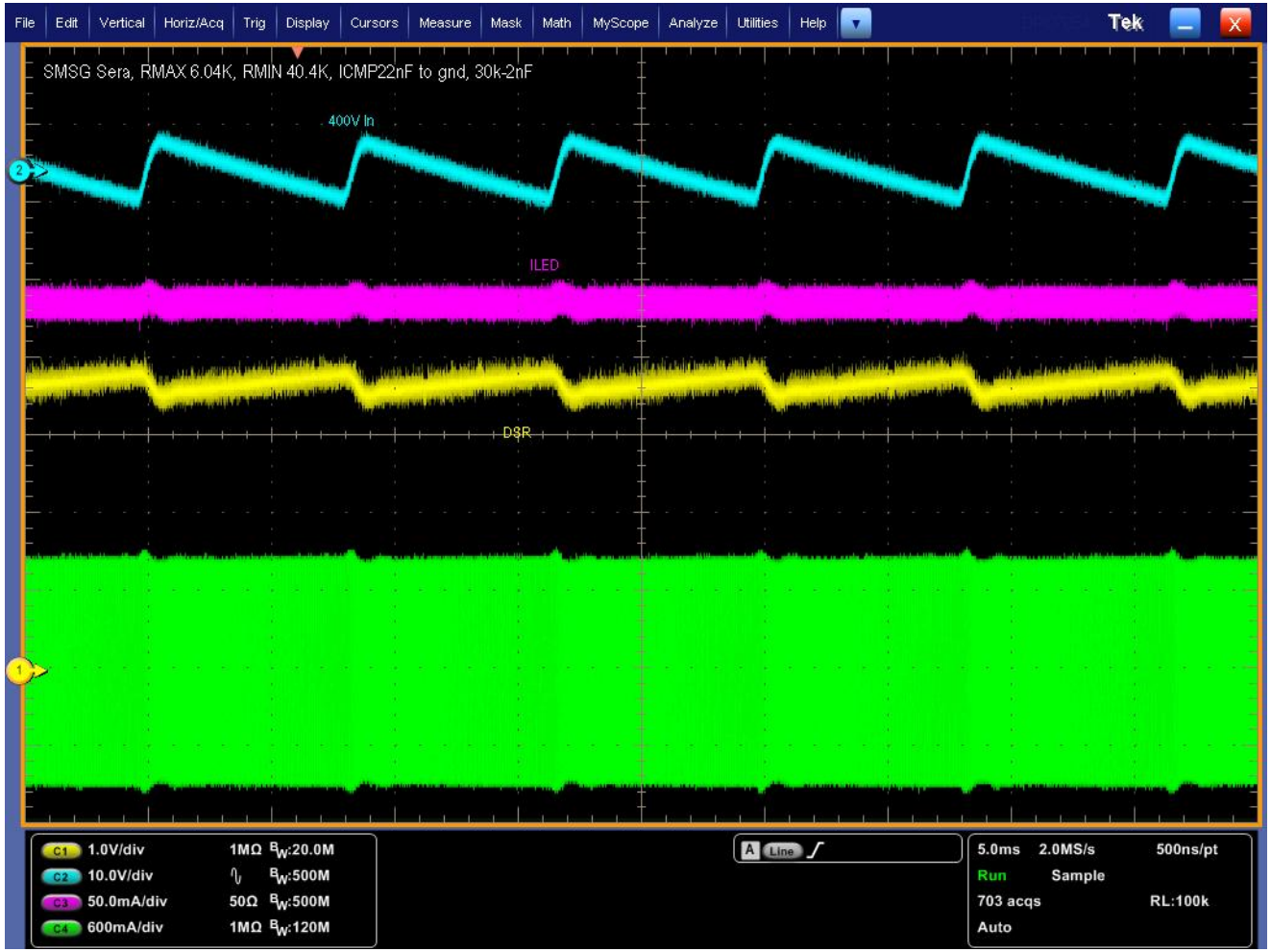
- Ipri peak current during dimming is minimized shown in the previous plots by selecting ICOMP compensation that has fairly low bandwidth.
- ICOMP values in this example: Cp:22nF, Cz:6.8nF, Rz: 30k Ohm





Test Data From LED Driver with UCC25710

- Low bandwidth in the LLC may create a line frequency rejection concern.
- Below Line frequency component is shown with 10Vp-p 240Hz ripple on 400V input. LED ripple is low even with 10uf output caps and 240mA ILED.



400V Vin

~10V/Div

- ILED

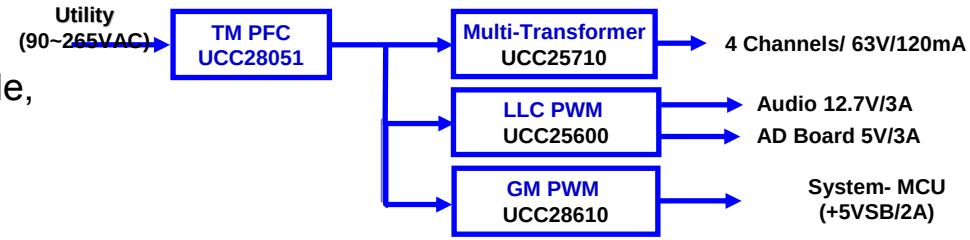
50mA/Div

- DSR
- Ipri

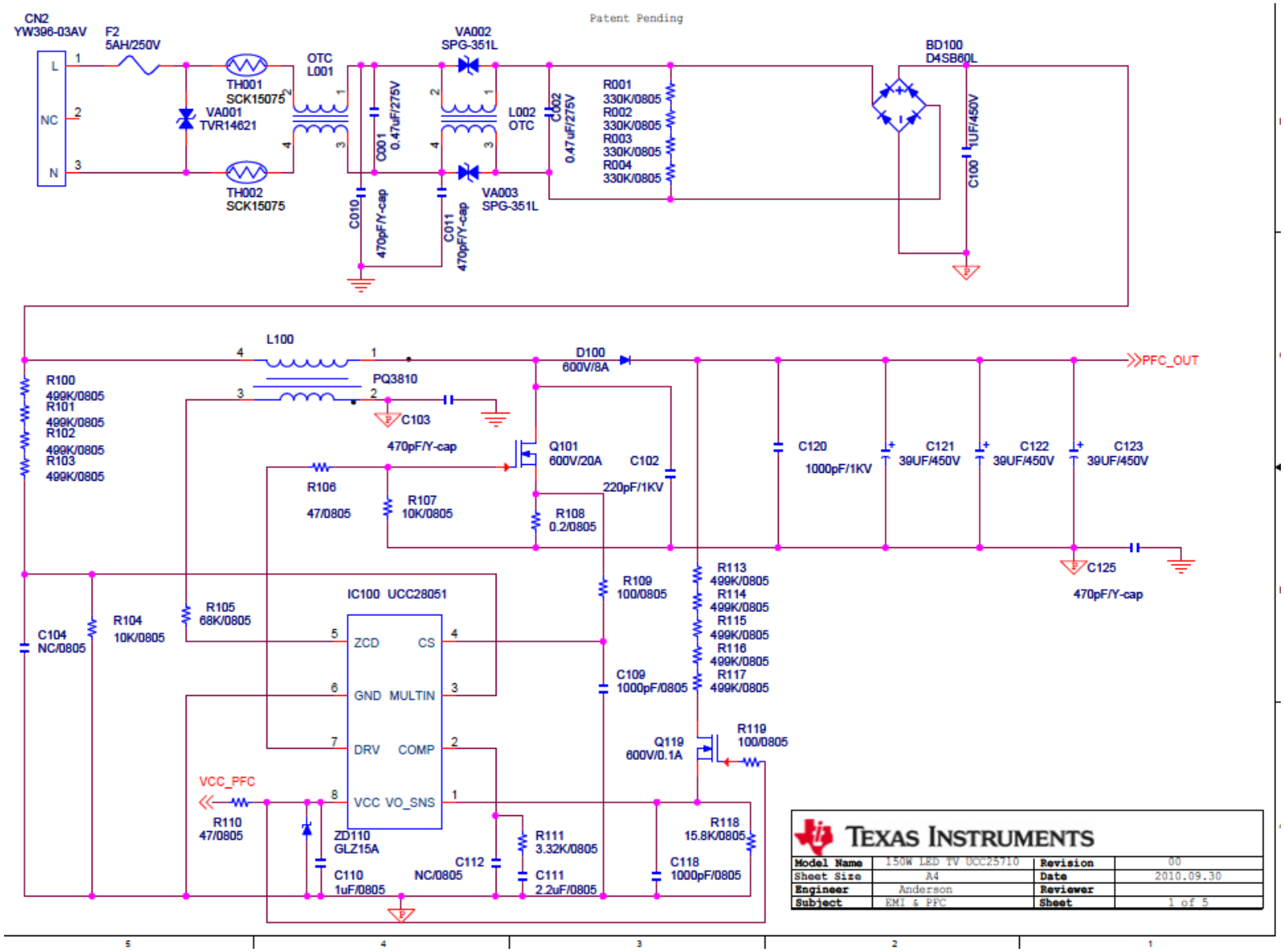
PMP6251 LED Backlighting for Edge-Lite/ Group Dimming Digital TV Application

Reference design Features

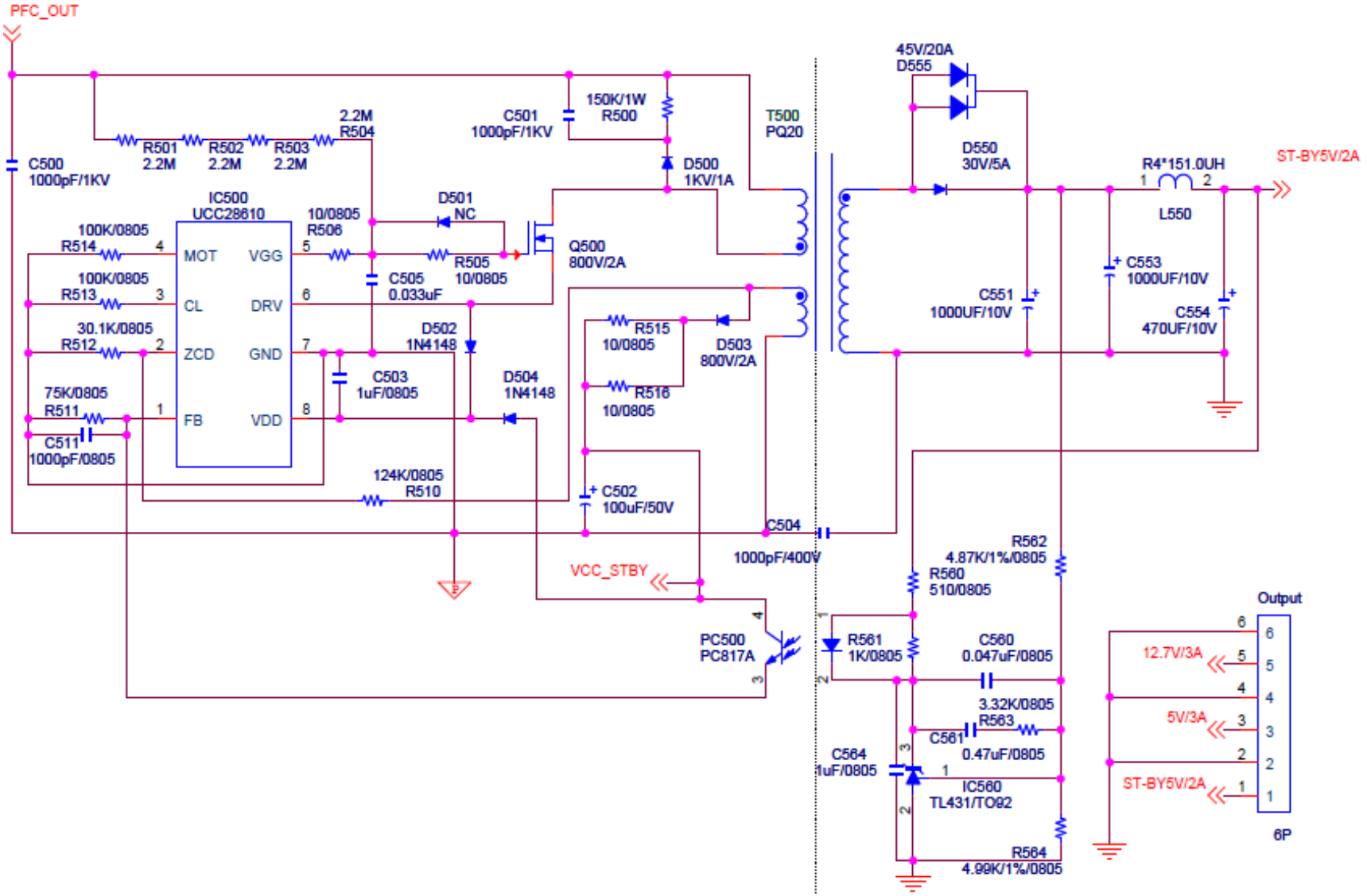
- Support to universal 90~264Vac range
- LED 4 outputs @120mA, 63V, 5Vsb@1A, 5V@3A, 13V@3A
- Eff 83.7%@110Vac, 85.2%@240Vac
- Secondary side 120Hz blanking control for dimming
- 8mm height and 6mmheight for LED magnetic component
- Board dimension 300mm(L) * 200mm(W) * 8mm(H)
- LED output common + and LED OVP and UVP
- Integrated the protection ckt to reduce the solution part count.
- Dedicated controller for edge-lit/ group dimming base on the LLC topology – **UCC25710.**
- Providing design package – Schematic, Gerbo file, PCB file, Magnetic components…



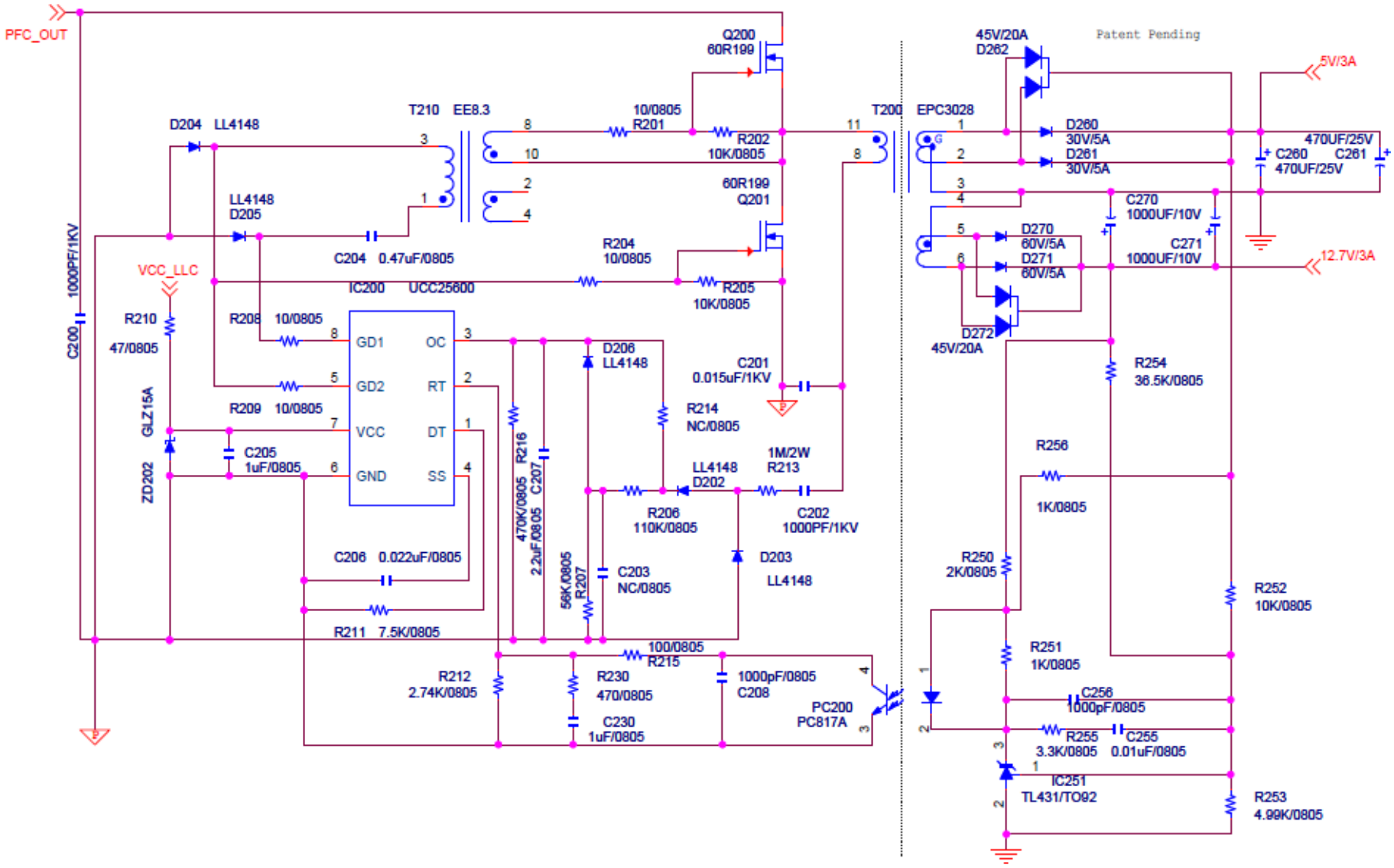
Schematic PFC



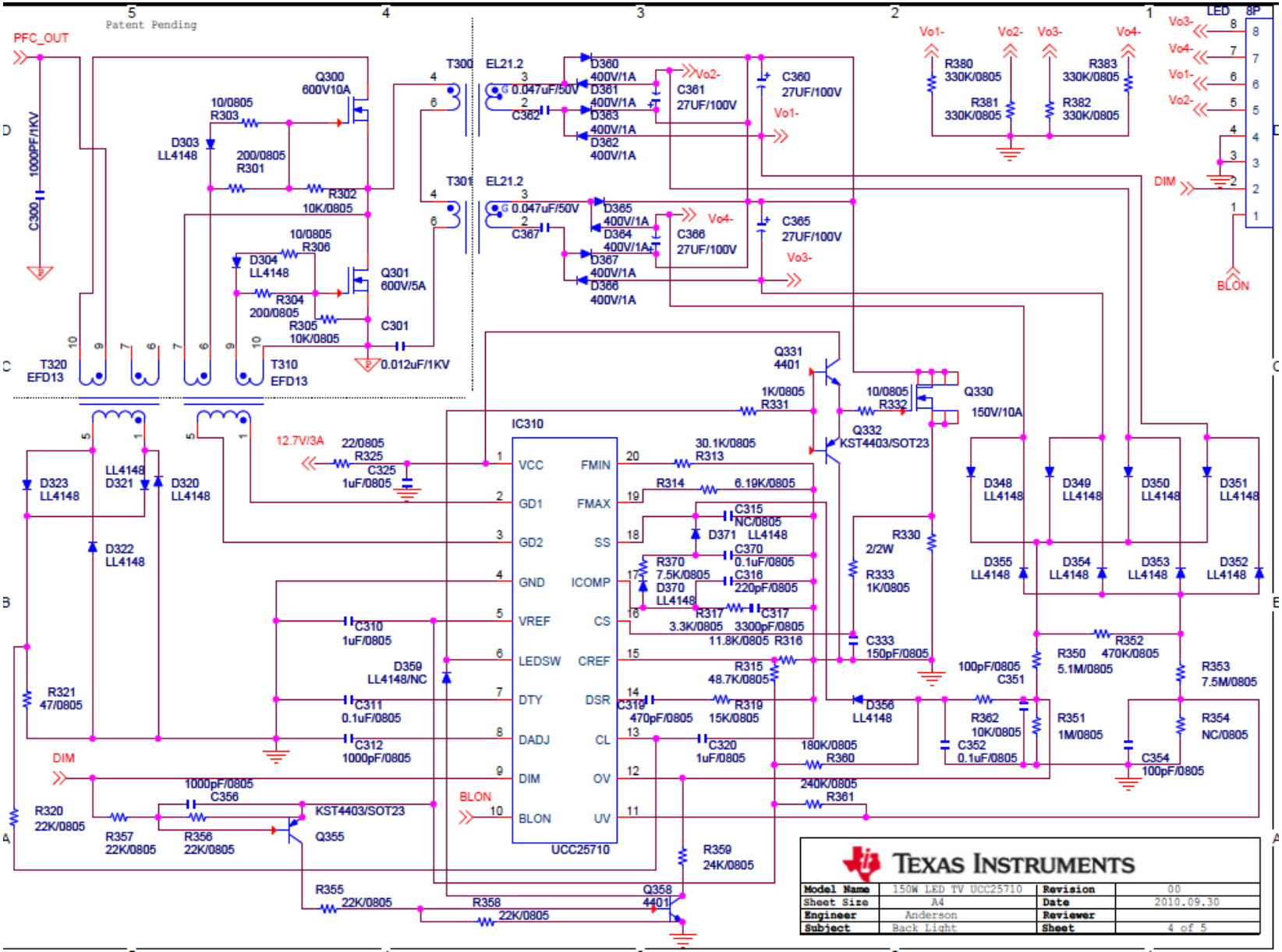
Schematic Standby



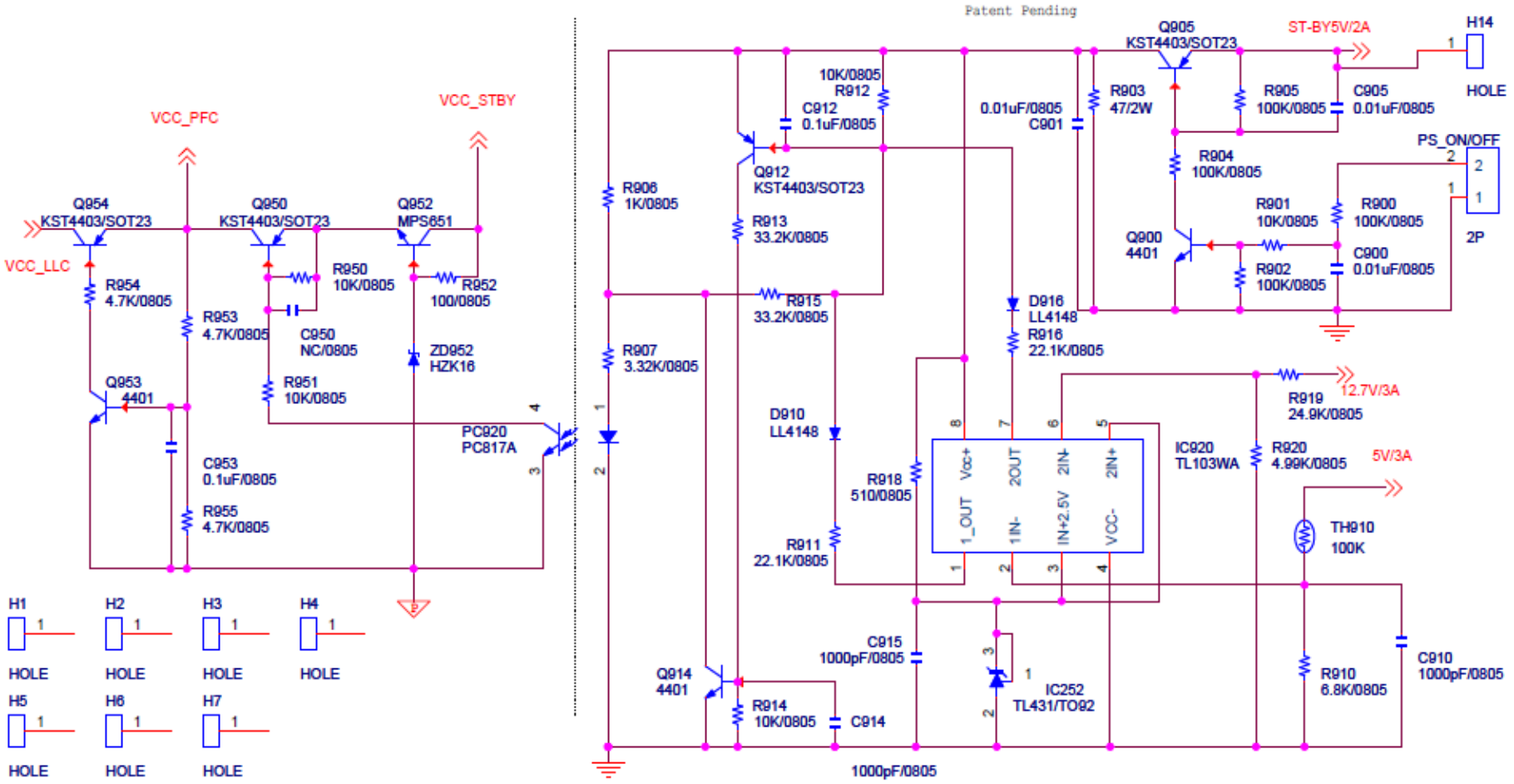
Schematic 5V/12V



Schematic LED Driver



Schematic Protection



Cross Regulation

Cross Regulation			
Load Condition		Output Voltage	
5V	13V	5V	13V
4mA	0A	5.13V	13.08V
4mA	3A	5.18V	12.55V
3A	0A	5.04V	13.82V
3A	3A	5.09V	13.4V

LED Current

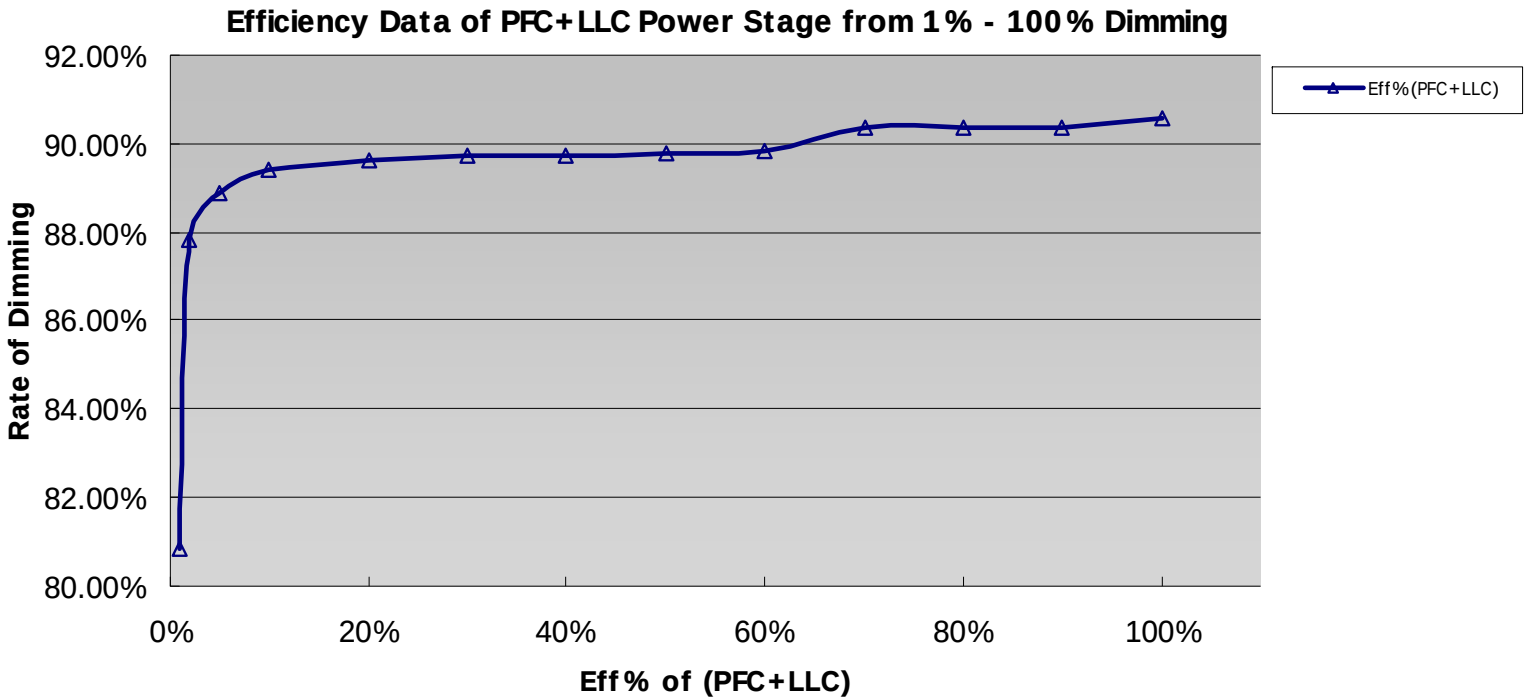
	LED1	LED2	LED3	LED4	AVG
100.00%	120.2	120.4	122.95	123.11	121.665
90.00%	108.2	108.32	110.77	110.8	109.5225
80.00%	96.18	96.26	98.49	98.52	97.3625
70.00%	84.16	84.24	86.19	86.19	85.195
60.00%	72.13	72.22	73.9	73.9	73.0375
50.00%	60.13	62.2	60.13	61.6	61.015
40.00%	48.12	48.16	49.26	49.28	48.705
30.00%	36.1	36.13	36.95	36.98	36.54
20.00%	24.07	24.09	24.63	24.66	24.3625
10.00%	12.04	12.05	12.32	12.34	12.1875
5.00%	6.02	6.02	6.15	6.18	6.0925
2.00%	2.4	2.41	2.46	2.47	2.435
1.00%	1.2	1.2	1.23	1.24	1.2175

LED Current Tolerance

	Tolerance1	Tolerance2	Tolerance3	Tolerance4
100.00%	-1.204126084	-1.03974027	1.05617885	1.1876875
90.00%	-1.207514438	-1.09794791	1.13903536	1.16642699
80.00%	-1.214533316	-1.13236616	1.15804339	1.18885608
70.00%	-1.214860027	-1.1209578	1.16790891	1.16790891
60.00%	-1.242512408	-1.11928804	1.18090022	1.18090022
50.00%	-1.450463001	1.942145374	-1.450463	0.95878063
40.00%	-1.201108716	-1.11898162	1.1395134	1.18057694
30.00%	-1.204159825	-1.12205802	1.12205802	1.20415982
20.00%	-1.2006157	-1.11852232	1.09799897	1.22113905
10.00%	-1.21025641	-1.12820513	1.08717949	1.25128205
5.00%	-1.18998769	-1.18998769	0.94378334	1.43619204
2.00%	-1.437371663	-1.02669405	1.02669405	1.43737166
1.00%	-1.437371663	-1.43737166	1.02669405	1.84804928

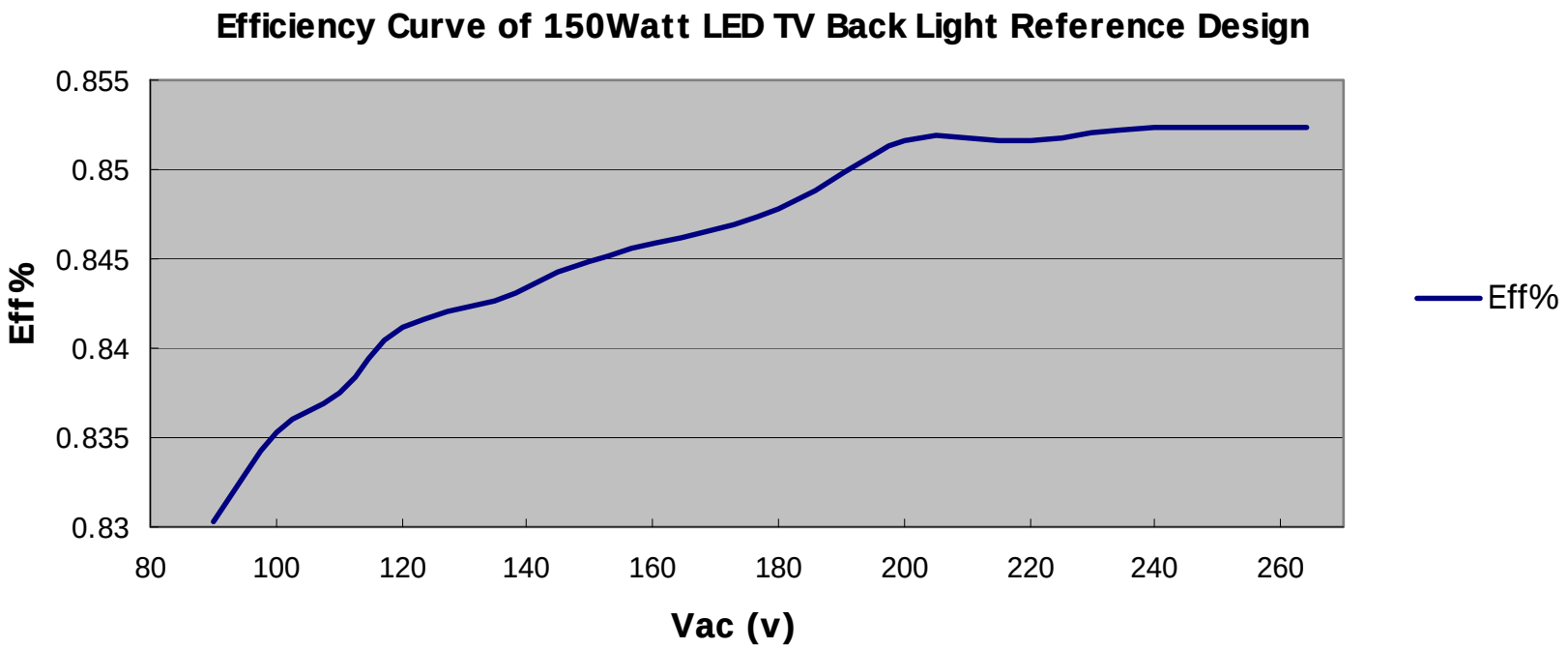
Inductance tolerance 3% might cause current tolerance 1%

LLC Efficiency



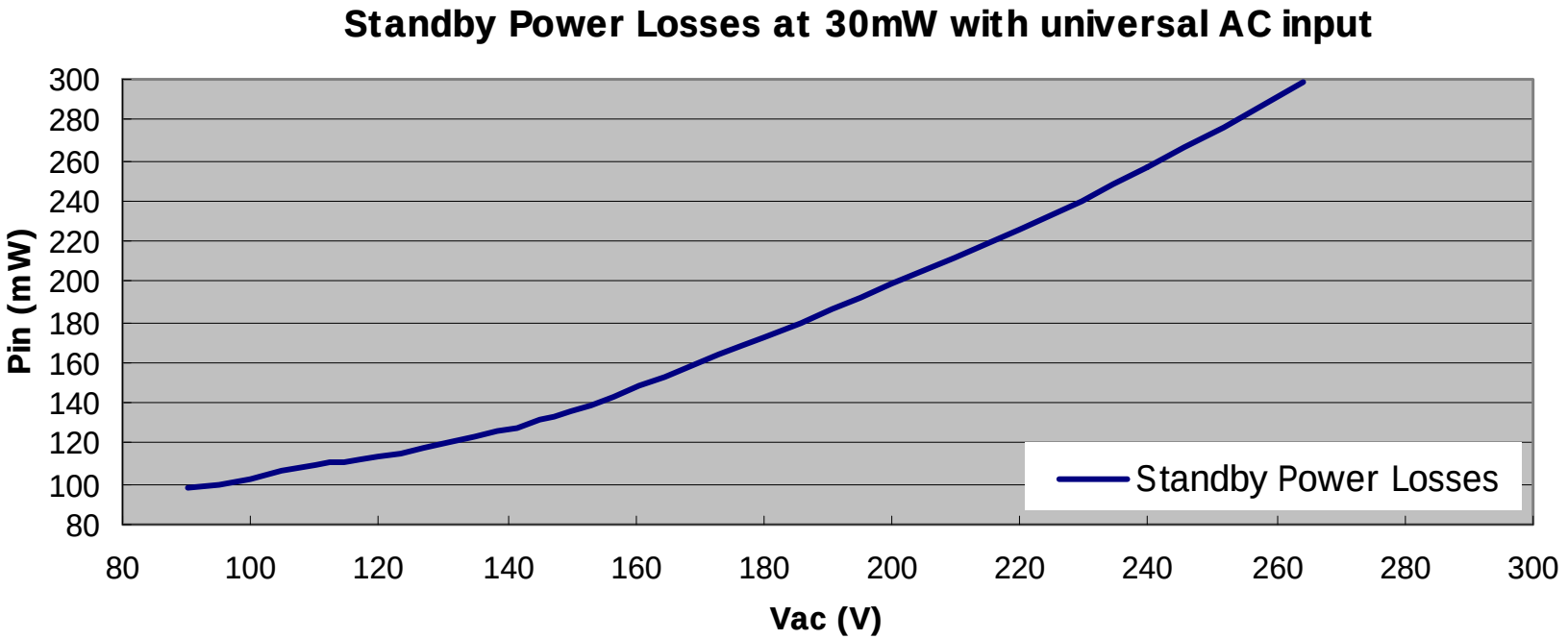
Efficiency exclude Stby Power Converter at full load condition ~ 90%

Efficiency



Vin	90	100	110	120	135	150	180	200	220	240	264
Pin	115.6	114.9	114.6	114.1	113.9	113.6	113.2	112.7	112.7	112.6	112.6
Eff	0.83023	0.83529	0.83748	0.84115	0.84262	0.84485	0.84783	0.85159	0.85159	0.85235	0.85235

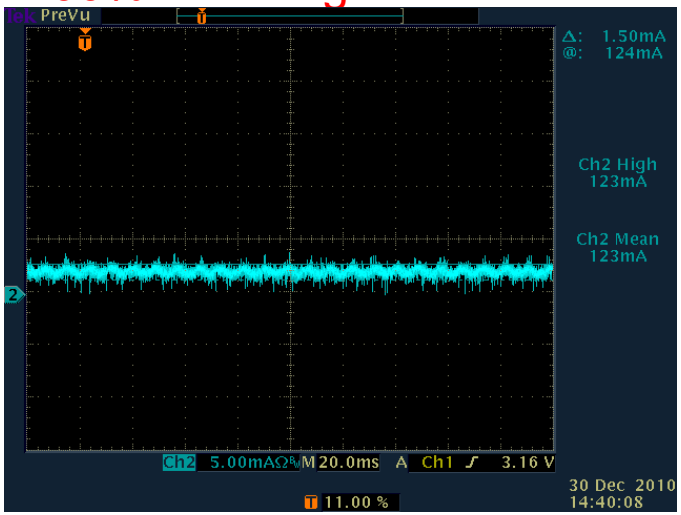
Standby Mode Power Consumption Performance – @5V/ 30mW



Vin	90	100	110	120	135	150	180	200	220	240	264
Pin	98.3	103	109	114	124	136	173	199	226	256	298

Dimming Waveforms

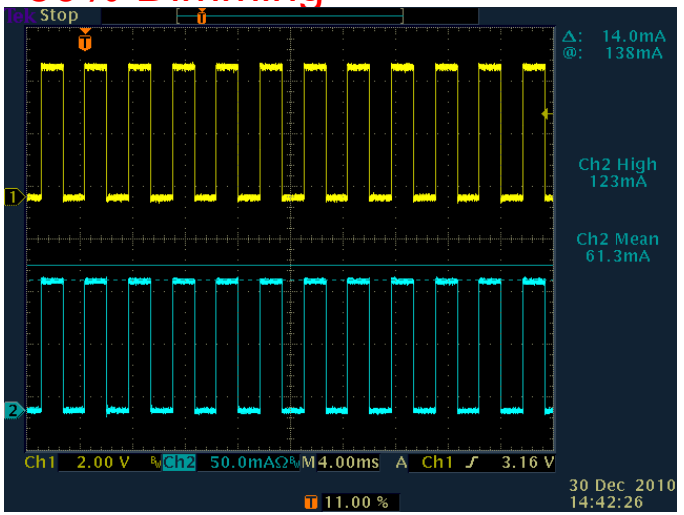
100% Dimming



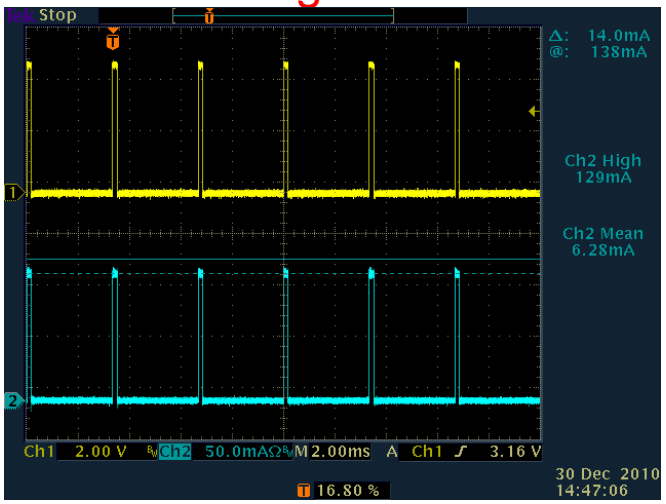
Current

DIM

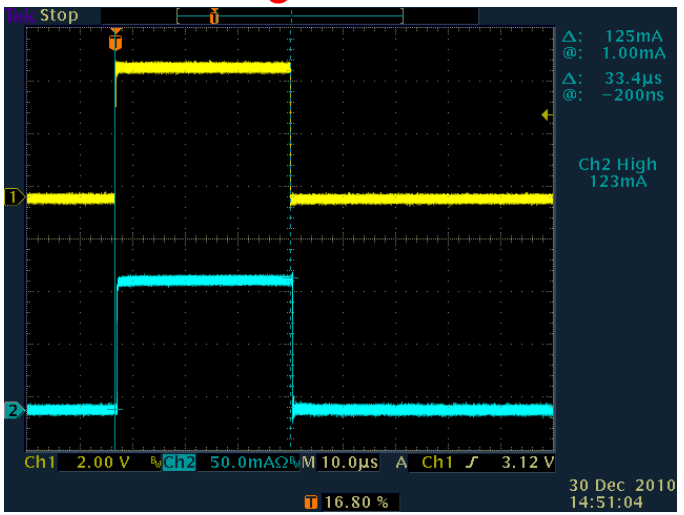
50% Dimming



10% Dimming



1% Dimming



Introducing

- UCC28051
- UCC28610
- UCC25600
- UCC24610

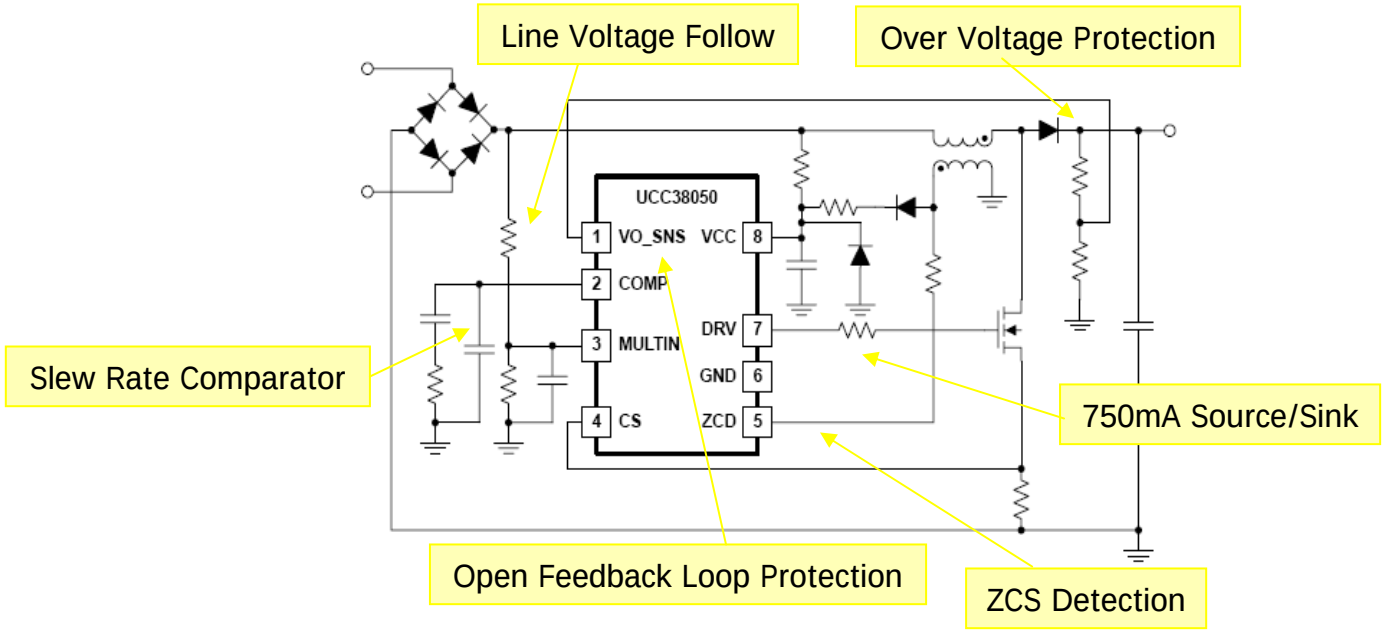
UCC28051 Transition Mode PFC Controller

Features

- Slew Rate Comparator for Improved Transient Response
- Zero Power Detect to Prevent Over Voltage Conditions under Light Load
- Over Voltage Protection
- Open Feedback Protection and Enable Circuits
- Low Startup & Operating Current
- 750mA Source/ Sink Peak Gate Drive to Reduce Switching Losses

Applications

- LCD-TV Power Board
- AC-DC Open Frame Power
- Mid to High Power AC Adapters



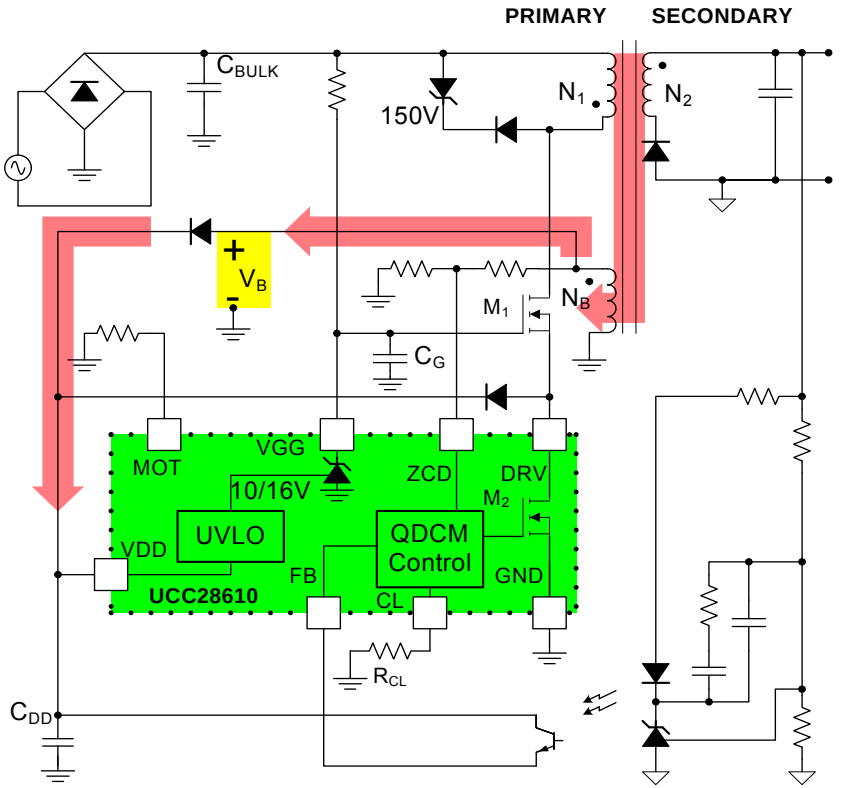
UCC28610 QR-GM Cascoded Flyback PWM

Features

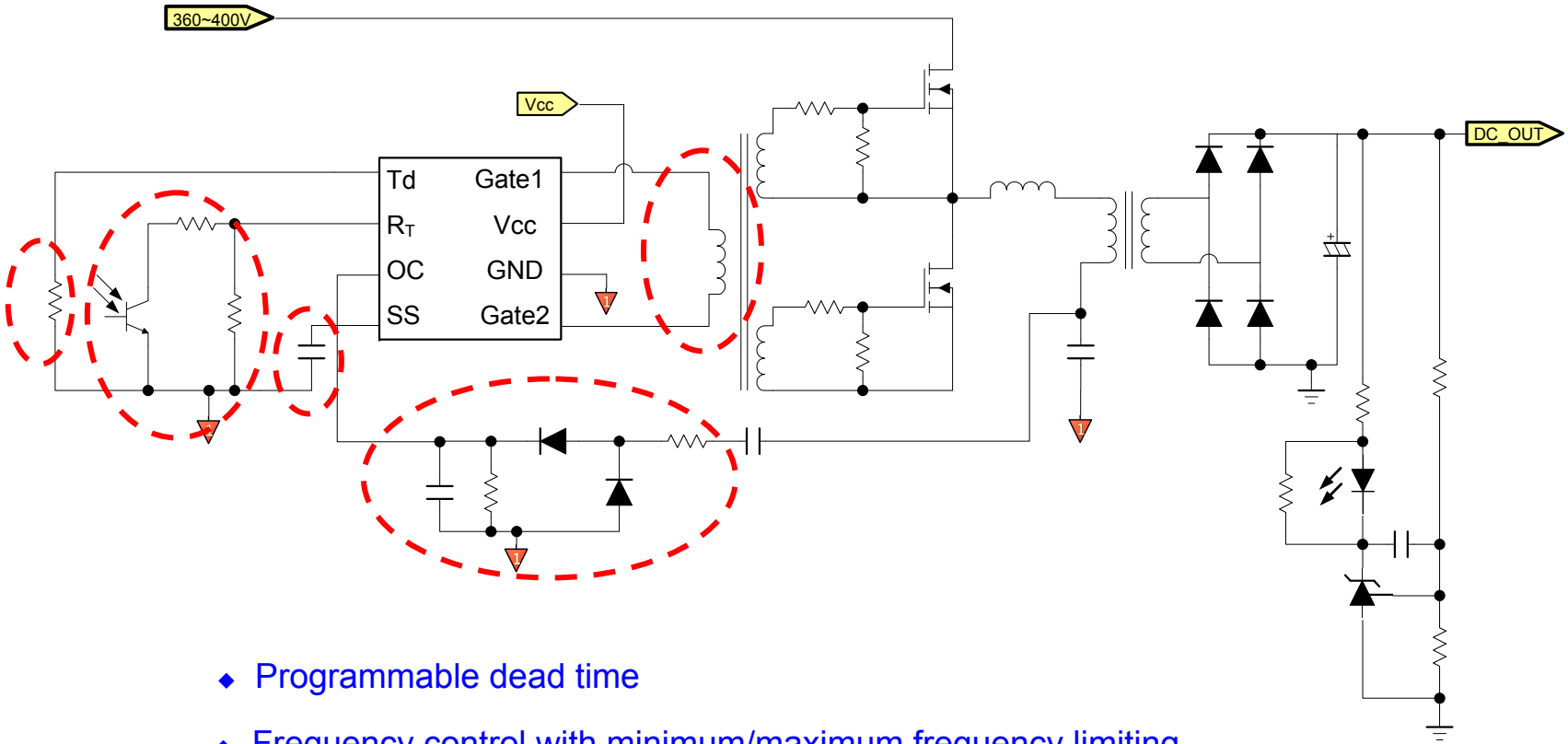
- Quasi-Resonant Green Mode PWM Operation
- Multiple Modes: Pulse Position Modulation (PPM); Discontinuous Conduction Mode (DCM); Burst Operation
- Surge Protection is Externally Set
- Valley Switching is always Engaged – Limits Primary and Secondary RMS Currents
- Fast Latched Fault Recovery for Output OVP, Timed OCP, Over Temperature Protection
- External Shutdown & Latched Shutdown at MOT Pin
- Current Sensing for Current Limit uses Rds(on) of Internal FET

Applications



UCC25600 Resonant (LLC) Application Circuit



- Programmable dead time
- Frequency control with minimum/maximum frequency limiting
- Programmable soft start with on/off control
- Two level over current protection, auto-recovery and latch up
- Matching Gate output with 50ns tolerance

Question?

Thanks for Your Time !

Back up

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265