AN5420

Evaluation Board

Features

- Eight 13-bit DACs on the SPT5420
- Wide output voltage swing; V_{DD} - 2.5V to V_{SS} +2.5V on each DAC
- On-board address, load and write circuits
- BNC connectors on the DAC outputs
- Two clock input connections
- On-board manual chip select and clear
- On-board reference circuit
- Automatic or manual control of DAC registers
- Prototype area for analog and digital circuitry

Applications

- Evaluation of the SPT5420 DAC
- Eight analog controls as subsystem
- 13-bit precision control system
- Engineering prototype aid
- Guide to PCB layout
- Guide for design of SPT5420

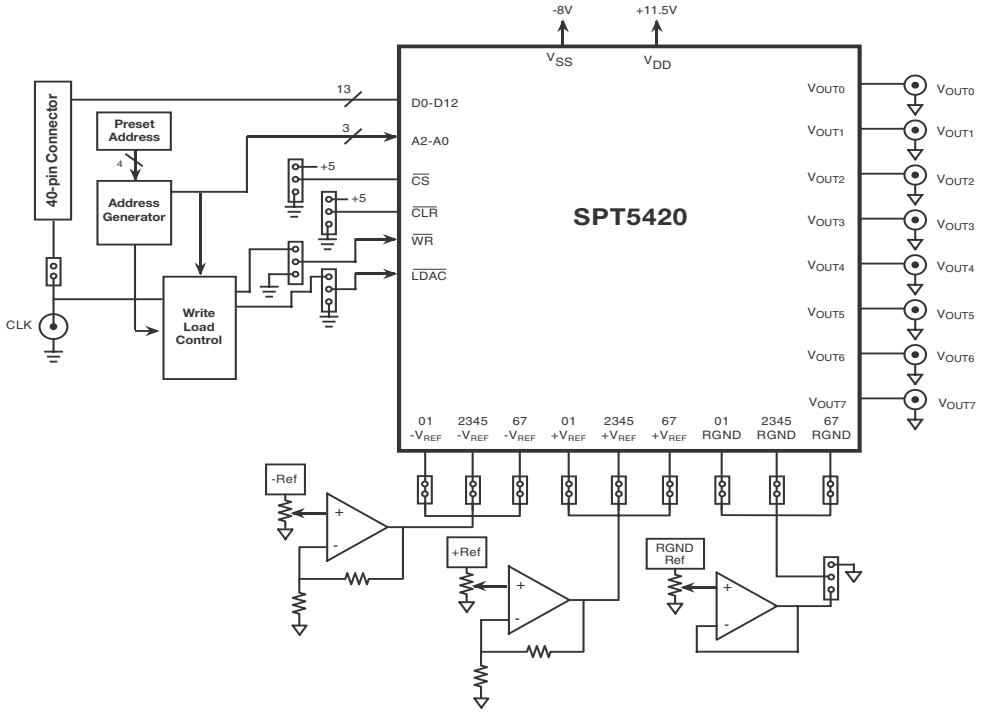
Description

The SPT5420 is a 13-bit octal DAC capable of outputting bipolar values from V_{DD} - 2.5V to V_{SS} +2.5V with a supply voltage of ±15V. There are two separate reference input pins V_{REFT} and V_{REFC} for each DAC pair. (DAC pairs are delineated as 01, 23, 45 and 67 respectively.) As many as four separate reference inputs are available for all eight DACs. It is possible to produce four different full-scale output voltages with a resolution of 13 bits (full scale/8192) from the four DAC pairs.

The SPT5420 is capable of bipolar, unipolar (positive or negative) or custom output voltages. The voltage output of each DAC is a single-ended source. The SPT5420 provides for a double latch of the data or may be set to transparent mode for each DAC. An asynchronous clear (/CLR) pin clears the data value in the DAC to a voltage set by the value of RGND.

This device is ESD sensitive. All ESD precautions should be exercised when handling this device.

Block Diagram



The EB5420 evaluation board is a tool for device evaluation and characterization and demonstrates the performance of the SPT5420 (13-bit, octal DAC). The SPT5420 accepts up to 13 binary bits into its logic inputs. The clock signal source may be provided from one of two input sources, the logic connector or a BNC connector.

Various termination schemes are provided, depending on the type of clock signal used. The data is presented to the SPT5420, then, depending on the control lines of the address (load and write), the data is transferred to the selected DAC. The output voltage is a function of the reference voltages (see the Reference section) at the V_{REFT} and V_{REFC} pins for the selected DAC.

This application note is a supplement to the data sheet and includes more detailed technical information on the interfacing circuits required to operate the SPT5420. The evaluation board is designed to accommodate a wide variety of applications and can be easily modified to suit a specific application with the use of the prototype area provided. Contact the Fairchild Applications Engineering Department if assistance is needed.

This application note describes in more detail the functional blocks of the evaluation board. The topics include Power Supplies and Grounding, Logic Interface Circuit, Conversion Clock, Analog Output, Reference Circuits and Layout.

POWER SUPPLIES AND GROUNDING

The EB5420 is powered by +11.5V and -8V supplies. The +D5V supplies the digital control circuitry ('161 counter and '139 dual two-four decoder). The +11.5 V is the supply for the analog section (+11.5V, V_{DD} of the DAC and +11.5V for the reference source and reference op amp). The -8V supply is used for the DAC's V_{SS} and the op amp's negative supply. Adequate isolation filtering and decoupling of the power between the analog and digital circuits have been incorporated into the design; however, Fairchild recommends that you use low-noise (nonswitching), regulated and low source impedance supplies. Refer to table I for power and signal connections.

Power is brought onto the evaluation board via the banana post. Power distribution to the analog +11.5V of the SPT5420 is filtered to isolate it from the digital switching noise associated with the TTL signals. Fairchild recommends that you use a similar design approach when using a single analog supply.

The power return connections and grounding are accomplished with a split ground plane: one for the digital return and one for the analog return. The two ground planes are coupled together through ferrite beads (FB1, 2) near the DAC. This reduces the high-speed digital switching signal noise from disturbing the low-noise analog section.

Power up should be done in the following sequence: V_{SS}, V_{DD}, references and, finally, the logic inputs. The power supply voltages should be at their nominal operating levels before applying digital logic signals to this device. If this sequence is not possible, limit the input voltage level at the logic input pins to no more than +0.3 V above V_{DD} during power up. Ensure that the absolute maximum voltage ratings are not exceeded at power up.

Table I - J1, Pinouts

Pin #	Description	Pin #	Description
1	Clock	2	Digital Ground
3	D0 (l LSB)	4	Digital Ground
5	D1	6	Digital Ground
7	D2	8	Digital Ground
9	D3	10	Digital Ground
11	D4	12	Digital Ground
13	D5	14	Digital Ground
15	D6	16	Digital Ground
17	D7	18	Digital Ground
19	D8	20	Digital Ground
21	D9	22	Digital Ground
23	D10	24	Digital Ground
25	D11	26	Digital Ground
27	D12	28	Digital Ground
29	NC	30	Digital Ground
31	NC	32	Digital Ground
33	NC	34	Digital Ground
35	/CLR	36	Digital Ground
37	/CS	38	Digital Ground
39	/WR	40	Digital Ground
41	A0	42	Digital Ground
43	A1	44	Digital Ground
45	A2	46	Digital Ground
47	/LDAC	48	Digital Ground
49	+D5	50	Digital Ground

DATA INPUT

Negative transients at the data inputs or control pins should not be allowed. Note that there are 4.7 kΩ resistors in parallel with the data inputs. These reduce the transients for the data input. Ensure that the SPT5420 is powered up before any logic input is applied.

You can achieve simultaneous output voltage change by performing a write to each address and then simultanoeously providing a common load strobe to /LDAC.

Asserting the clear pin (/CLR) will load the value of RGND into the latches in the DAC. There are four different RGND inputs partitioned for four output pairs. Refer to the block diagram in the technical data sheet. Deasserting the chip select pin (/CS, high logic level) will force the outputs to stay at their last program level, provided that the /CLR signal has not been asserted.

CONTROL CIRCUITS

The SPT5420 DAC can be controlled by a combination of jumpers, digital control logic and analog reference voltages. The board can operate in many different modes and is easily modified to meet your DAC control needs. The value of the analog full-scale output voltage is a function of the set reference voltages. Refer to the Reference Voltage section in the technical datasheet for details on the output setting.

The following table outlines the control of jumpers, connectors, potentiometers and switches. Refer to the reference diagram to determine the location of each described name.

Table II - Control Table

NAME	DESCRIPTION
J10 (CLK)	When jumpered, the clock source originates from the J1 connector. The clock requires a TTL-level signal.
BNC (CLK)	This is typically driven by a 50 Ω source. Ensure that J10 is unjumpered. The clock requires a TTL-level signal.
J9 (CLK)	Select position A for CLK through BNC connector. Position B to disable CLK.
Address Select	The switch setting selects the address of the DAC when the J8 is jumpered to A.
J2 (/LDAC)	J8 can be jumped to allow /LDAC to directly address the SPT5420 through J1. Ground to make each output latch transparent or used within the digital circuitry to latch outputs independently.
J3, J4, J5 (A0, A1, A2)	Individual DAC outputs can be selected between the connector J1 directly, address switch, or incremented automatically by placing the jumper on J8 in position B.
J6 (/WR)	When jumpered to the C position, the associated address determines which latch is loaded. In the fixed position, the 0B through 7B latches are transparent when the associated address is selected (both in conjunction with /CS).
J11 (/CS)	This signal allows the DAC latches to be loaded.
J7 (/CLR)	This signal must be low to allow the DACs to be loaded with values other than the fixed value of RGNB. In the /CLR position, it forces all DAC data inputs to RGNB, forcing the analog outputs to the value of RGNB. (The value depends on the reference inputs.)
J3, J14, J15 ($-V_{REF}$)	When jumpered, it allows the value of the $-V_{REF}$ (reference low) voltage (from the on-board op amp) to be supplied to this reference input (low side). When unjumpered, an external low reference may be input to the pin closest to the DAC.
J15, J16, J17 (CD_{REF})	When jumpered, the value of the RGND voltage (from the on-board op amp) is supplied to this reference input (high side). When it is unjumpered, an external high reference may be input to the pin closest to the DAC.
J18 (RGND)	Jumpering allows the value of the $+V_{REF}$ (reference high) voltage (from the on-board op amp) to be supplied to this reference offset to DAC 0 and 1.
J19 (RGND)	Jumperering allows the value of the RGND voltage (from the on-board op amp) to be supplied to this reference offset DAC 2, 3, 4, and 5. When it is unjumpered, an external high reference may be input to the pin closest to the DAC.

Table II - Control Table - Continued

NAME	DESCRIPTION
J20 (RGND)	When jumpered, the value of the RGND voltage (from on-board op amp) is supplied to this reference offset to DAC 6 and 7. When it is unjumpered, an external low reference may be input to the pin closest to the DAC.
J21	Selects ground or RGND for offset voltage.
REF LOW ADJ	(R26) This potentiometer adjusts the value for the $-V_{REF}$ (V_{DD} +0.3V to V_{SS} -0.3V). This may be supplied to the Reference Low inputs of the eight DACs
REF HIGH ADJ	(R27) This potentiometer adjusts the value for the $+V_{REF}$ (V_{DD} -0.3V to V_{SS} +0.3V).
RGND	(R25) This potentiometer adjusts the value for RGNB offset voltages (-2.0V to +2.0V).

OPERATIONAL DETAILS

RGND (R25), this potentiometer adjusts the value for RGND (-0.2V to +0.2V). This evaluation board was designed to be as flexible as possible for control of the eight DACs in the SPT5400. It was designed to operate just one DAC or all eight DACs in automatic sequence. To accomplish automatic sequencing through each DAC, a counter and a decoder were implemented on this evaluation board.

A description of the board when set to sequential eight DAC operation follows. (See the timing diagram as necessary.) The clock input supplies the clock for the counter. On the low half-cycle of the clock, the decoder output is enabled which allows for the active-low write strobe (this loads the first latch of the address pointed to by the counter) or enables the load for the respective address pointed to by the counter when the LSB of the counter is low or high respectively. The second half of the decoder is used to decode which load strobe is asserted. In the single address mode, the operation is the same except the address pointed to is fixed by the address select switch. Note that it takes two rising clock edges to complete a latched mode operation for either cycling through the eight DACs or a single DAC.

If the /WR (latch write signal) is forced low (jumpered to DGND), all the first latches are transparent when its associated address is asserted and stable. If any of the /LDXX (load DAC latch) is forced low, the second latch to the DAC pair is transparent. If a fixed voltage value out is required, at least one of the latches (write-latch or load-latch) must be made nontransparent (i.e., latch the data) at the appropriate data value input.

All control signals can be easily wired for external control. They include ADDRESS, /LDAB, /LDCD, /LDEF, /LDGH, /WR, /CLR, /PE and /CS.

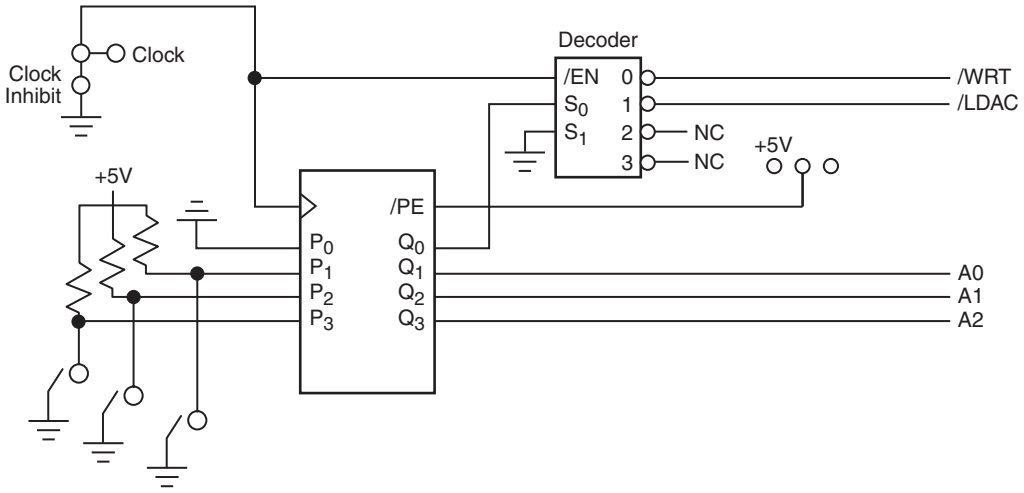
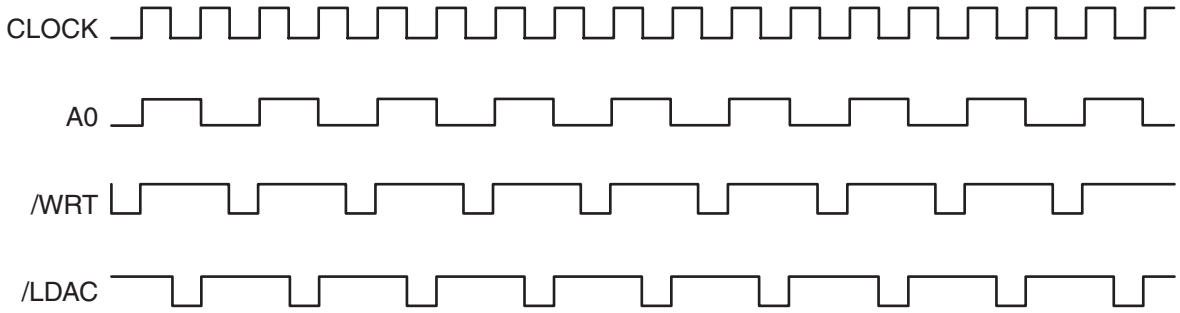


Figure 1 - Logic Control Circuit Diagram



NOTES:
1. Assume a 1kHz clock.
2. The timing diagram shows digital operation for SPT5420 applicationcard.
3. Refer to timing A0 to sync up data transitions with/WRT and /LDAC.
4. Refer to timing diagram in the technical datasheet for /CS and /WRT set up times.

Figure 2 - Timing Diagram

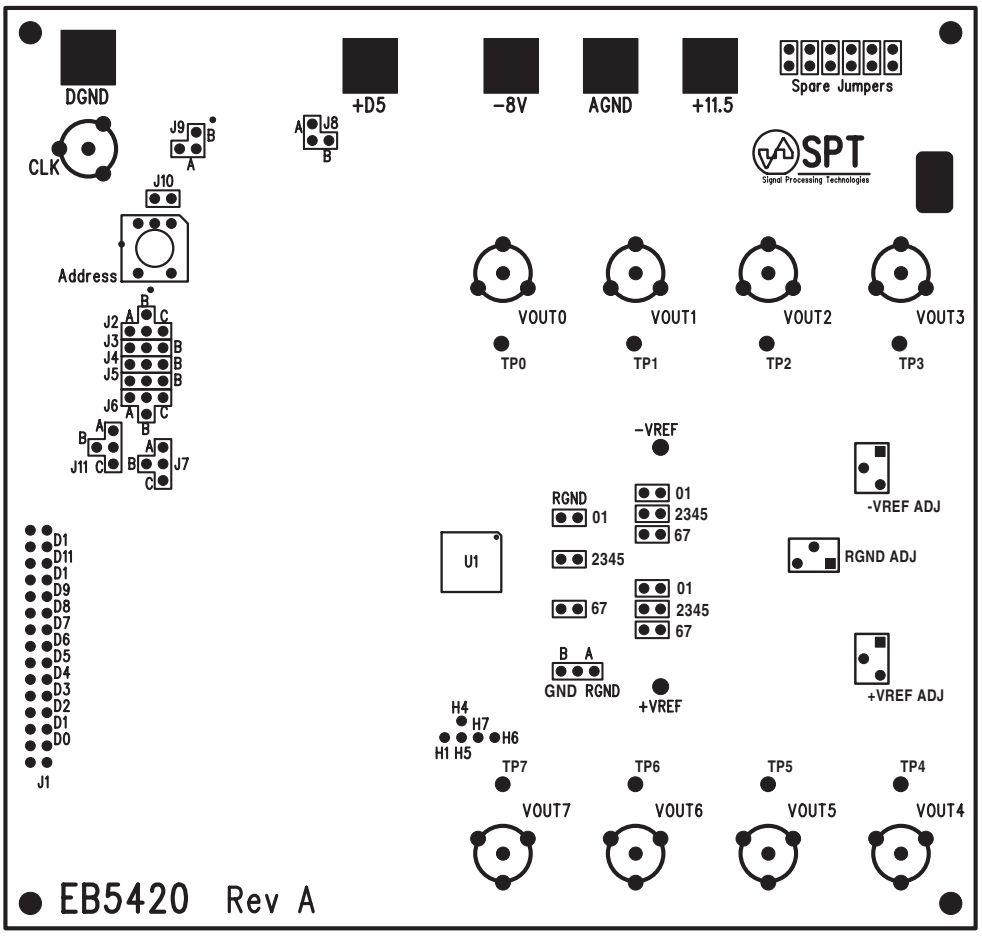


Figure 3 - Key Control Diagram

Table III - Key Control References

Part Name	Signal Name	Jumper Position	Pin Description
J1		N/A	Main signal port
J2	/LDAC	A	/LDAC provided by external connection through J1
		B	/LDAC pulled Low
		C	/LDAC provided by step count circuitry
J3	A2	A	A2 provided by external connection through J1
		B	A2 provided by step count circuitry
J4	A1	A	A1 provided by external connection through J1
		B	A1 provided by step count circuitry
J5	A0	A	A0 provided by external connection through J1
		B	A0 provided by step count circuitry
J7	/CLR	A	/CLR pulled High
		B	/CLR provided by external connection through J1
		C	/CLR pulled Low
J8	CH_Address	A	Active channel selected with address switch
		B	All 8 channels active
J9	CLK_enable	A	Clock provided through BNC(CLK)
		B	Clock disable
J10		on/off	Clock input provided through J1 when on
J11	/CS	A	/CS pulled High
		B	/CS provided by external connection through J1
		C	/CS pulled Low
J18	RGND 0,1	on/off	Provides RGND offset voltage to DAC's 0,1
J19	RGND 2,3,4,5	on/off	Provides RGND offset voltage to DAC's 2,3,4,5
J20	RGND 6,7	on/off	Provides RGND offset voltage to DAC's 6,7
J21	RGND	A	Provides RGND offset voltage to J18,J19,J20
		B	RGND voltage is set to null
J12	-Vref	on/off	Provides -Vref reference voltage to DAC's 0,1
J13	-Vref	on/off	Provides -Vref reference voltage to DAC's 2,3,4,5
J14	-Vref	on/off	Provides -Vref reference voltage to DAC's 6,7
J15	+Vref	on/off	Provides +Vref reference voltage to DAC's 0,1
J16	+Vref	on/off	Provides +Vref reference voltage to DAC's 2,3,4,5
J17	+Vref	on/off	Provides +Vref reference voltage to DAC's 6,7

CLOCK

A clock input is only required when operating the SPT5420 in its latched modes. If a latch mode is required, this design requires a clock that operates at two times the frequency of the data update rate. (See the timing diagram below.) The clock signal can be applied to the board via the BNC connector or to the J1 (connector pin 1).

REFERENCE CIRCUIT

There are eight DACs in the SPT5420. The reference voltage is shared by groups of two; that is, DACs 0-1 share the same reference voltages as do 2-3, 4-5 and 6-7.

Operation of the reference voltage for this evaluation board is as follows. A stable reference voltage is provided by J9. This provides the reference voltage for the reference high op amp, reference low amp and RGND offset voltage. The reference high voltage is supplied by one-half of U8 by adjusting R27. This op amp is designed with a gain of two which provides a reference high between 0 to +5V. The output of the op amp is sent to jumpers J15 through J17. The stable reference (4,7) from J9 is inverted by the second half of U8 and is used across a resistor bridging with the +4.7V to provide (±2V to 12V for RGND offset.

The other half of U7 is used to provide a low reference voltage. It is designed as a voltage follower. The output voltage may be adjusted between 0 and -5V. This reference low voltage can provide for a symmetrical bipolar up to unipolar operation and all levels in between.

The following are tips for other reference design concepts:

- Use a star configuration if all pins are using a common reference and/or ground reference.
- Separate reference buffering may be applied. Use op amps that can drive capacitive loads. Sense the reference voltage at the pin of the SPT5420 for accurate reference voltages.
- Input reference resistance for both Reference High and reference low input need to be considered when all input references are being driven from a common source (parallel loads). Refer to the minimum reference resistance information in the data sheet.
- The output of DAC may be used for a reference voltage to other DAC pairs. (Do not use the output as a self-reference.)

Refer to the Analog Output section of this document for attainable output voltage values with the SPT5420.

MULTIPLYING OPERATION

The SPT5420 can be used for multiplying in a two-quadrant application. When using AC signals on the reference inputs, do not use filter capacitors. Limit the amplitude of the input Reference High and refernce low inputs to the level the output can achieve. Refer to the Analog Output section to determine the level the reference input signals can attain. The input capacitance of the reference pins is not sufficient to serve as a low-pass filter in the frequency range in which the SPT5420 multiplies. To achieve near 13-bit results in multiplying applications, the input reference voltage must not slew at a rate that causes the output to slew faster than the rate specified in the data sheet.

ANALOG OUTPUT

The output can operate in bipolar or a level-shifted unipolar operation. Due to a common reference to a pair of DACs, there will be a slight perturbation from one to the other output when one DAC is updated.

Always refer to the latest data sheet for this part when designing for a specific output voltage requirement.

Table VI - Reference Voltage Settings vs. Output Voltage

Parameter	Description	Output Voltage Value
Volts per LSB (V/LSB)	Voltage per bit	$2*(V_{REFT} - V_{REFB})/8192$
Positive full scale	Full Scale (1FFFh) high	$2*(V_{REFB} + [V_{REFT} - V_{REFB}])$
Negative full scale	Full Scale (0000h) low	$2* V_{REFB} - V_{RGND}$
Mid scale	Middle scale (1000h) MID	$V_{REFT} + V_{REFB} - V_{RGND}$
Output vs. Digital Input	D (digital input pattern) D=0 to 8191	$2*(V_{REFB}+[V_{REFT}-V_{REFB}])*\text{input code}/8192)-V_{RGND}$

NOTES:
1. Bipolar Operation: For symmetrical bipolar operation, set the reference high and reference low equal to each other and V_{RGND} to 0V.
2. Unipolar Operation: For positive unipolar operation, set the reference high to maximum positive full scale value and reference low to zero volts.

LAYOUT

Fairchild carefully considered the layout of this evaluation board to ensure maximum performance of the part. It was designed to aid the user in developing similar designs and layout aspects. Some highlights of the design are as follows:

- Stable reference voltage designs
- Digital pull-down resistors to protect input to the SPT5420
- Series resistors for transient suppression
- Generous decoupling and filtering on all power supply and analog input signals
- Split power and ground planes

TEST POINTS

There are several test points on key signals. They are described in the table below.

Table V - Key Signal Test Points

TEST	DESCRIPTION
V_{OUTX}	Analog output signal from the respective DAC.
$+V_{REF}$	Reference High, i.e., the reference voltage sourced by the on-board reference buffer op amp.
/WR	Monitors the active-low write signal pin of the DAC.
$-V_{REF}$	Reference Low, i.e., the reference voltage sourced by the on-board reference buffer op amp.
/LDAC	Monitors the respective active-low load pins (AB - GH).
D0	Monitors the LSB pin of the DAC.
DGND, AGND,	Test points ground.

INITIAL SETUP AND OPERATIONAL CHECK

Before connecting to the J1 connector, verify that all power sources, including logic, are disabled,

Perform the following steps for initial set up and functional verification.

1. Set the power supplies to within ± 100 mV of their nominal value.
2. Connect the power supplies to their respective test point input. (Refer to the pin connection table.)
3. Ensure that the logic input signals (including the clock signal) are at zero volts and are powered off.
4. Connect the customer-provided J1 connector.
5. Depending on your clock source, do the following:
   J1-pin 1 input: Install R4 and remove R5 (GND clock input). Remove R4 and install R5 (51.1Ω).
6. Set the clock input to 1 kHz, square wave TTL level. Disable before connecting to the EB5420.
7. Set all controls and jumpers indicated in the table as follows: (Refer to key table diagram.)

Table VI - Control/Jumper Positions

Control/ Jumper	Position	Control/ Jumper	Position
J9 (CLK EN)	A	–	–
J8 (/PE)	B	J18-J20	Jumper all
J3, J4, J5	B	J21	A
J2, J6	C	H4-H5	Jumper
J11/CS	C	H6-H7	Jumper
J7/CLR	A	–	–
J12-J17	Jumper all	J10	Open

8. Turn on the power supplies.
9. Set Reference High to +3.5V by adjusting R27.
10. Set Reference Low to -1.5V by adjusting R26. Set RGND to 0.0V by adjusting R25.
11. Set the clock to enable. Set the input data pattern to 0000 hex (minimum input) at logic inputs.
12. Monitor the output of each analog signal (V_{OUT0} through V_{OUT7}). Verify that the output levels are at 1.99V ± data sheet value for code error.
13. Set the input data pattern to 1FFF hex (maximum input) and monitor the analog outputs. Verify that the output is 6.99V ± data sheet value for gain error.
14. Jumper the /CLR position (C). Verify that all outputs go to RGND. (Include the calculated mid scale offset based on the zero and gain values obtained in steps 11 and 12.)
15. This concludes initial functional operation. For other desired operation, ensure the data update relative to the respective clock meets setup and hold times.

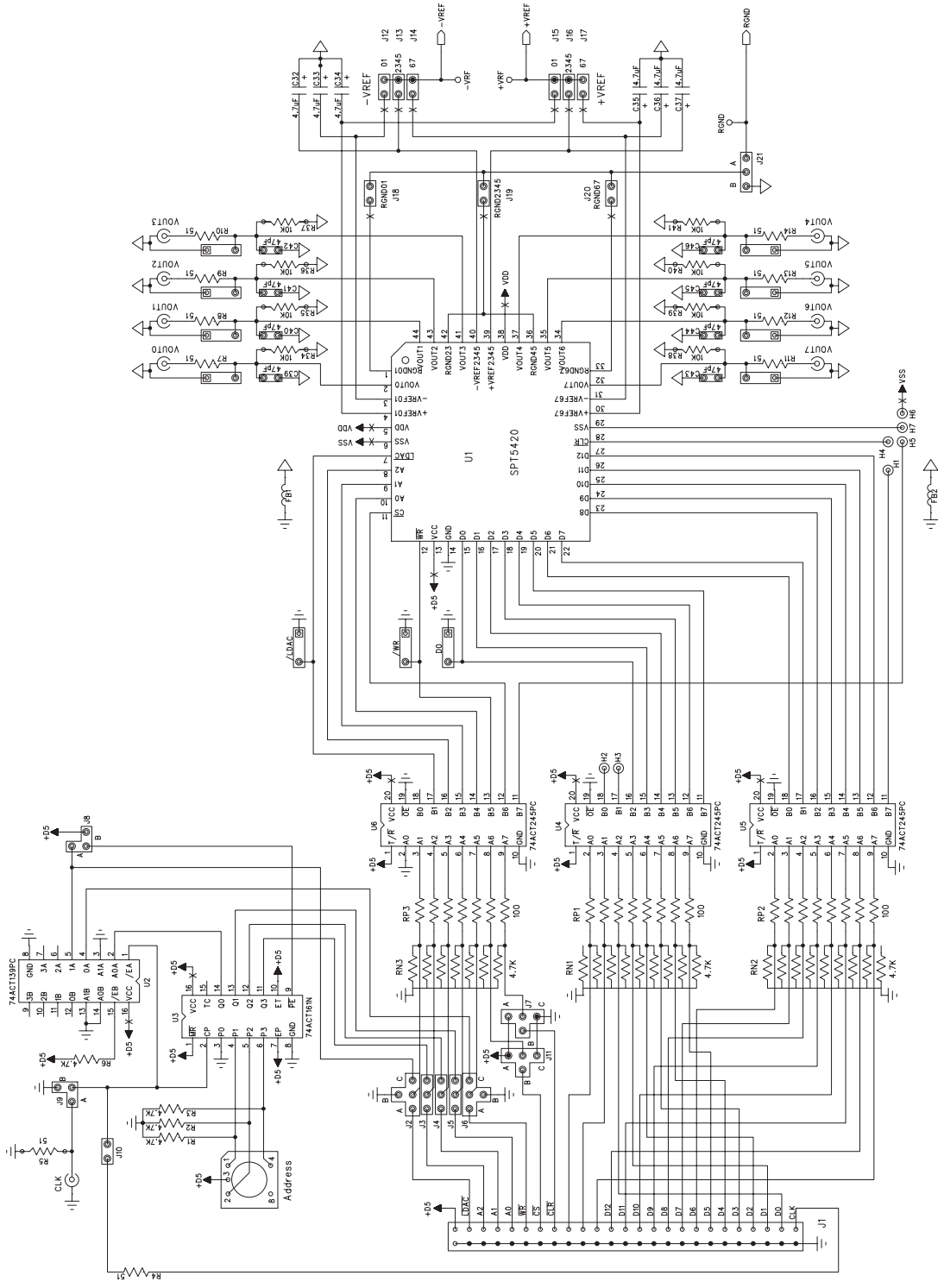


Figure 4 - Detailed Schematic, Rev. B Board

Table VII - Bill of Materials

	Reference	Vendor Part No.	Description	Qty	Vendor
1	C1-4	ECS-T1CX106R	10µF Tantalum Chip Cap	4	Panasonic/Any
2	C5	12062R103K9B20D	0.01µF Chip Cap	1	Philips/Any
3	C6-30	12062R104K9B20D	0.1µF Chip Cap	25	Philips/Any
4	C32-37	ECS-T1CY475R	4.7µF Tantalum Chip Cap	6	Panasonic/Any
5	C38	ECS-T1CY105R	1µF Tantalum Chip Cap	1	Panasonic/Any
6	C39-46	ECU-S2A470JCA	47pF Radial Cap (socketed)	8	Panasonic/Any
7	D1,8	SD103B	Schottky Diode	2	Vishay/LiteOn
8	D2-7,9-12	1N4148DICT	Switching Diode	10	Vishay/LiteOn
9	FB1,2	EXC-ELSA35V	Ferrite Bead	2	Panasonic
10	J1	SSW-125-22-S-D-RA	50-pin Rt Ang Female Connector	1	Samtec
11	J2-21,36-41	PZC36SAAN	Jumper Pins (trim from 36-pin)	2	Sullins
12	J22-29,35	31-5329	BNC Connector	9	Amphenol
13	J30-34	108-0740-001	Banana Jack	5	Johnson
14	J42,43		Bare Jumper Wire	2	
15	R1-3,6	ERJ-8ENF4751	4.7k Chip Resistor	4	Panasonic/Any
16	R4,7-14,31-33	ERJ-8ENF51R1	51.1Ω Chip Resistor	12	Panasonic/Any
17	R5	MFR-25FBF 51R1	51.1Ω Axial Resistor (socketed)	1	Yageo/Any
18	R15,20,21-24	ERJ-8ENF4991	4.99kΩ Chip Resistor	6	Panasonic/Any
19	R16,17	ERJ-8ENF3011	3.01kΩ Chip Resistor	2	Panasonic/Any
20	R18,19	ERJ-8ENF4531	4.53kΩ Chip Resistor	2	Panasonic/Any
21	R25-27	3266W-1-502	5k Potentiometer	3	Bourns
22	R28-30	ERJ-8ENF22R1	22.1Ω Chip Resistor	3	Panasonic/Any
23	R34-41	MFR-25FBF 10K0	10kΩ Axial Resistor (socketed)	8	Yageo/Any
24	RN1,2	770-101-R4.7K [socket]*	10-pin 9-Res SIP Network	2	CTS
25	RN3	770-81-R4.7K [socket]*	8-pin 7 Res SIP Network	1	CTS
26	RP1,2	761-3-R100	100Ω 8-Res DIP Array	2	CTS
27	RP3	760-3-R100	100Ω 7-Res DIP Array	1	CTS
28	SW1	A6A-16R	Rotary DIP Switch	1	Omron
29	TP1-3	40F6045	Solder Terminal	3	NEWARK
30	U1	SPT5420	13-bit Octal Voltage DAC	1	SPT
31	U2	74ACT139PC	Dual 1-of-4 Decoder	1	Fairchild
32	U3	74ACT161N	Synchronous Counter	1	Motorola
33	U4,5,6	74ACT245PC	Octal Bus Transceiver	3	Fairchild
34	U7,8	OPA2130PA	FET-Input Op Amp	2	Burr-Brown
35	U9	TK11247B	4.7V Voltage Regulator	1	Toko
36	N/A	ED7636-ND*	Socket for Items 24,25 (trim from 36)	1	DIGI-KEY
37	N/A	ED5044-ND	Pin Receptacles (for “socketed” parts)	34	DIGI-KEY
38	N/A	929955-06	Shunt for Jumper	20	DIGI-KEY (3M)
39	N/A	1902EK-ND (Note 1)	1” Nylon Spacer	4	DIGI-KEY
40	N/A	H143-ND (Note 1)	4-40 Pan-head Screw	4	DIGI-KEY
41	EB5420	Rev A	Evaluation Board	1	Short Circuits

NOTE: 1 Mount in four corners as bottom side legs.

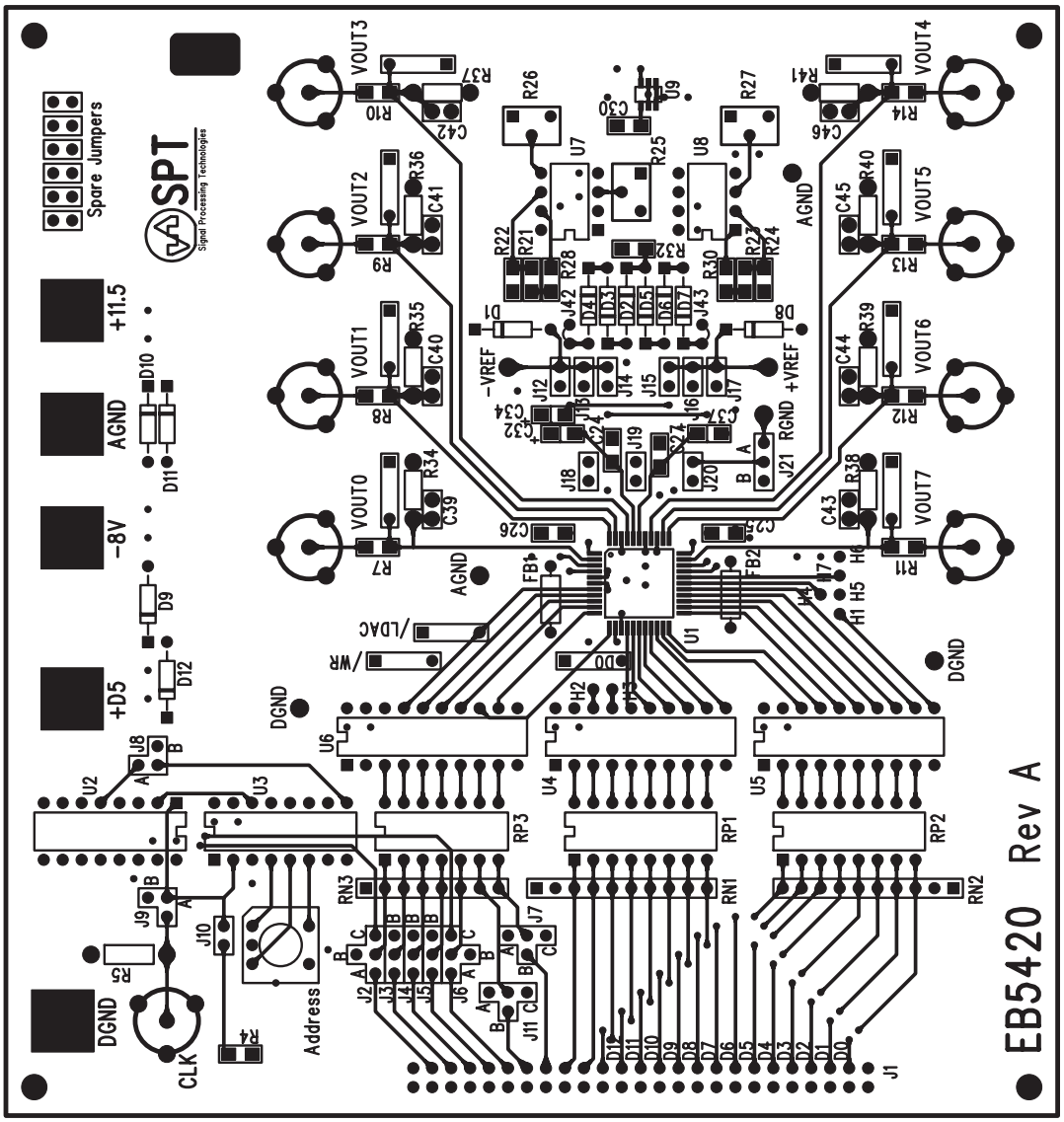


Figure 5 - EB5420 Top Layer

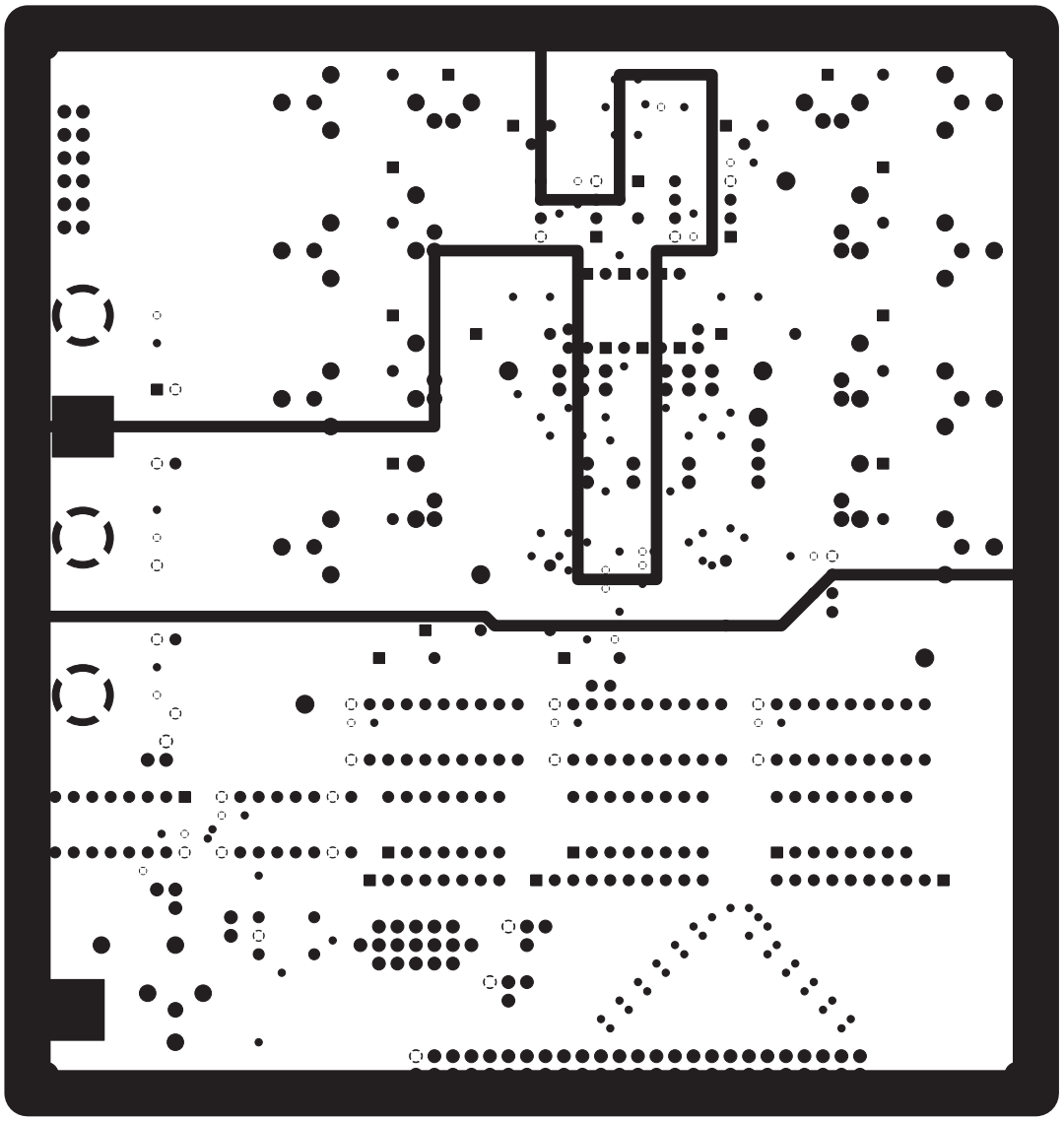


Figure 6 - EB5420 Power Layer

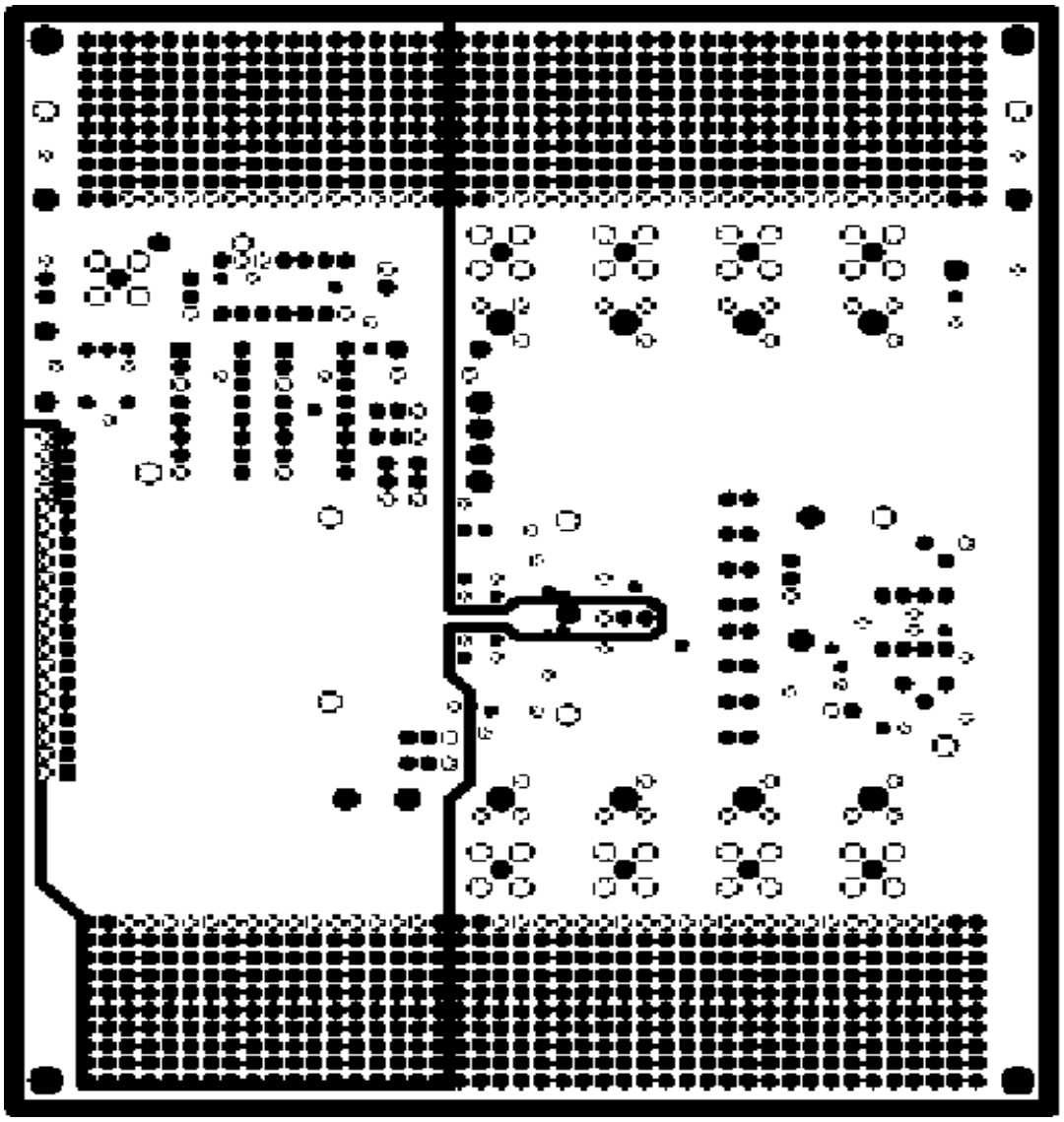


Figure 7 - EB5420 Ground Layer

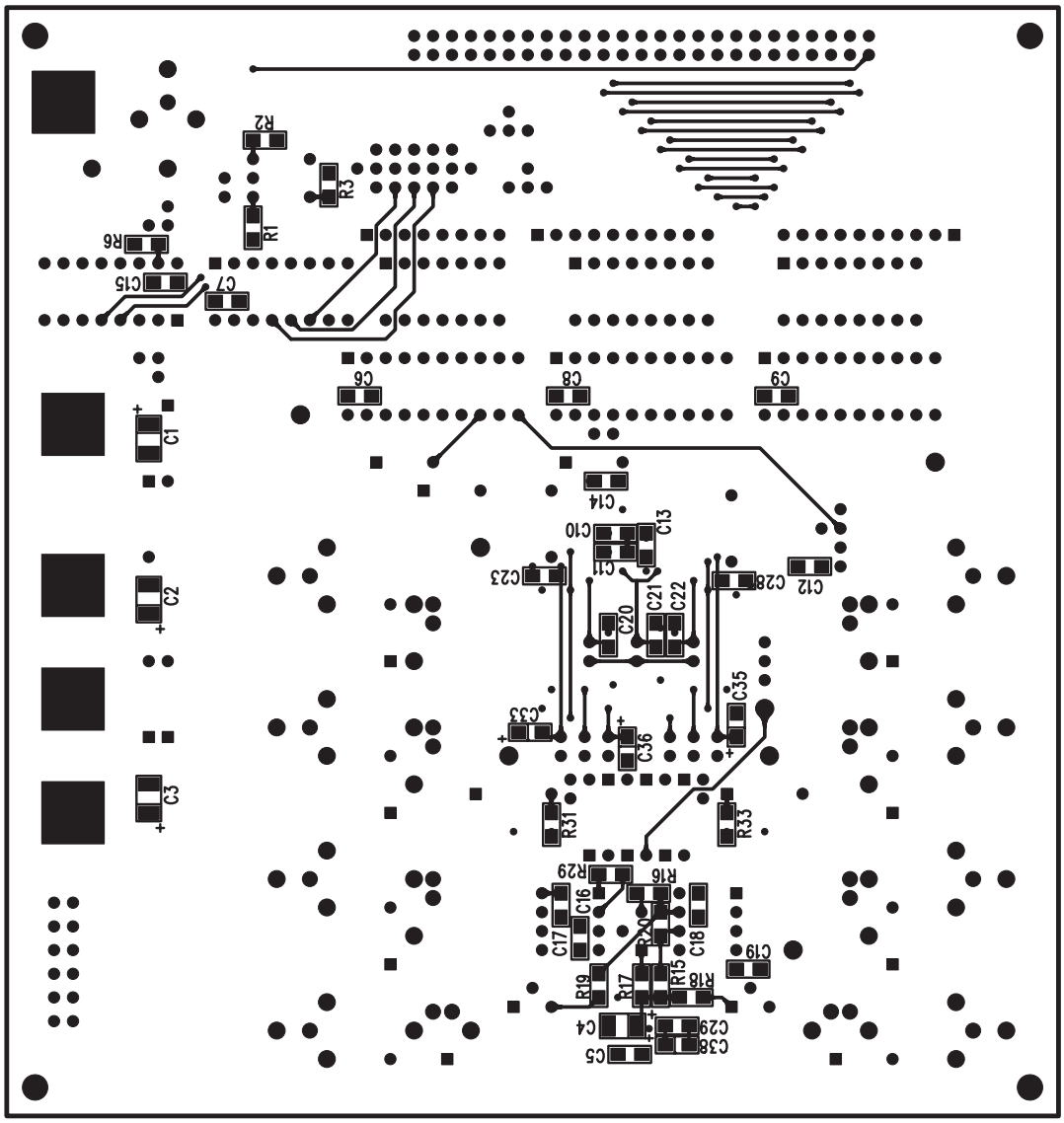


Figure 8 - EB5420 Bottom Layer

DISCLAIMER

LIFE SUPPORT POLICY