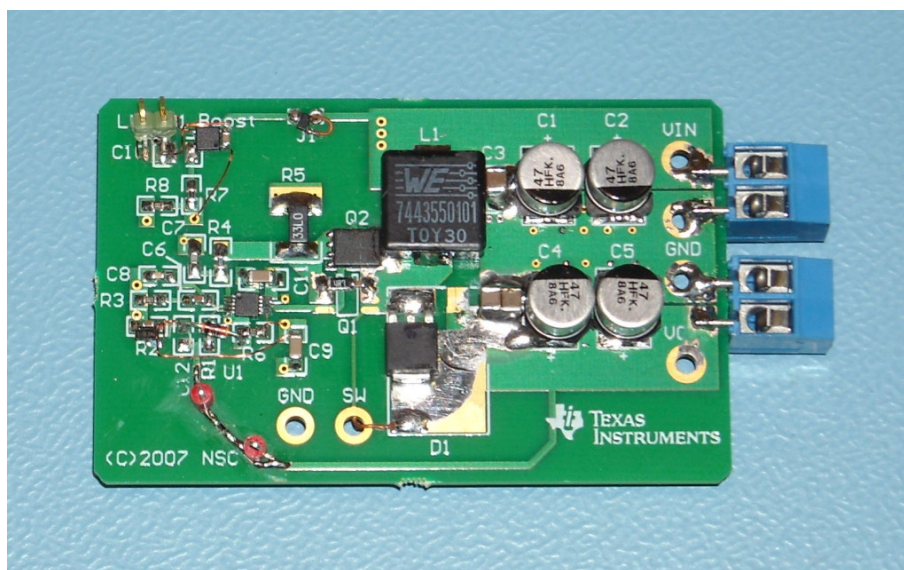


LM3481 Boost Circuit - 9.5V @ 1.5A

- Input 4..10V DC
Can withstand up to 40V
- Output 9.5V @ 1.5A
- Working in continuous conduction mode
- Enable/disable by logic signal (3.3V or 5.0V)
- Built on PCB LM3481 Boost EVM



1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 5.0V, with no load on the 9.5V output.

The boost is switched on by the enable signal.

Channel C1: **Input voltage**
2V/div, 50ms/div

Channel C2: **Output voltage**
2V/div, 50ms/div

Channel C3: **Enable signal**
2V/div, 50ms/div

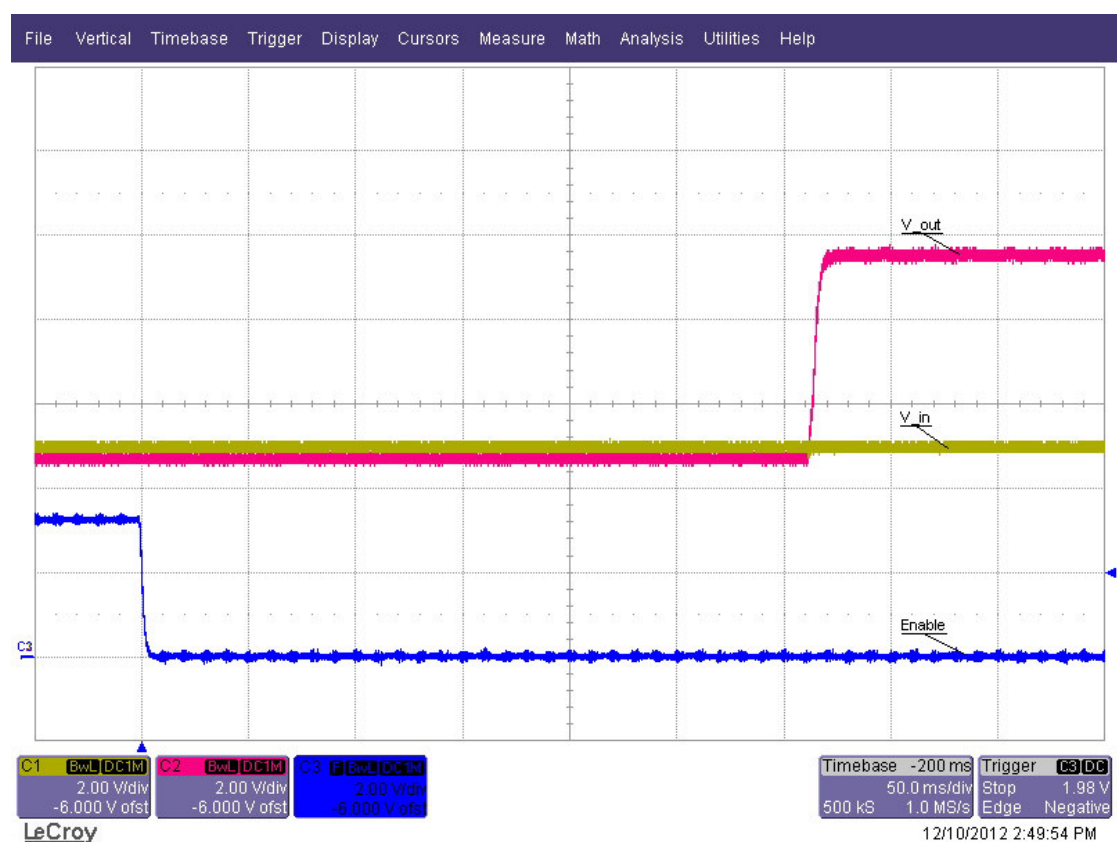


Figure 1

2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage is set at 5.0V with a 1.5A load on the 9.5V output.

The boost is switched off by the enable signal.

Channel C1: **Input voltage**
2V/div, 200us/div

Channel C2: **Output voltage**
2V/div, 200us/div

Channel C3: **Enable signal**
2V/div, 200us/div

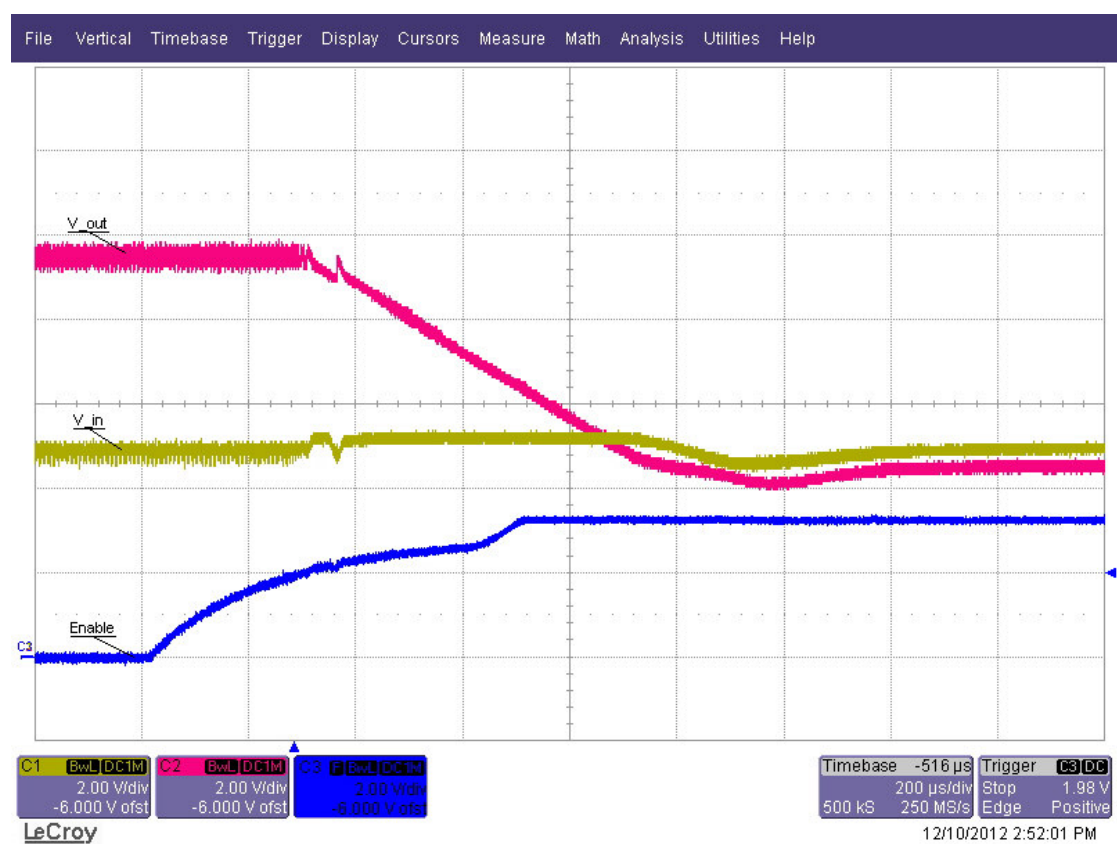


Figure 2

3 Efficiency

The efficiency and load regulation at 4.0V, 6.0V and 9.0V input voltage are shown in Figure 3 and Figure 4.

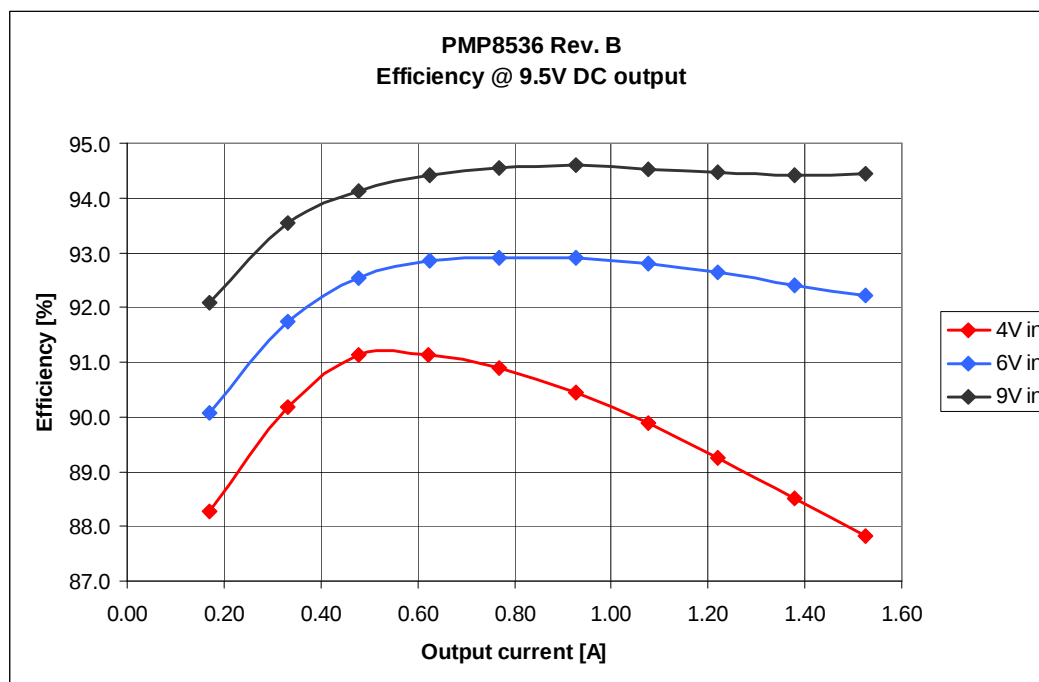


Figure 3

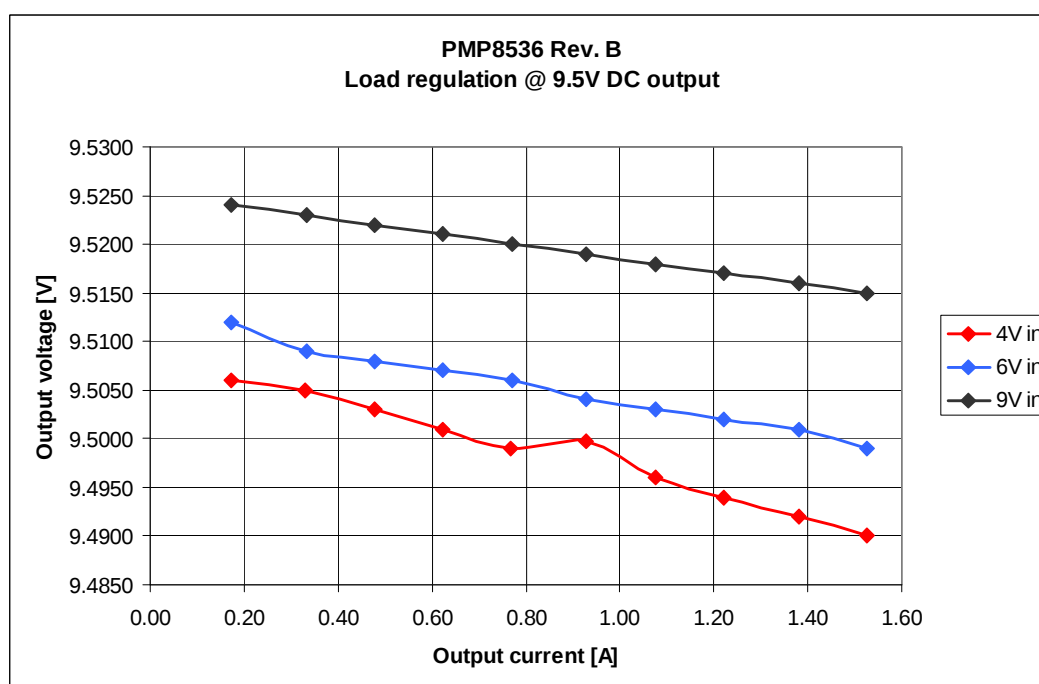


Figure 4

4 Output ripple voltage

The output ripple voltage at 1.5A load and 4.0V, 6.0V and 9.0V input voltage is shown in Figure 5.

Channel M1: **Output voltage**, AC coupled, 36mV peak-peak, **4.0V in**
50mV/div, 5us/div

Channel M2: **Output voltage**, AC coupled, 36mV peak-peak, **6.0V in**
50mV/div, 5us/div

Channel M2: **Output voltage**, AC coupled, 15mV peak-peak, **9.0V in**
50mV/div, 5us/div

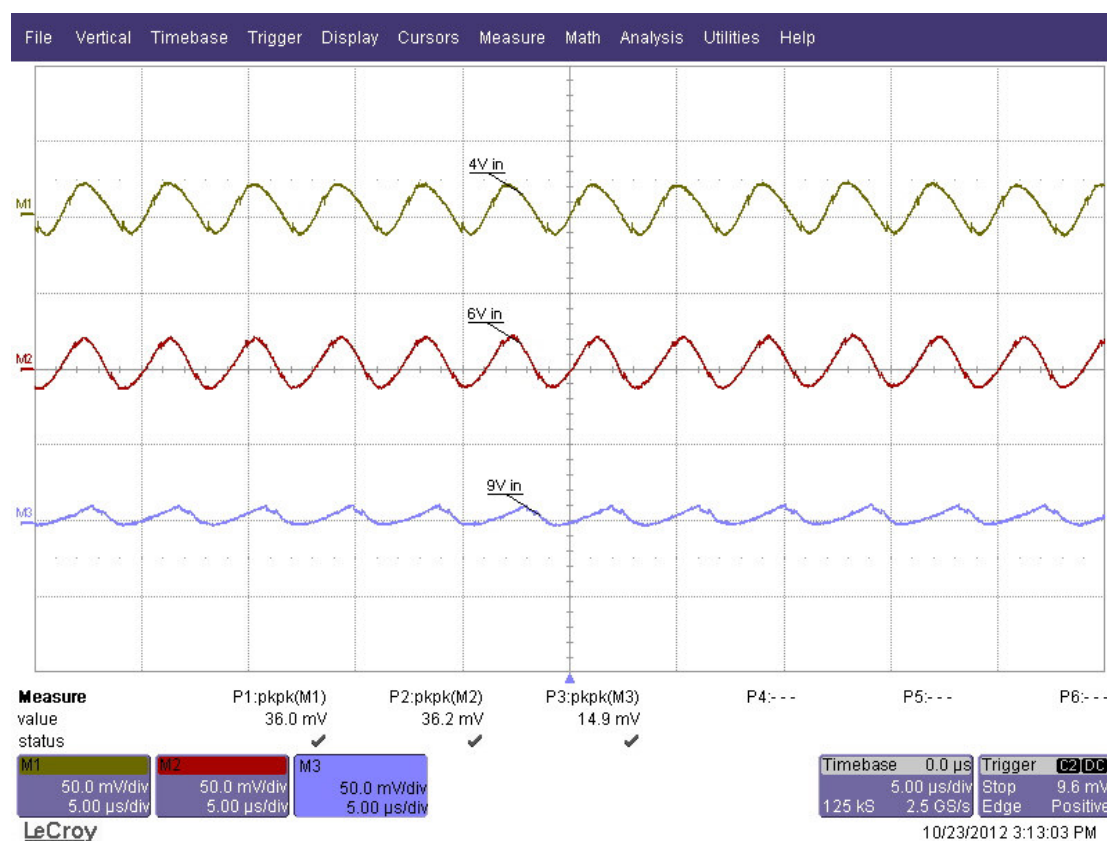


Figure 5

5 Load step

The response to a load step and a load dump at an input voltage of 4.0V is shown in Figure 6.

Channel C2: **Output voltage**, -552mV undershoot, 504mV overshoot
500mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step **0.75A to 1.5A** and vice versa
1A/div, 1ms/div

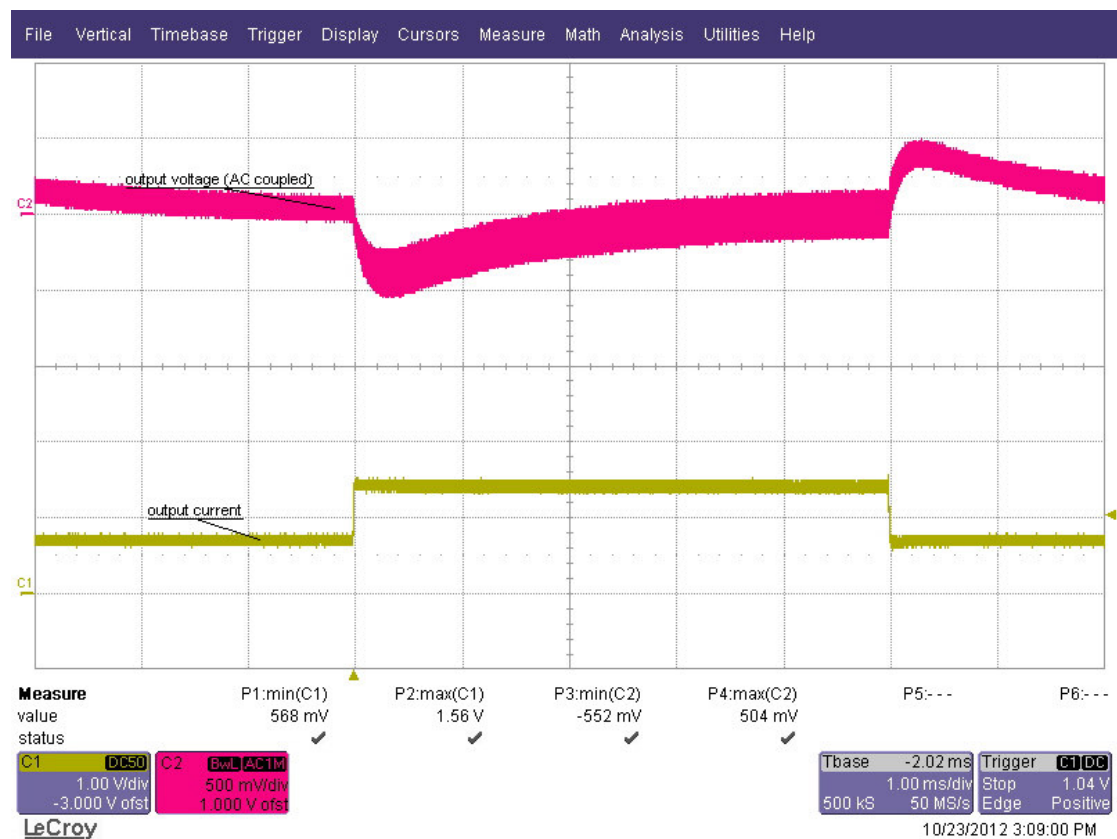


Figure 6

6 Frequency response

Figure 7 shows the loop response of the 9.5V output with 4.0V and 6.0V input voltage and a 1.5A load.

4.0V in 85 deg phase margin @ crossover frequency 1.1 kHz
 -22 db gain margin

6.0V in 85 deg phase margin @ crossover frequency 1.9 kHz
 -27 db gain margin

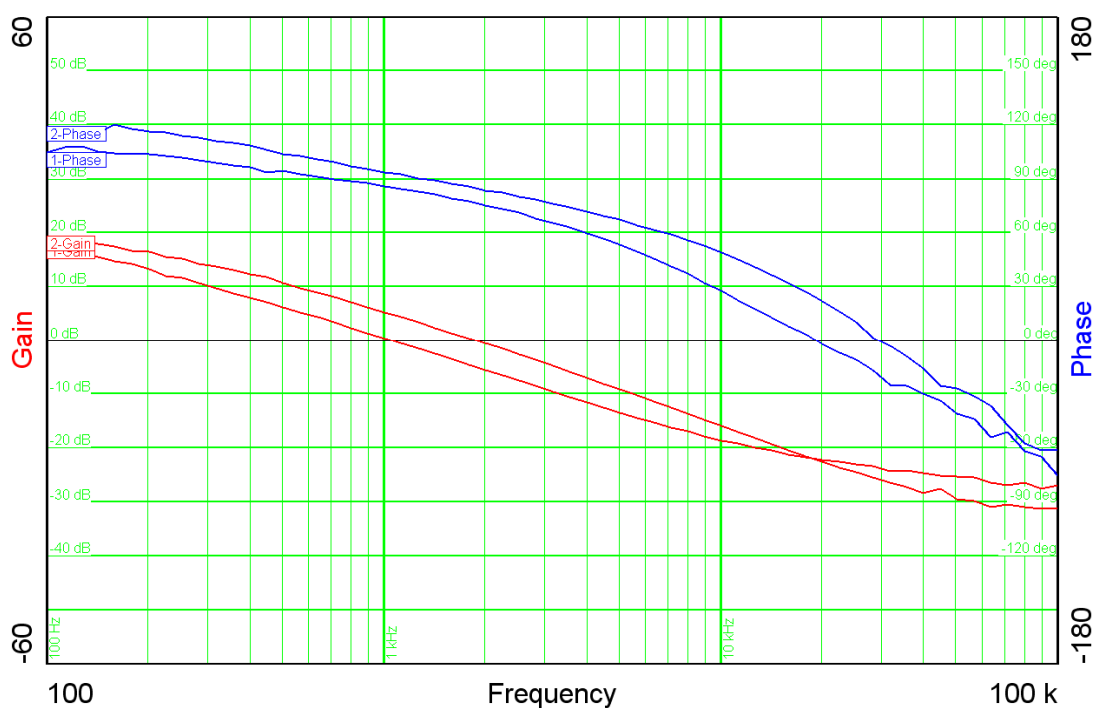


Figure 7

7 Miscellaneous waveforms

The drain-source voltage on the switching node is shown in Figure 8. The image was captured with 4.0V input and a 1.5A load.

Channel C2: **Drain-source voltage**, -0.6V minimum voltage, 18.9V maximum voltage
5V/div, 2 μ s/div

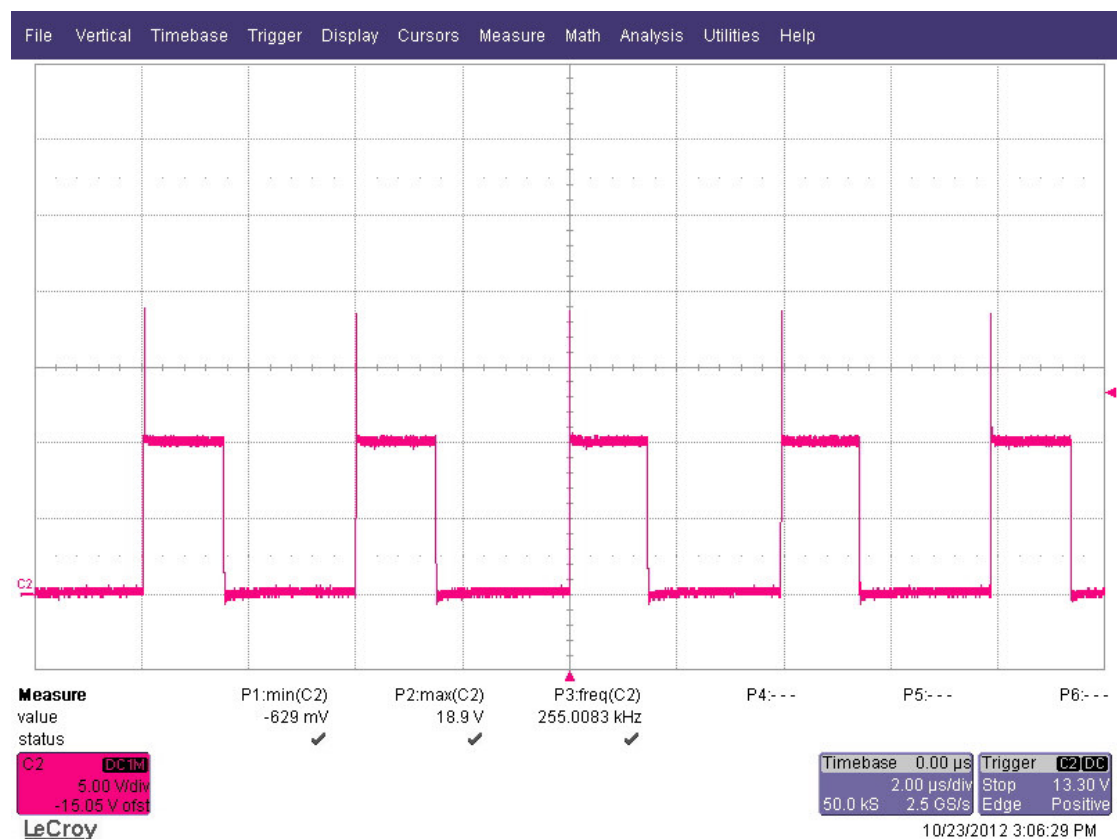


Figure 8

8 Thermal measurement

The thermal image (Figure 9) shows the circuit at an ambient temperature of 21 °C with an input voltage of 12.0V and a load of 2.5A.

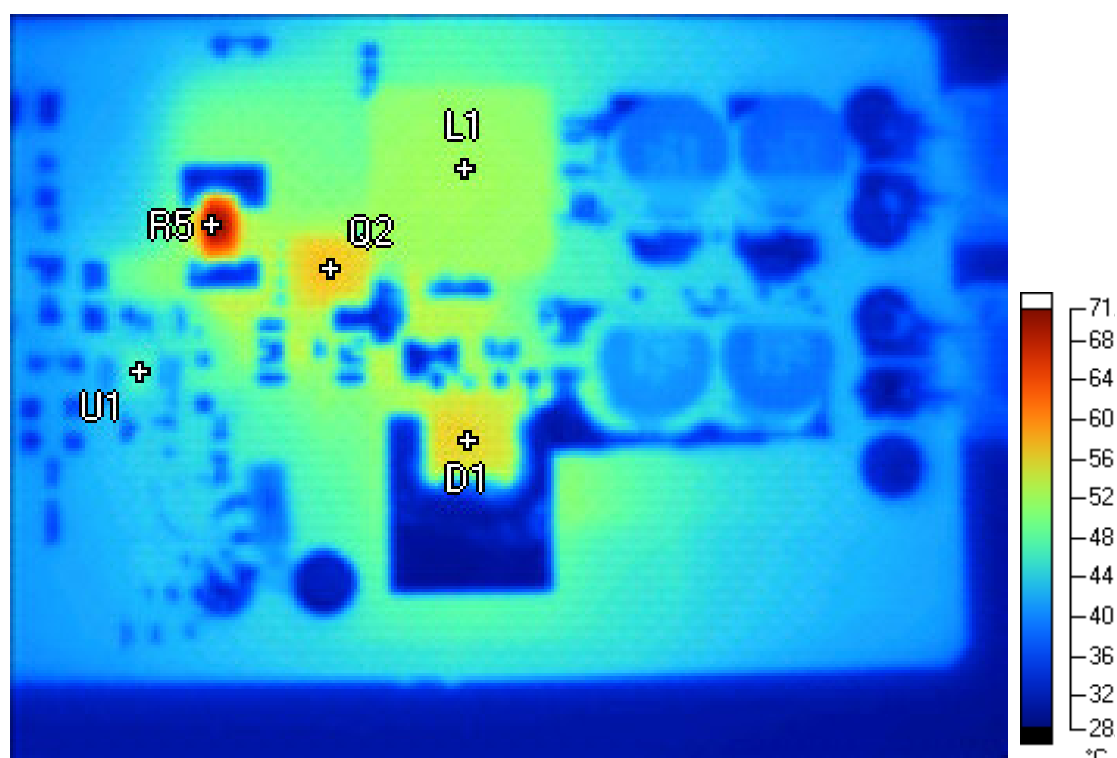


Figure 9

Markers

Label	Temperature	Emissivity	Background
L1	52.0 °C	0.95	21.0 °C
R5	70.4 °C	0.95	21.0 °C
Q2	56.7 °C	0.95	21.0 °C
D1	55.9 °C	0.95	21.0 °C
U1	46.5 °C	0.95	21.0 °C

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