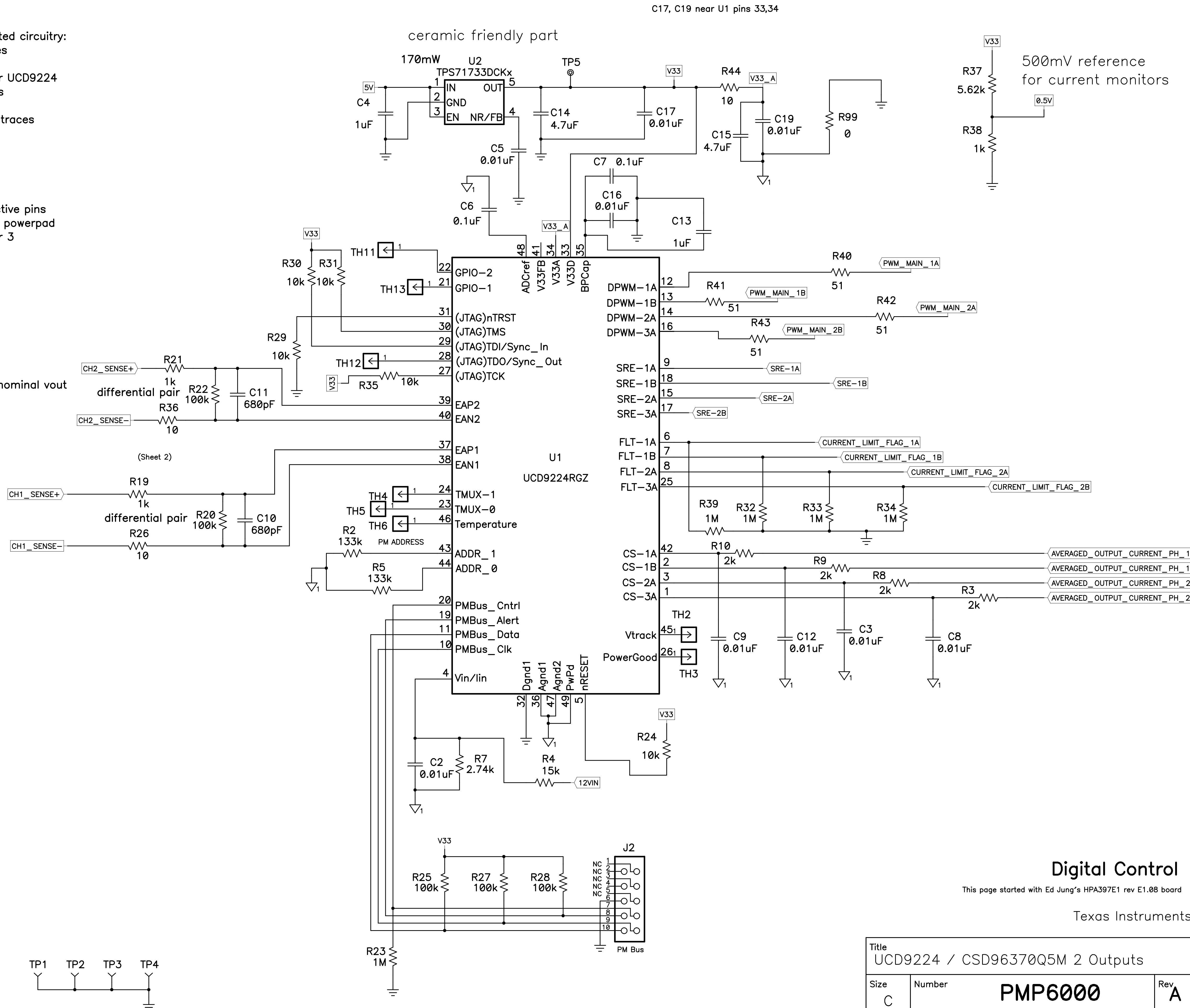
Layout plan for UCD9224 & related circuitry:
Top & bottom layer: Signal traces
Layer two: ground plane
layer 3: Analog ground near near UCD9224
to pick up all analog connections
and V33 elsewhere
if inner layers needed for signal traces
use layer 3, not 2

Generally: most critical to get
filter caps close as possible to respective pins
Pins 36 7 47 to be tied directly to U1 powerpad
and have a feed thru close by to layer 3

target 1.2v across eap – ean at nominal vout


C17, C19 near U1 pins 33,34
ceramic friendly part
170mW
U2
TPS71733DCKx
IN
OUT
GND
EN
NR/FB
5V
C4
1uF
TP5
V33
C14
4.7uF
C17
0.01uF
C5
0.01uF
R44
10
V33_A
C15
4.7uF
C19
0.01uF
R99
0
C7 0.1uF
C16
0.01uF
C13
1uF
C6
0.1uF
V33_A
500mV reference
for current monitors
R37
5.62k
0.5V
R38
1k
TH11
TH13
R30
10k
R31
10k
R29
10k
TH12
R35
10k
CH2_SENSE+
R21
1k
differential pair
R22
100k
C11
680pF
CH2_SENSE–
R36
10
(Sheet 2)
CH1_SENSE+
R19
1k
differential pair
R20
100k
C10
680pF
CH1_SENSE–
R26
10
TH4
TH5
TH6
PM ADDRESS
R2
133k
R5
133k
GPIO–2
GPIO–1
(JTAG)nTRST
(JTAG)TMS
(JTAG)TDI/Sync_In
(JTAG)TDO/Sync_Out
(JTAG)TCK
EAP2
EAN2
EAP1
EAN1
TMUX–1
TMUX–0
Temperature
ADDR_1
ADDR_0
PMBus_Cntrl
PMBus_Alert
PMBus_Data
PMBus_Clk
Vin/lin
ADCref
V33FB
V33A
V33D
BPCap
U1
UCD9224RGZ
DPWM–1A
DPWM–1B
DPWM–2A
DPWM–3A
SRE–1A
SRE–1B
SRE–2A
SRE–3A
FLT–1A
FLT–1B
FLT–2A
FLT–3A
CS–1A
CS–1B
CS–2A
CS–3A
Vtrack
PowerGood
Dgnd1
Agnd1
Agnd2
PwPd
nRESET
R40
51
PWM_MAIN_1A
R41
51
PWM_MAIN_1B
R42
51
PWM_MAIN_2A
R43
51
PWM_MAIN_2B
SRE–1A
SRE–1B
SRE–2A
SRE–2B
CURRENT_LIMIT_FLAG_1A
CURRENT_LIMIT_FLAG_1B
CURRENT_LIMIT_FLAG_2A
CURRENT_LIMIT_FLAG_2B
R39
1M
R32
1M
R33
1M
R34
1M
R10
2k
R9
2k
R8
2k
R3
2k
AVERAGED_OUTPUT_CURRENT_PH_1A
AVERAGED_OUTPUT_CURRENT_PH_1B
AVERAGED_OUTPUT_CURRENT_PH_2A
AVERAGED_OUTPUT_CURRENT_PH_2B
TH2
TH3
C9
0.01uF
C12
0.01uF
C3
0.01uF
C8
0.01uF
R24
10k
C2
0.01uF
R7
2.74k
R4
15k
12VIN
V33
R25
100k
R27
100k
R28
100k
J2
NC
PM Bus
R23
1M
TP1
TP2
TP3
TP4

Digital Control

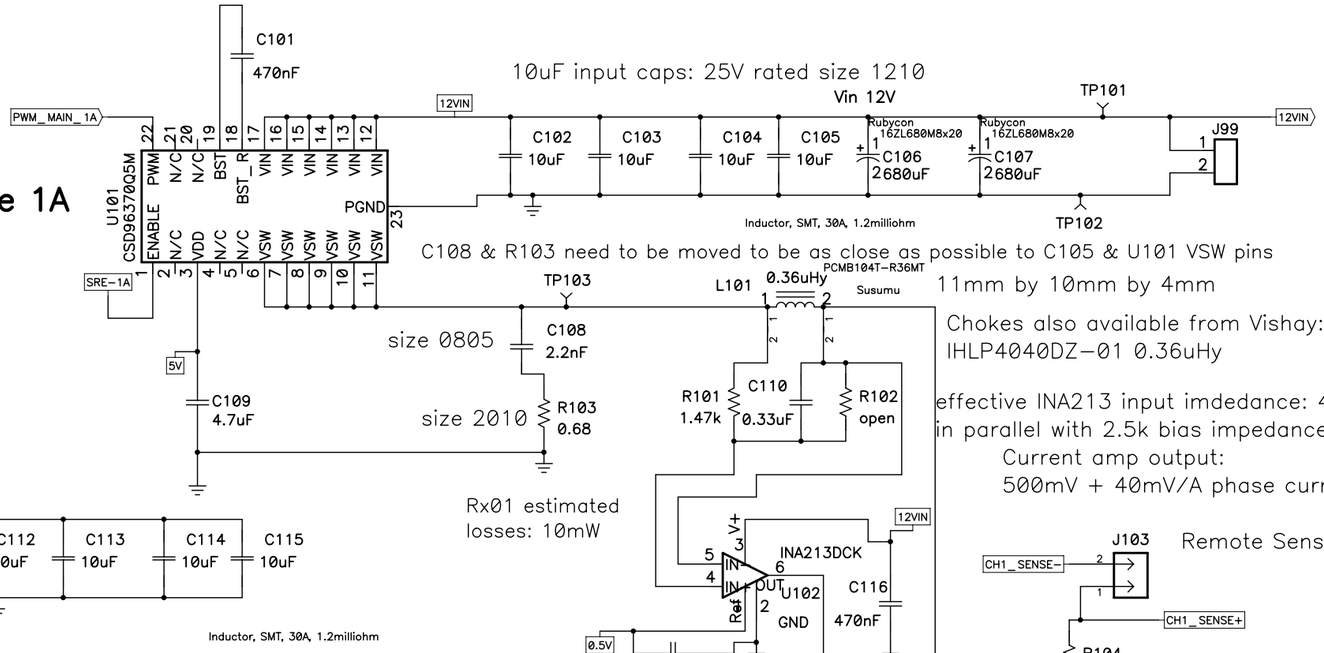
This page started with Ed Jung's HPA397E1 rev E1.08 board

Texas Instruments

Title	UCD9224 / CSD96370Q5M 2 Outputs	
Size C	Number PMP6000	Rev A
Date February 16, 2011	Drawn by Josh Mandelcorn	
Engineer Josh Mandelcorn	Filename PMP6000_revA.sch	Sheet 1 of 3

Layout plan for power stages:
layers top & bottom for most power and signal traces
layer 2 will be ground,
power pad of U101 and U103 to ground with several vias
Get as much ground plane around U101 and U103 on each layer to cool these parts

Pwr Stage 1A



Pwr Stage 1B

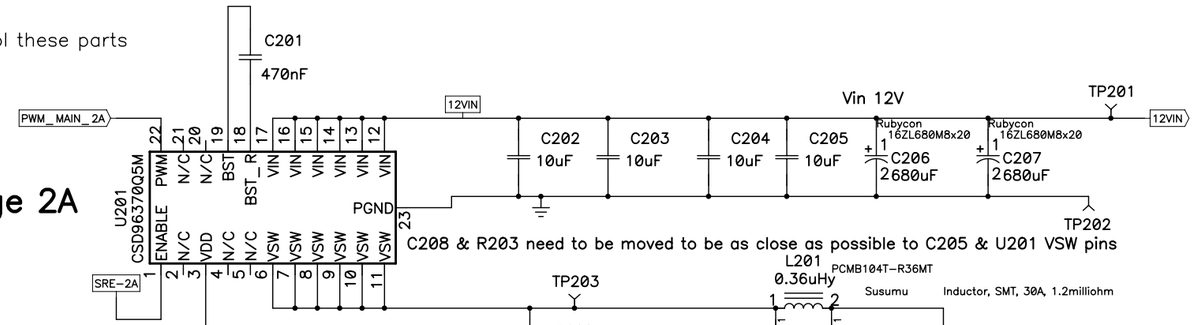
Channel 1

Texas Instruments

Title: UCD9224 / CSD96370Q5M 2 Outputs		
Size: C	Number: PMP6000	Rev: A
Date: February 16, 2011		Drawn by: Josh Mandelcorn
Engineer: Josh Mandelcorn	Filename: PMP6000_revA.sch	Sheet: 2 of 3

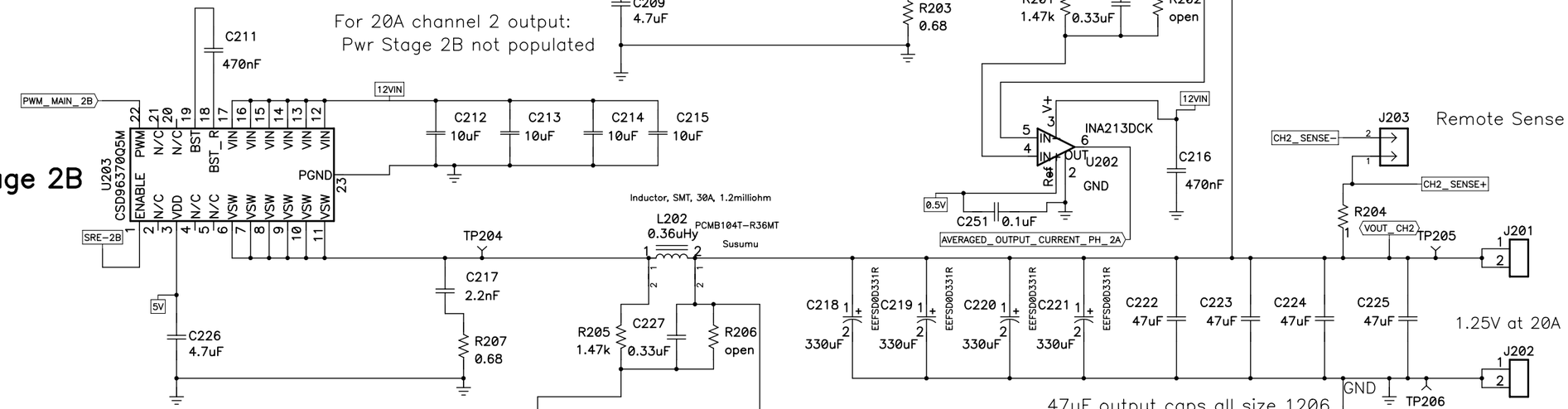
Layout plan for power stages:
layers top & bottom for most power and signal traces
layer 2 will be ground,
power pad of U201 and U203 to ground with several vias
Get as much ground plane around U201 and U203 on each layer to cool these parts

Pwr Stage 2A



For 20A channel 2 output:
Pwr Stage 2B not populated

Pwr Stage 2B



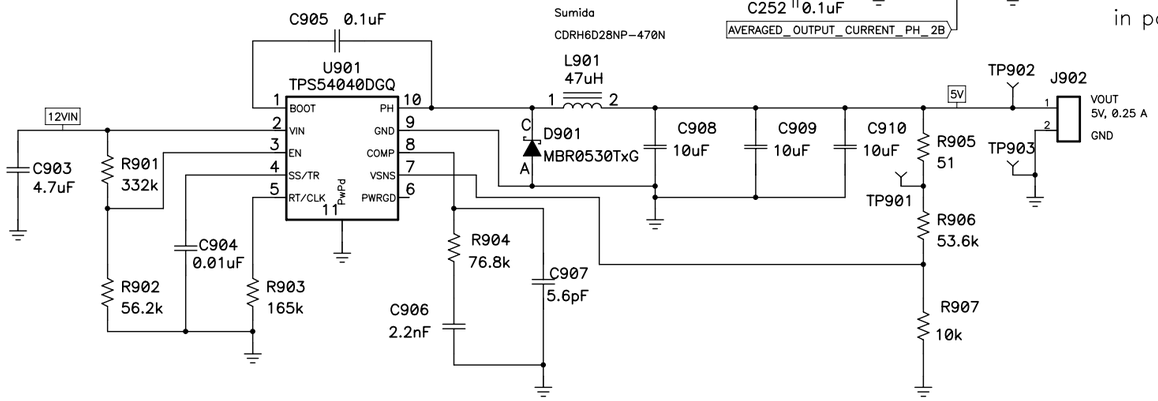
C217 & R207 need to be moved to be as close as possible to C215 & U203 VSW pins

47uF output caps all size 1206

All 4 output ceramics need to be in one place
near positive output connector
on current rev A layout:
stack Cx22 / Cx23 on top of Cx24 / Cx25

effective INA213 input imdedance: 40k
in parallel with 2.5k bias impedance or 2.353k
target 500mV + 40mV/A typical
48mV/A max or about 2V at 30A

Bias For Gate Drive



Channel 2 & 5V

Texas Instruments

Title: UCD9224 / CSD96370Q5M 2 Outputs			
Size: C	Number: PMP6000		Rev: A
Date: February 16, 2011		Drawn by: Josh Mandelcorn	
Engineer:	Filename: PMP6000_revA.sch	Sheet: 3 of 3	

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