Test Data
For PMP7848
8/17/2012

1 Power specification

Vin = 12V

Vout: VBL = -24V, VBH=-58V, VBP=+80V

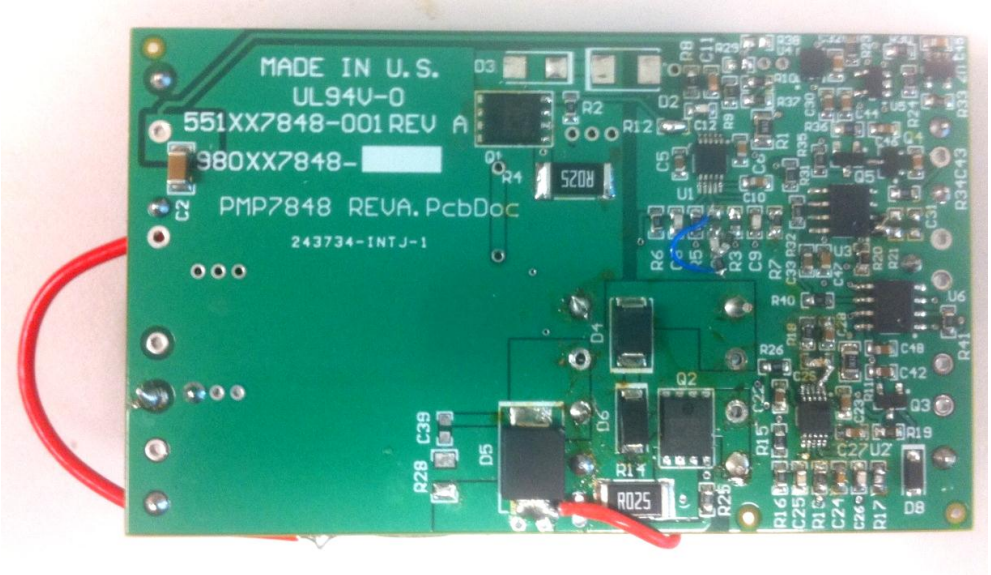
Iout_BL+ Iout_BH =0.7A

Iout_BP=0.4A

Fsw = 325kHz

1.1 Top Side

1.2 Bottom Side



2 Efficiency

2.1 Typical Full Load Test Condition:

	Input	VBL(-24V)	VBH(-58V)	VBP(+80V)
Voltage (V)	11.92	24.48	63.8	80.46
Current (mA)	1590	629.8	6.85	4.01
Power (W)	18.95	15.41	0.437	0.323

Under ambient temperature, no air flow

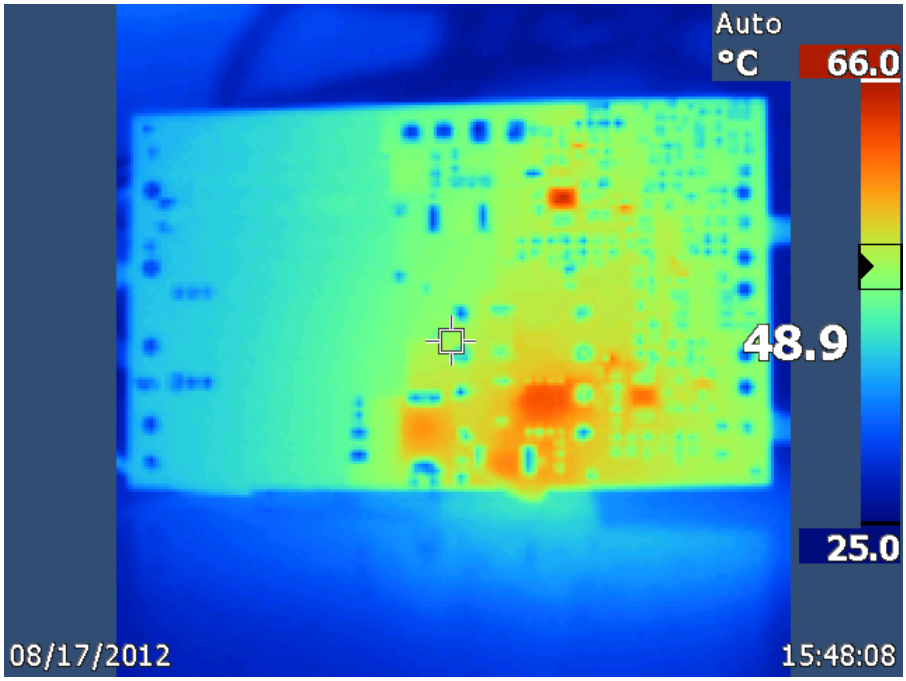
2.2 Efficiency Data:

Pin (W)	Pout (W)	Ploss (W)	Efficiency (%)
18.95	16.17	2.78	85.33%

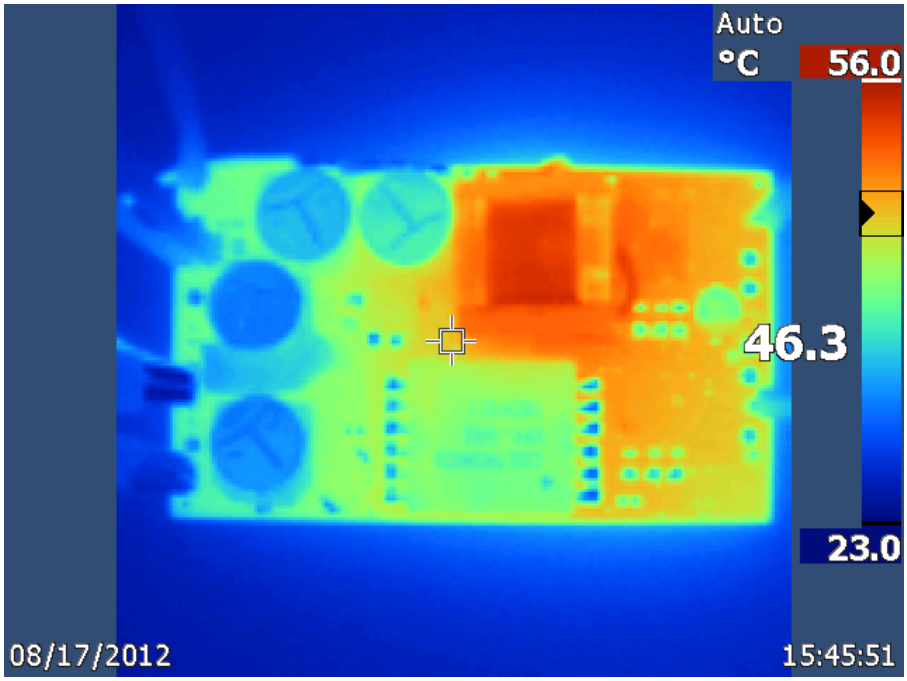
3 Thermal information

Under typical full load condition, ambient temperature, no air flow

3.1 Top side:



3.2 Bottom side:



4 Power Up Waveforms

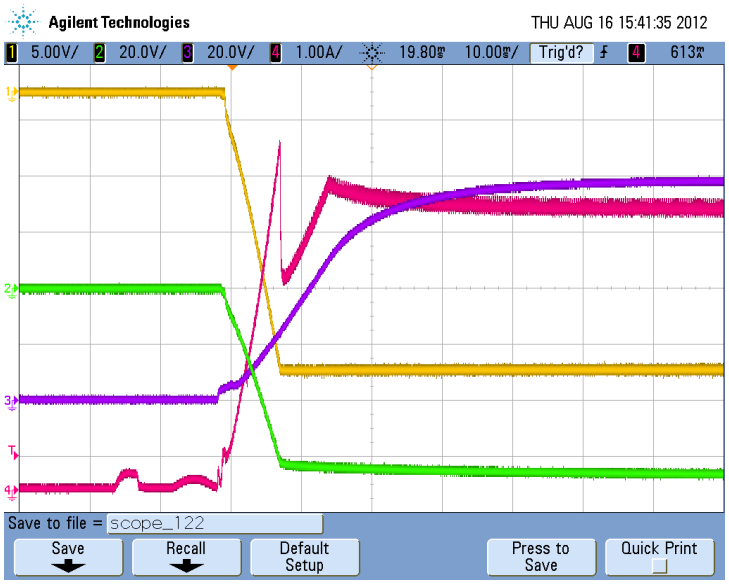
The rise time of VBP, VBH and VBL are all lower than 50ms

4.1 Start up to no load:

Ch1- VBL, Ch2-VBH, Ch3-VBP, Ch4-Input current

4.2 Start up to full load

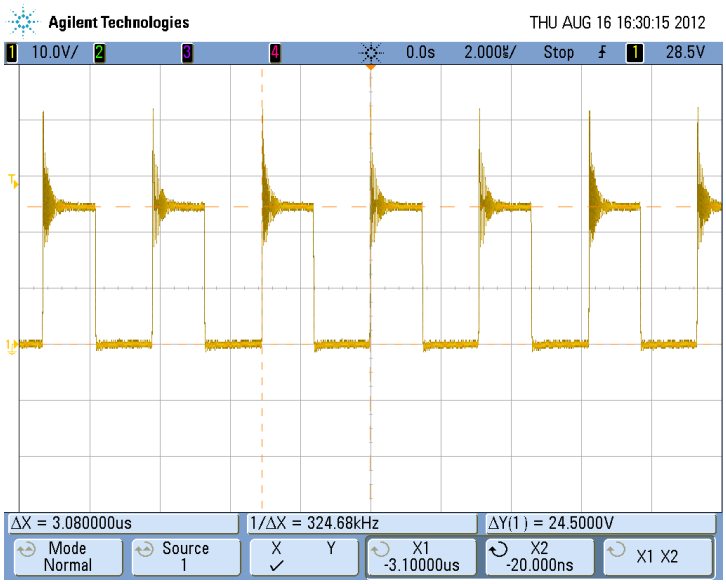
Iout_BL=0.7A, Iout_BH =0A, Iout_BP=0.4A
Ch1- VBL, Ch2-VBH, Ch3-VBP, Ch4-Input current



5 Switching Node Waveforms

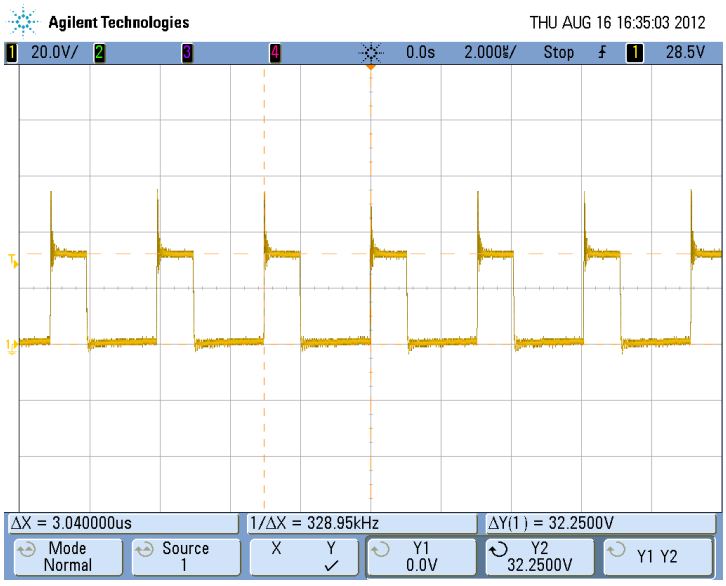
5.1 VBL full load switching

Iout_BL= 0.7A, Iout_BH= 0A
Ch1 – Vd_q2, Drain voltage of switch Q2



5.2 VBP full load switching

Iout_BP= 0.4A
Ch1 – Vd_q1 Drain voltage of switch Q1

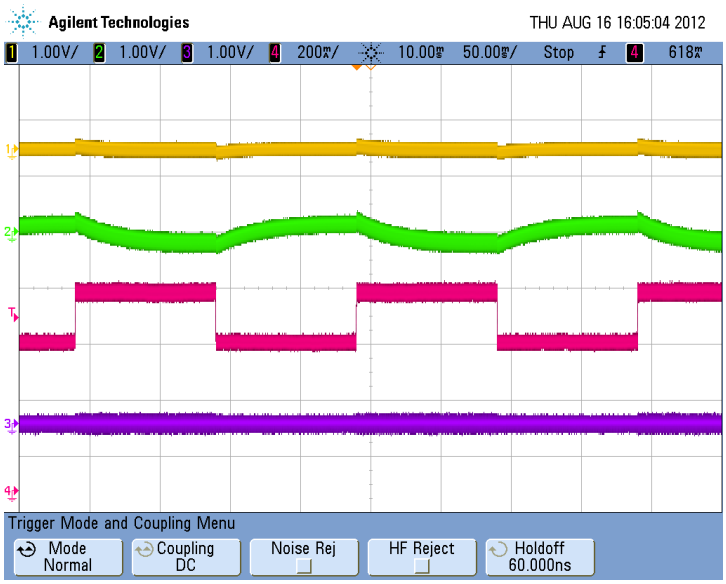


Load Transient and Cross Regulation Waveforms

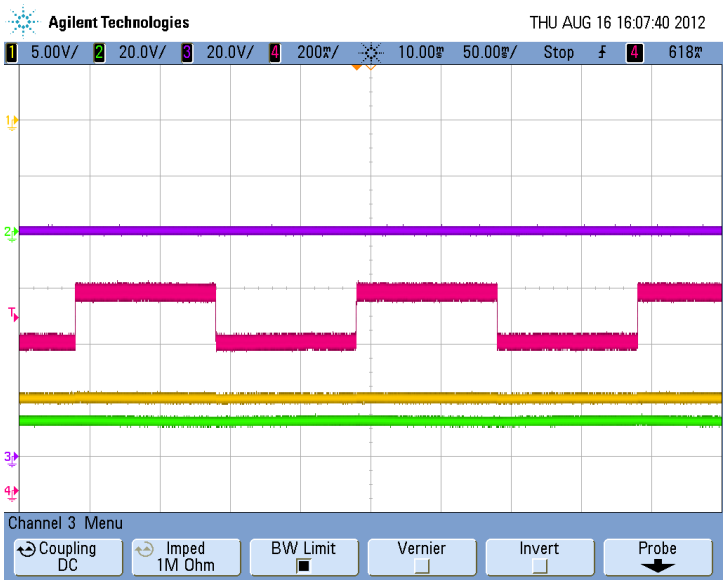
Test condition: Load steps from 75% to 100% load @ 0.5A/uS. Under load transient, the outputs' deviations are all within ±3%, and the settle time is within 15ms. The test waveforms also show that the load change on one output rail won't drive the other outputs out of their spec.

5.3 VBL load step

Iout_BL from 0.525A to 0.7A, with no load on other rails
Ch1- VBL (AC mode), Ch2-VBH (AC mode), Ch3-VBP (AC mode), Ch4- Iout_BL

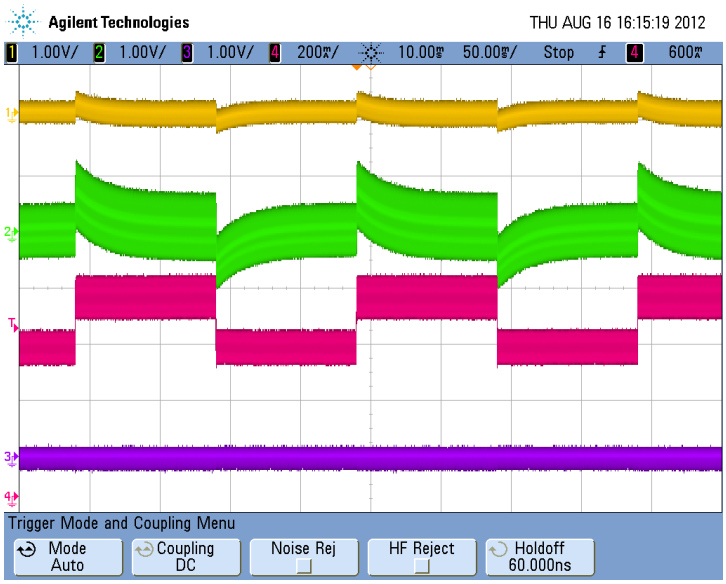


Ch1- VBL (DC mode), Ch2-VBH (DC mode), Ch3-VBP (DC mode), Ch4- Iout_BL

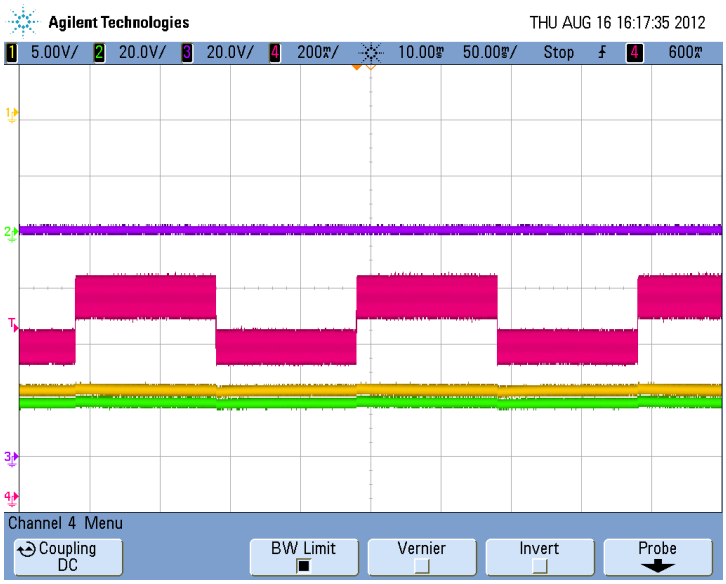


5.4 VBH load step

Iout_BH from 0.525A to 0.7A, with no load on other rails
Ch1- VBL (AC mode), Ch2-VBH (AC mode), Ch3-VBP (AC mode), Ch4- Iout_BH

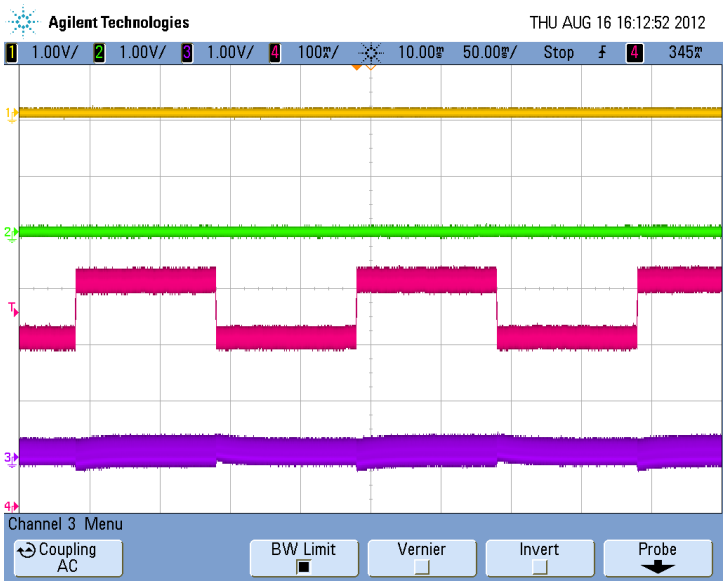


Ch1- VBL (DC mode), Ch2-VBH (DC mode), Ch3-VBP (DC mode), Ch4- Iout_BH

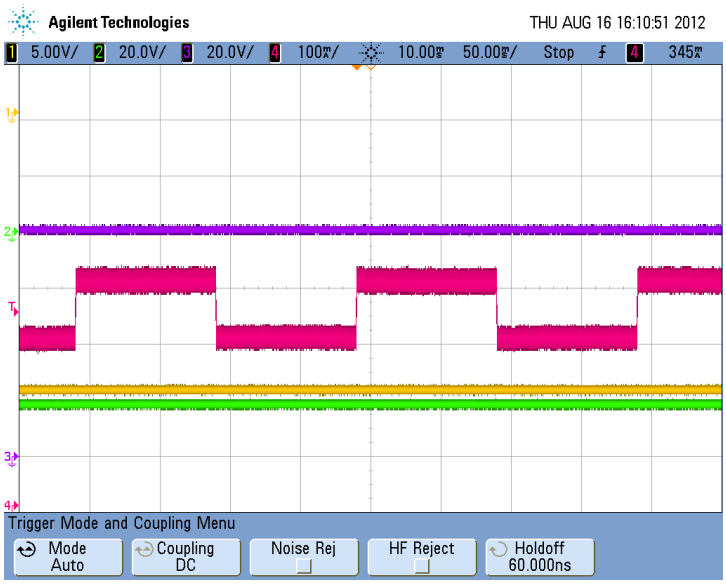

Agilent Technologies
THU AUG 16 16:17:35 2012
1 5.00V/ 2 20.0V/ 3 20.0V/ 4 200V/ 10.00s 50.00s/ Stop 4 600V
Channel 4 Menu
Coupling DC
BW Limit
Vernier
Invert
Probe

5.5 VBP load step

Iout_BP from 0.3A to 0.4A, with no load on other rails
Ch1- VBL (AC mode), Ch2-VBH (AC mode), Ch3-VBP (AC mode), Ch4- Iout_BP



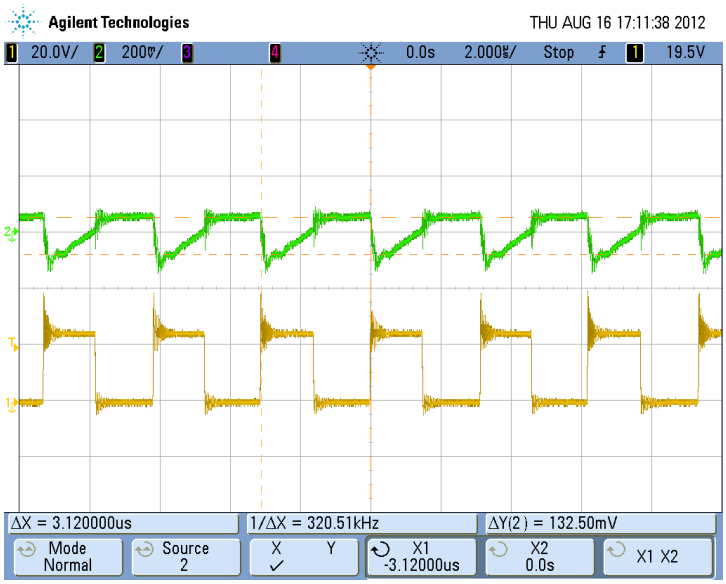
Ch1- VBL (DC mode), Ch2-VBH (DC mode), Ch3-VBP (DC mode), Ch4- Iout_BP



6 Output Voltage Ripple Waveforms

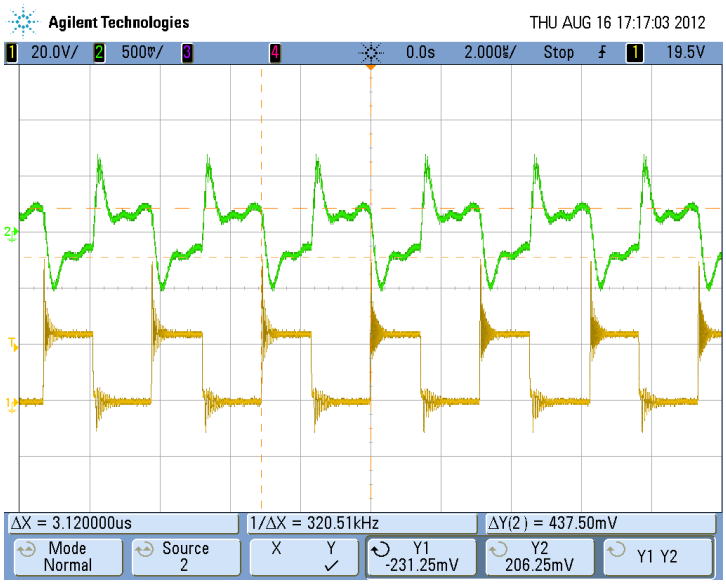
6.1 VBL ripple at full load out

Iout_BL=0.7A, Iout_BH=0A
Ch1- VBL (AC mode), Ch2- Vd_q2 Drain voltage of switch Q



6.2 VBH ripple at full load out

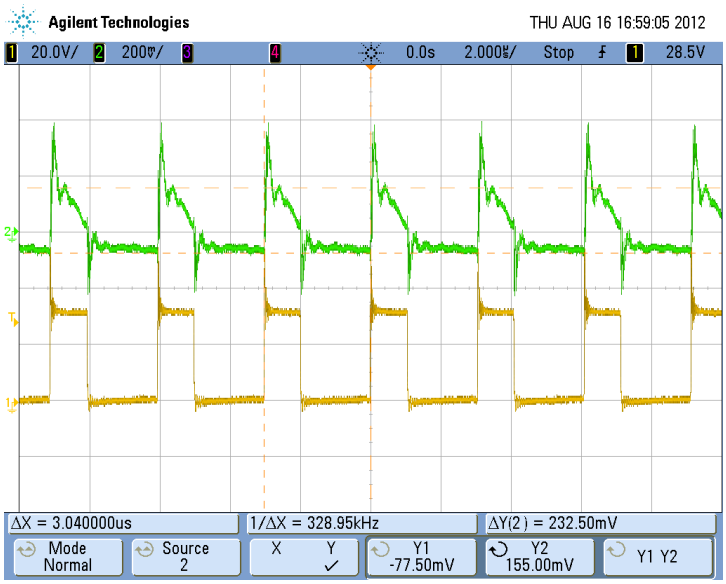
Iout_BL=0A, Iout_BH=0.7A
Ch1- VBH (AC mode), Ch2- Vd_q2 Drain voltage of switch Q2



6.3 VBP ripple at full load out

Iout_BP=0.4A

Ch1- VBP (AC mode), Ch2- Vd_q1 Drain voltage of switch Q1

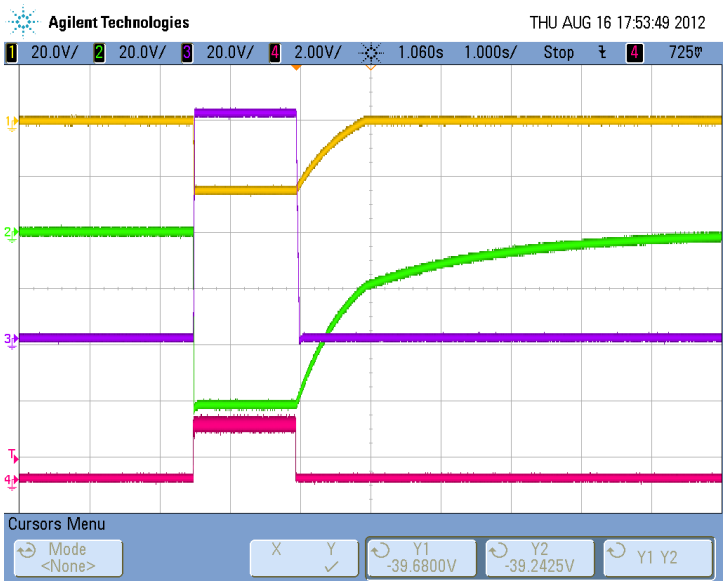


7 Remote ON/OFF Test

All outputs are shut down when remote pin is pulled down to ground.

7.1 Remote ON/OFF

Ch1- VBL, Ch2-VBH, Ch3-VBP, Ch4- Vremote

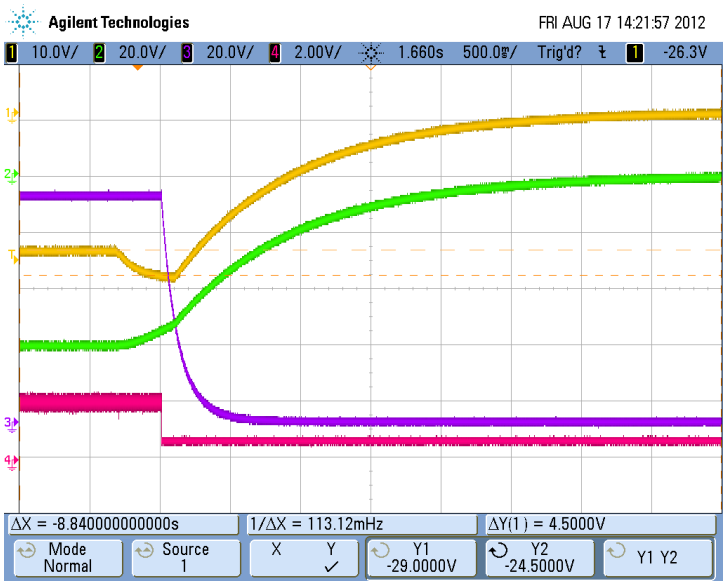


8 OVP Test

VBL is shortly jumped to -29V to trip the OVP condition. Once OVP occurs, Vremote is latched to 0.6V to disable all outputs.

8.1 OVP on VBL

Ch1- VBL, Ch2-VBH, Ch3-VBP, Ch4- Vremote

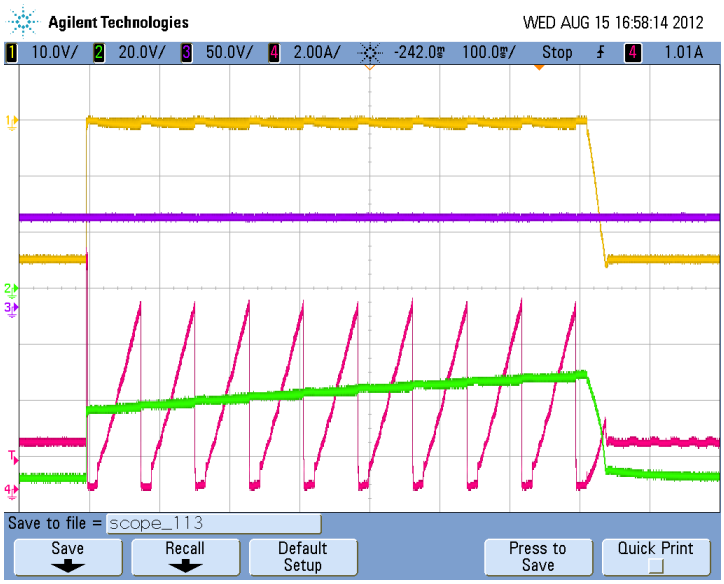


9 Short Circuit and OCP Test

Output VBL is shorted and then released during the test. Since there's no load on VBH, VBH is slowly dropping to 0V; VBP is not affected. The flyback converter for VBL and VBH is repeatedly trying to reboot during short, and the current limit set on the controller will prevent the input current going too high.

9.1 Short circuit on VBL

Ch1- VBL, Ch2-VBH, Ch3-VBP, Ch4- Input current

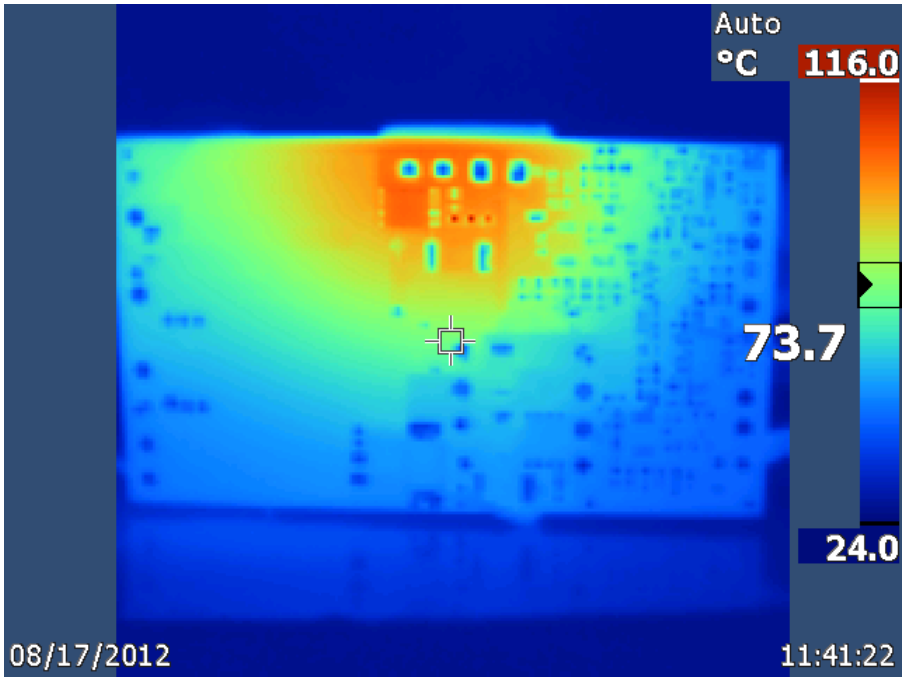


10 OTP Test

If the short circuit condition continues, the circuit will get heated and eventually enter OTP and shut down.

10.1 Bottom side thermal view in OTP

OTP is tripped when output VBP is shorted continuously



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