

miniPMU with 3 DC/DC Converters for Application Processors

Check for Samples: [TPS650380](#)

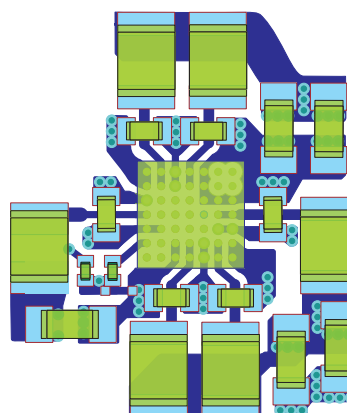
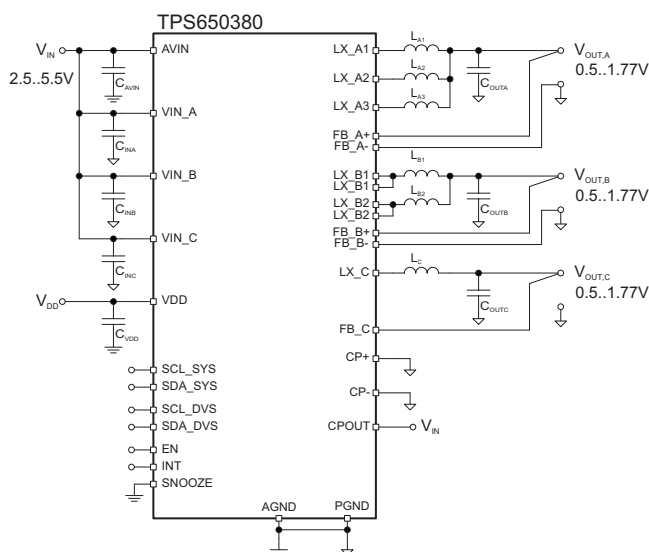
FEATURES

- **3 Step-Down Converters**
 - 3-Phase Step-Down Converter
 - 2-Phase Step-Down Converter
 - 1-Phase Step-Down Converter
- **Highest Efficiency:**
 - Reduced Inductor and On-Chip Losses by Multi Phase Design
 - Low $R_{DS,on}$ Switches and Active Rectifiers
 - Automatic Multi-to-Single Phase Operation Transition (Phase Shedding)
 - Power Save Mode for Light Load Efficiency
- **Two I²C High Speed Compatible Interfaces**
 - Digital Voltage Scaling
 - Monitoring, Software Control
- **Excellent DC and AC Output Voltage Regulation**
 - Differential Load Sensing
 - Precise DC Output Voltage Accuracy
 - Multiplied Regulation Bandwidth by Multi Phase Design
 - Reduced Output Voltage Ripple by Phase Shifted Operation
 - Low Battery Voltage Drop by Phase Shifted Operation

- **Multiple Dedicated Features:**
 - Soft Start
 - Power Good Indication
 - Programmable Slew Rate at Voltage Transition
 - Over Temperature Monitoring and Protection with Multiple Thresholds
 - Input Under Voltage Detection and Lockout
 - Output Current Limit and Protection
 - Interrupt Signal for Exception Handling
 - Built-in, programmable Output Rail Sequencer
- Available in 49-Bump, 3.25 x 3.25 mm² NanoFree™ Package
- Low External Device Count: down to 65 mm² Solution Size

APPLICATIONS

- Application Processor, DSP, ASIC and FPGA power
- Dynamic Voltage Scale Compliant Processors and DSPs
- Industrial Application
- Infotainment and Telematics Applications
- Smart Phones, Tablets, Ultrabooks



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PRODUCT PREVIEW



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

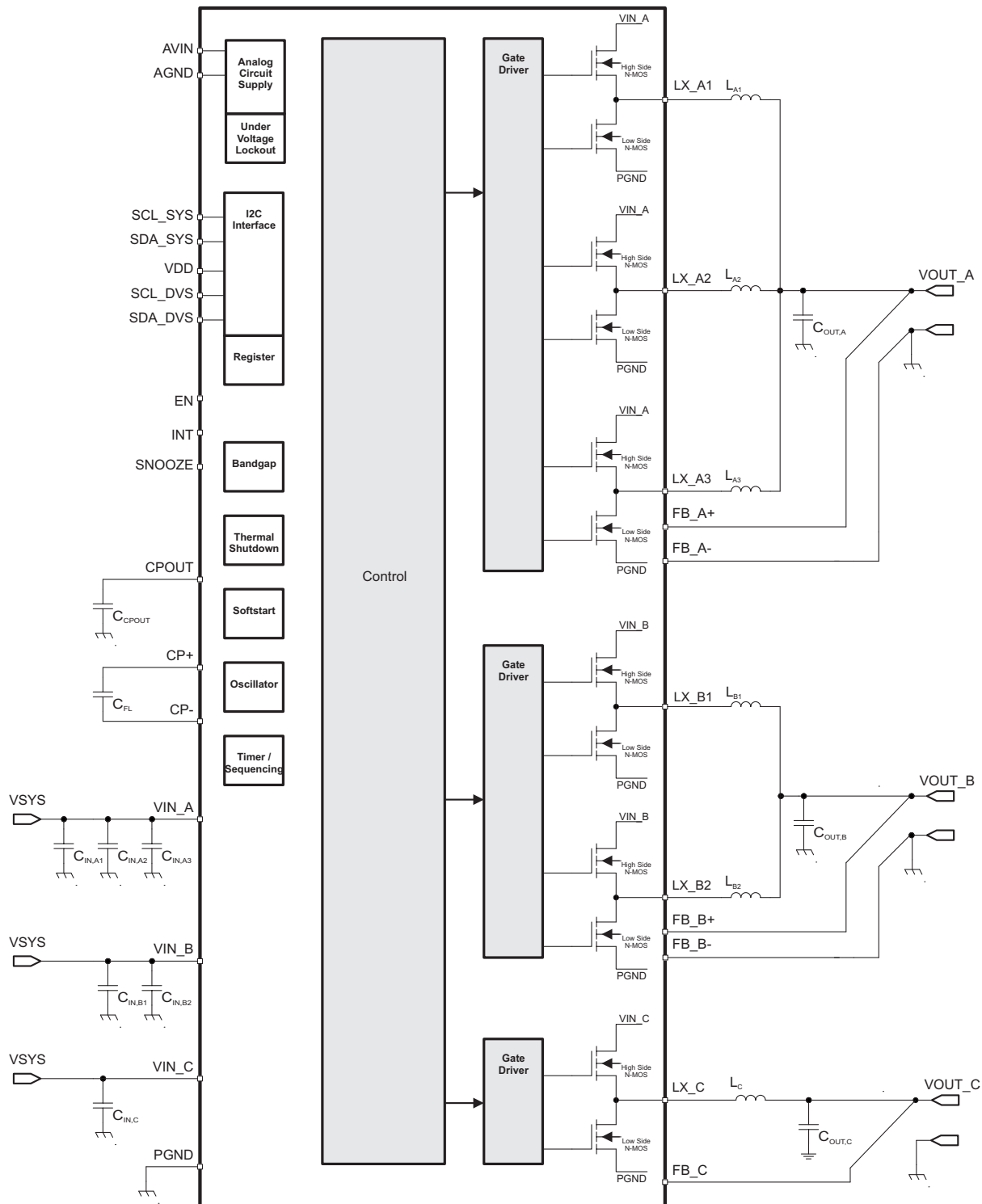


Figure 1. Block Diagram and Pin Functions

DESCRIPTION

The TPS650380 device is a high-frequency synchronous 3-rail mini PMIC solution for processors optimized for smallest solution size and battery-powered portable applications. With an input voltage range of 2.5V to 5.5V, 3.3V and 5V system rails as well as common and future battery technologies are supported.

The device's rails provide 6.8A / 3.7A / 1.8A load current, operating at 4MHz typical switching frequency to enable smallest inductors. The 6.8A rated rail is a 3-phase step down converter, the 2.9A rail is a 2-phase step down converter and the 1.5A rail operates as 1-phase step down converter.

All rails support an output voltage range of 0.5V to 1.77V. Programmable via I²C interface in 10mV steps, the TPS650380 supports low-voltage DSPs, ASICs, FPGAs and application processor including latest submicron processes and their retention modes, addressing digital voltage scaling technologies (DVS) such as Smart Reflex™. High efficiency conversion, accurate output voltage in the static and dynamic domain and a dedicated feature set address these applications.

Output Voltages and Modes can be fully programmed via I²C. Safe operation is supported by a comprehensive monitoring and exception handling feature set.

The 3.25 x 3.25 mm² package and the low number of required external components lead to a tiny solution size of approximately 65 mm².

OPERATION

High Efficiency Step Down Conversion

The device is equipped with a comprehensive set of built-in features to support high efficiency conversion over the complete output current and input voltage range. At highest output currents, the multi-phase rails operate in parallel. Thereby, the effective $R_{DS,ON}$ is significantly reduced leading to lowest on-chip losses. In addition, the external inductor losses are significantly lowered with an effective DCR being divided by 2 for the 2-phase rail (DCDC_B) and being divided by 3 for the 3-phase rail (DCDC_A). By reducing the on-chip and inductor losses, not only is efficiency improved; the device and PCB are kept cooler by reducing on-chip and external losses.

In order to maintain high efficiency conversion, the multi-phase rails automatically transition to single phase operation when required to maintain high efficiency conversion at medium load currents (phase shedding).

As the load current decreases further, the converter enters Power Save Mode to sustain high efficiency down to light loads. The transition from PWM to Power Save Mode is seamless and avoids output voltage transients.

Static Output Voltage Accuracy

The TPS650380 regulates the output voltage with a high accuracy voltage mode control. For the 3-phase (DCDC_A) and 2-phase (DCDC_B) rails, differential output voltage sensing (remote sense) is embedded which measures the output voltage at the point of load. With the differential and remote sensing, the TPS650380 compensates supply rail and ground shifts caused by non-ideal PCB traces.

The 1-phase output (DCDC_C) uses single-ended output voltage sensing due to its lower output current.

The multi-phase architecture reduces input and output voltage ripple to a minimum by operating the phases with a constant phase shift of 180° for the 2-phase rail and 120° for the 3-phase rail. A high precision clock keeps the phase shift constant while the duty cycle is altered to distribute the current equally to all phases (phase balancing).

Dynamic Output Voltage Accuracy

The current consumption profile of processors can be volatile due to sudden load changes which are caused by power gating, clock changes, etc. The TPS650380 addresses the sudden load changes by nearly instantaneously adjusting the output voltage to keep it in regulation. The multi-phase architecture helps further with a increased effective regulation bandwidth.

APPLICATION SPECIFIC FEATURES

The TPS650380 is equipped with application specific features. These features are accessible by software via I²C interface resulting in highest flexibility.

- The built-in, programmable output rail sequencer combined with a fast output rail start-up time allows precise sequencing of the output rail.
- The output voltage can be programmed with 10mV steps. A transition between different voltage levels is performed with a controlled, linear output voltage ramp. The slew rates can be programmed to both match timing requirements and provide predictability.
- An all integrated feature set to enable safe, most reliable operation and easy system integration addresses application specific requirements. These features can be controlled and monitored by I²C. In addition, a dedicated pin for exception handling is provided. The feature list includes output current monitoring with programmable electronic fuse, temperature monitoring / protection and individual power good indication for each output.

PACKAGE SUMMARY

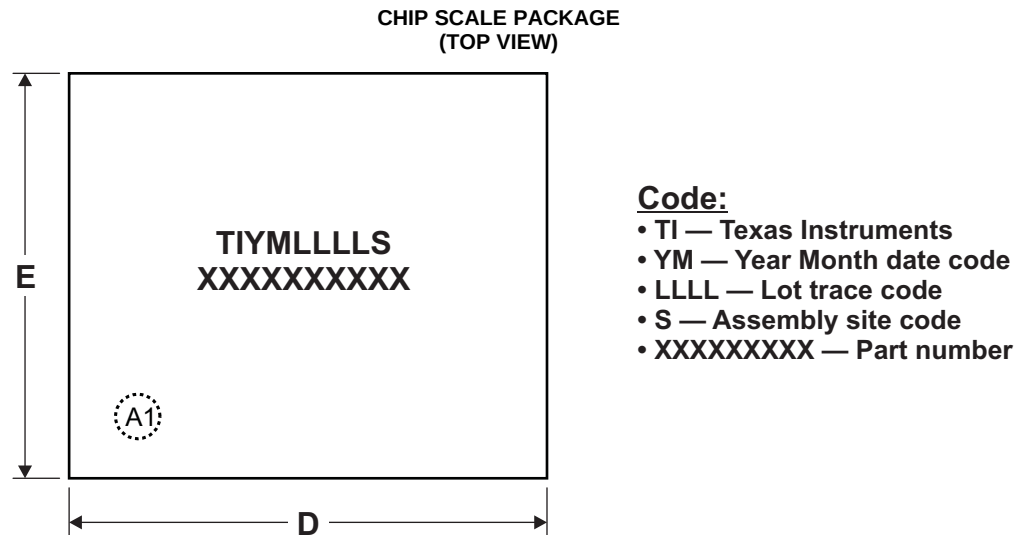


Figure 2. Package Marking and Dimensions

Package Marking

Table 1. Package Marking

Device	Marking
TPS650380	TPS650380

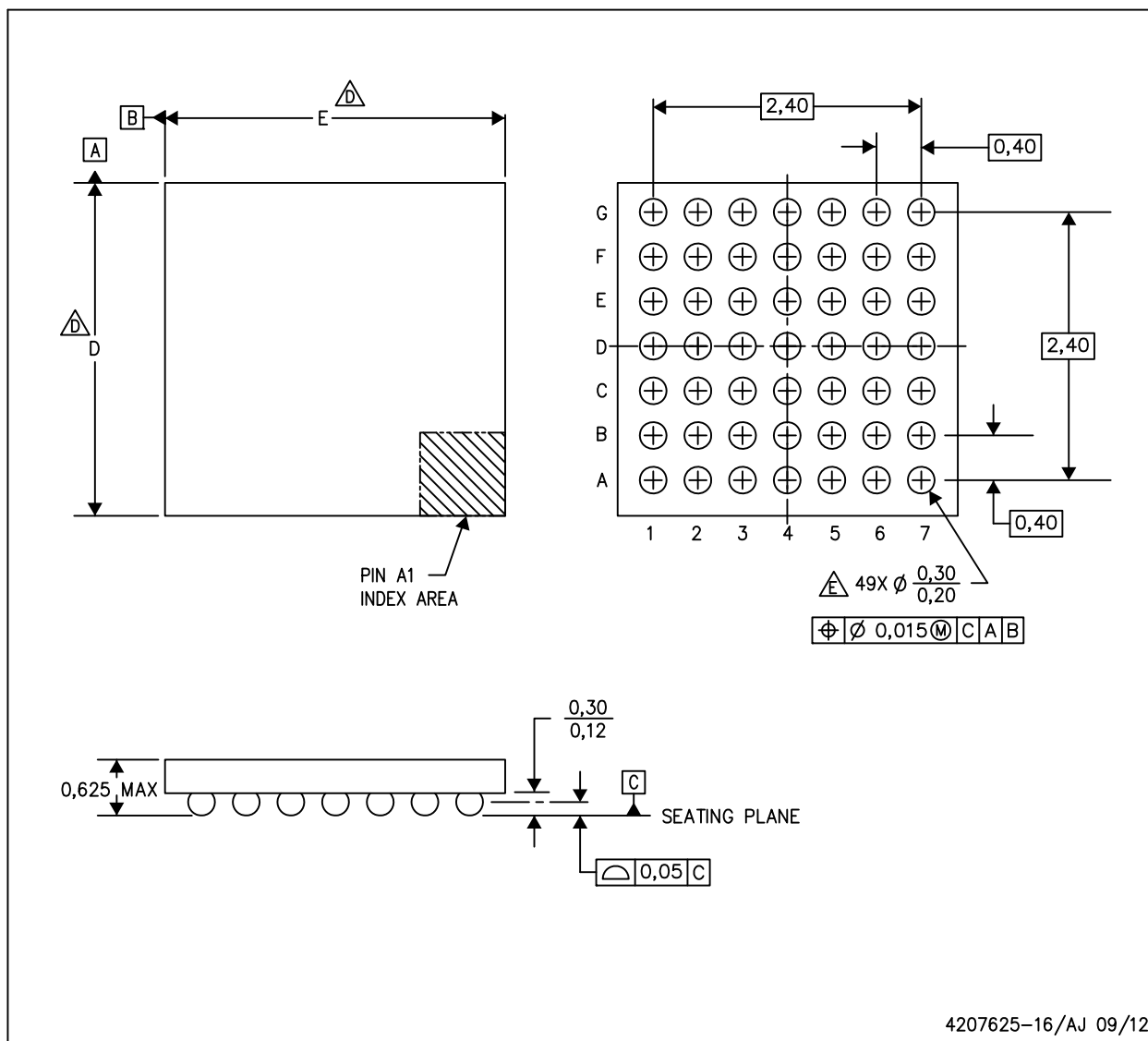
Chip Scale Package Dimensions

The TPS650380 devices are available in a 49-bump chip scale package (YFF, NanoFree™). The package dimensions are given as:

- D = 3.25mm (+/- 0.03mm)
- E = 3.25mm (+/- 0.03mm)

YFF (R-XBGA-N49)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - $\triangle$ The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
7 x 7 matrix pattern is shown for illustration only.
 - F. This package contains Pb-free balls.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS650380YFFR	PREVIEW	DSBGA	YFF	49		TBD	Call TI	Call TI	-40 to 85		
TPS650380YFFT	PREVIEW	DSBGA	YFF	49		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

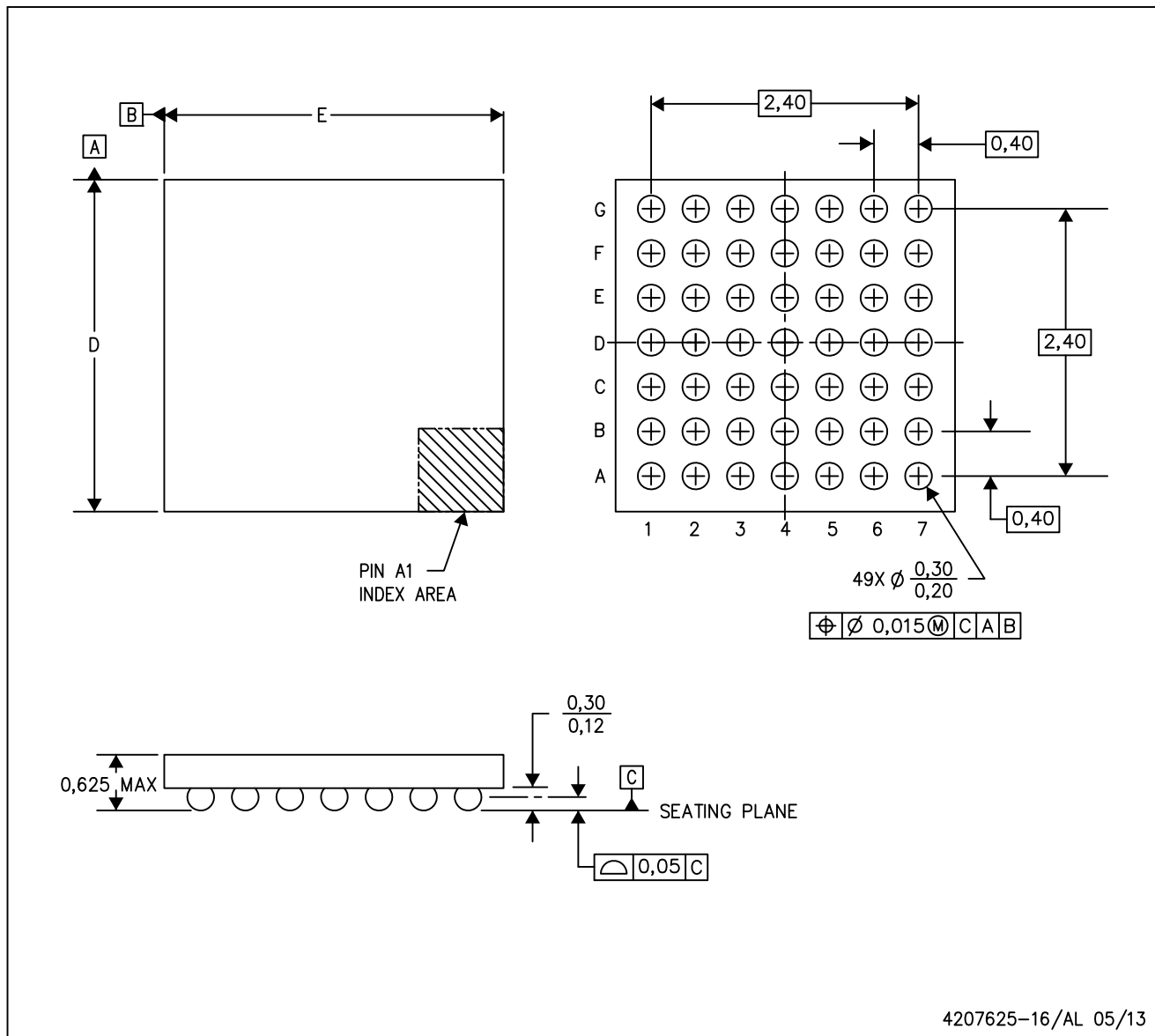
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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YFF (R-XBGA-N49)

DIE-SIZE BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.
 C. NanoFree™ package configuration.

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