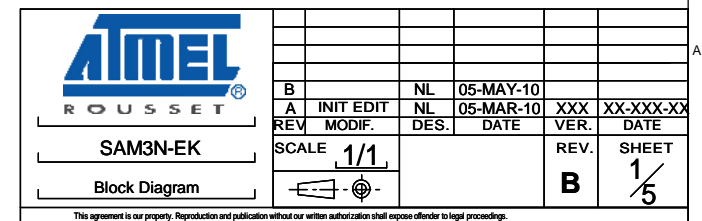
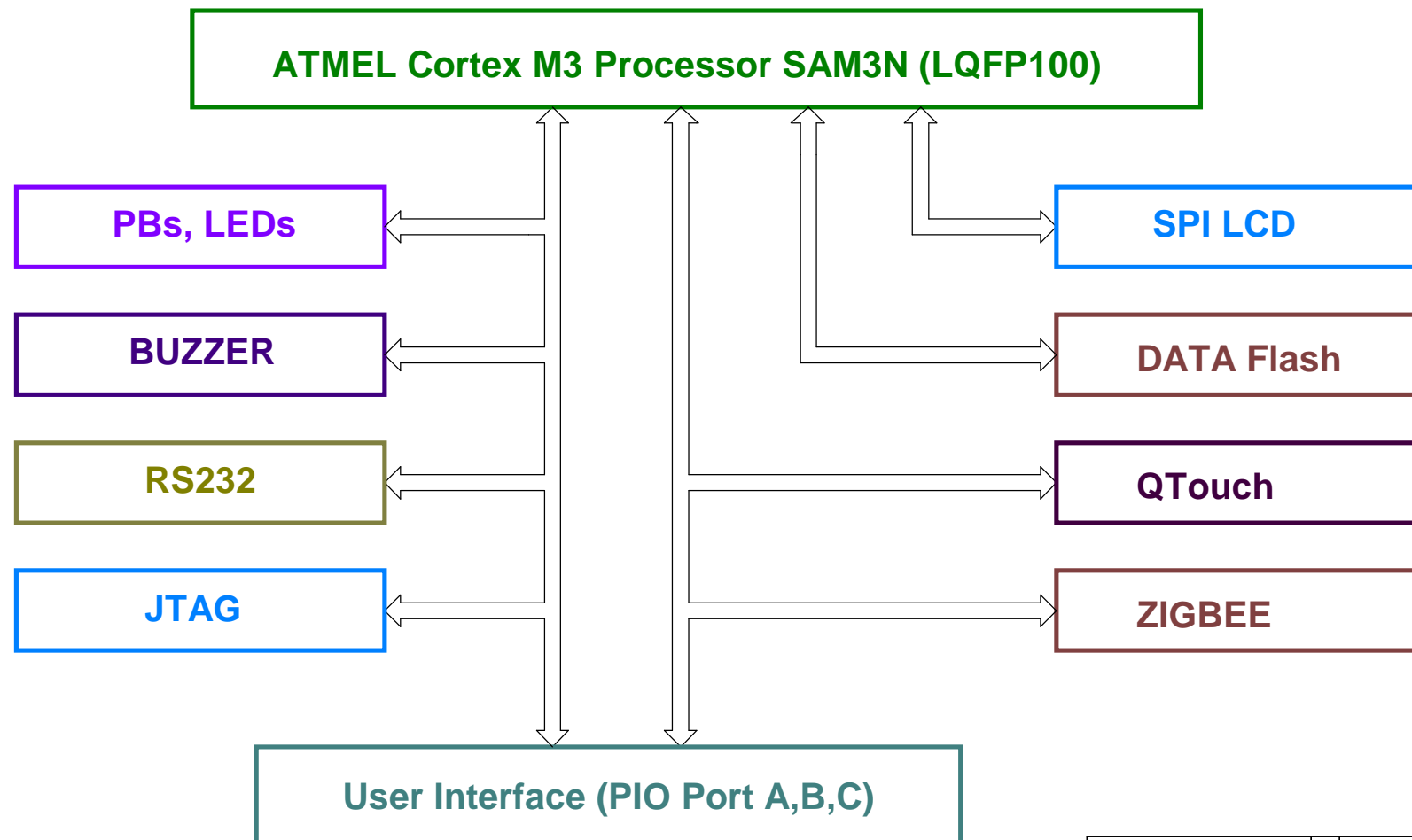


SAM3N-EK RevA Block Diagram



REVISION HISTORY

REV	DATA	NOTE
A	2010.03.04	ORIGINAL RELEASED

SCHEMATICS CONVENTIONS

(1) Resistance Unit: "K" is "Kohm", "R" is "Ohm"?
(2) "DNP" means the component is not populated by default

JUMPER and SOLDERDROP

PAGE	REFERENCE	DEFAULT	FUNCTION
3	JP1	DNP	Close to select JTAG boundary scan
	JP2	1-2	Analog reference voltage selection between 3.3V and 3V, default 3.3V
	JP3	OPEN	ERASE, Close to reinitialize the Flash contents and some of its NVM bits
	JP4	CLOSE	Access for current measurement on VDDIO
	JP5	CLOSE	Access for current measurement on VDDIN
	JP6	CLOSE	Access for current measurement on VDDPLL
	JP7	CLOSE	Access for current measurement on VDDCORE
5	JP8 JP9	1-2	DC voltage selection between 3.3V and 5V on PIO expansion ports, default for 3.3V

TABLE OF CONTENTS

PAGE	DESCRIPTION
1	Block Diagram
2	Reference guide
3	Microcontroller, Power
4	Data Flash, Micro SD, LCD, BL Driver, JTAG, RS232
5	IO Expansion, Buzzer, ZigBEE, LEDs, Buttons, QTouch

TEST POINT


PAGE	REFERENCE	FUNCTION
3	TP1	+5V
	TP2	+3V3
	TP3, TP4, TP5	GND
4	TP6 TP7	UTXD0 URXD0

PIO MUXING

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOC	USAGE	PIOC	USAGE
PA0	POWER LED	PA16	PB_USER2	PB0		PC0	QT_SL_SNS	PC16	
PA1	CMD_SOUND	PA17		PB1		PC1	QT_SL_SNSK	PC17	
PA2		PA18		PB2		PC2	QT_SM_SNS	PC18	
PA3		PA19	MicroSD_CD	PB3		PC3	QT_SM_SNSK	PC19	
PA4		PA20		PB4	JTAG	PC4	QT_SR_SNS	PC20	
PA5		PA21		PB5	JTAG	PC5	QT_SR_SNSK	PC21	
PA6		PA22	NPCS_DATAFLASH	PB6	JTAG	PC6		PC22	
PA7	XIN32	PA23	LED_BLUE	PB7	JTAG	PC7		PC23	ZB_RSTN
PA8	XOUT32 / ADTRG	PA24		PB8	XOUT_12M	PC8	QT1_SNS	PC24	ZB_IRQ0
PA9	RX_UART0	PA25	LED_AMBER	PB9	XIN_12M	PC9	QT1_SNSK	PC25	ZB_IRQ1
PA10	TX_UART0	PA26		PB10		PC10	QT2_SNS	PC26	ZB_SLPTR
PA11		PA27		PB11		PC11	QT2_SNSK	PC27	
PA12	SPI_MISO	PA28	RS_LCD	PB12	ERASE	PC12		PC28	
PA13	SPI_MOSI	PA29	RST_LCD	PB13		PC13	EN_LCD	PC29	
PA14	SPI_SPCK	PA30	NPCS_LCD	PB14	LED_GREEN	PC14		PC30	
PA15	PB_USER1	PA31	NPCS_ZigBee			PC15		PC31	

DEFAULT NO POPULATE PARTS

PAGE	REFERENCE	FUNCTION
3	Y1, R1, R7	External clock resource input
	JP1	Option access for JTAGSEL
	R6, R8	Isolation between 12MHz clock source and GPIO line
	R4, R9	Isolation between 32KHz clock source and GPIO line
5	S1, K1, K2	QTouch PADs, not real part



INT EDIT

REV

SCALE

Describe

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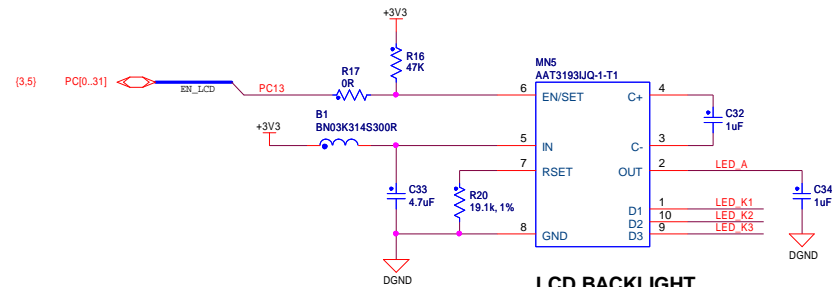
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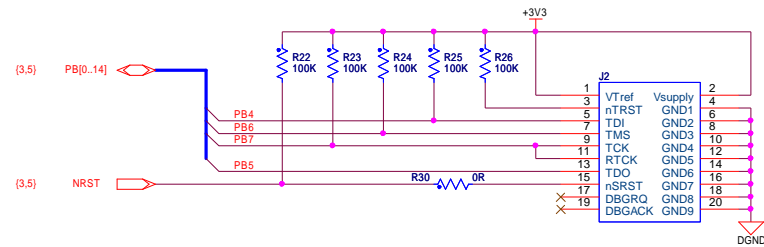
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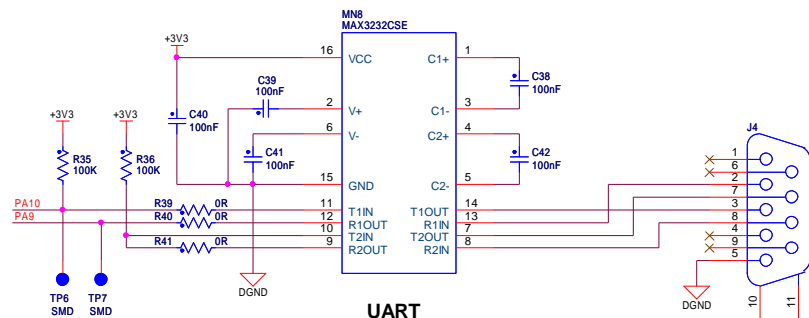
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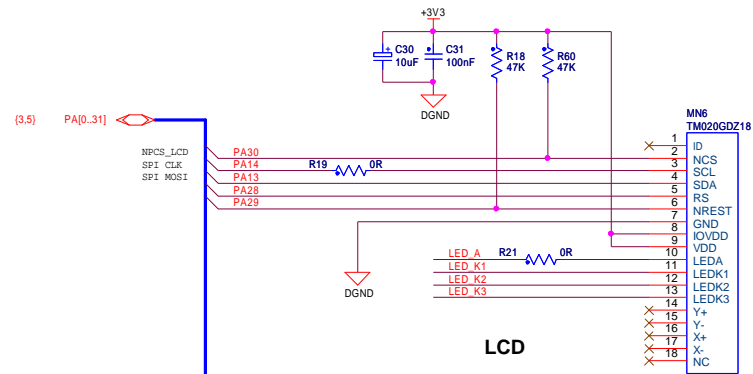
LCD BACKLIGHT



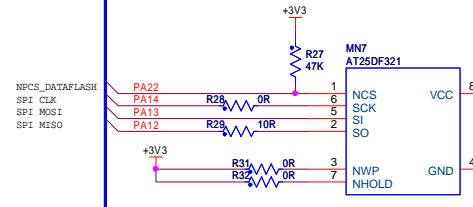
ICE INTERFACE



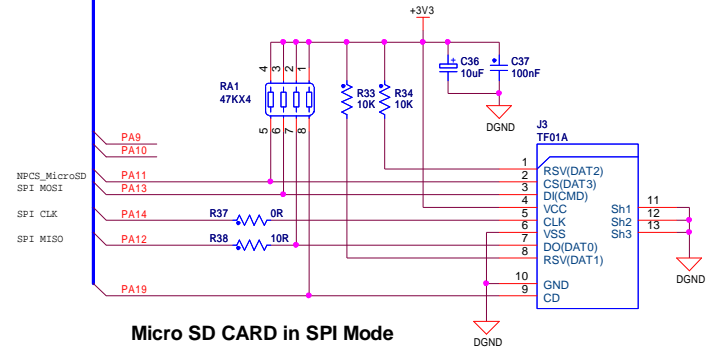
UART



LCD



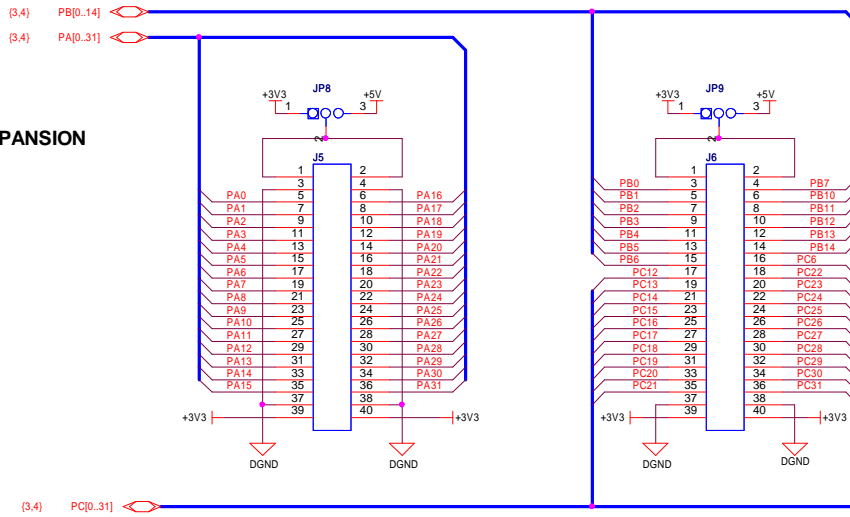
DATA FLASH



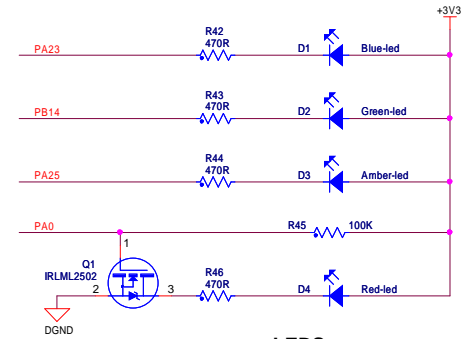
Micro SD CARD in SPI Mode

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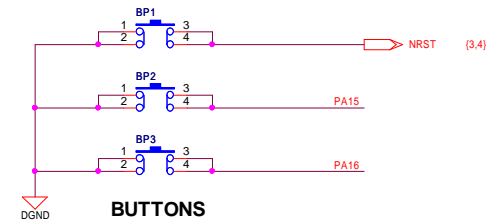
PIO EXPANSION



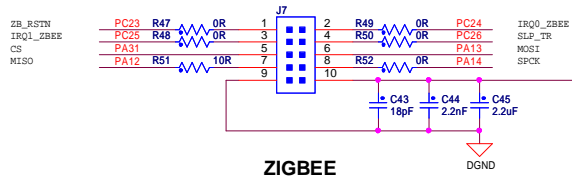
LEDS



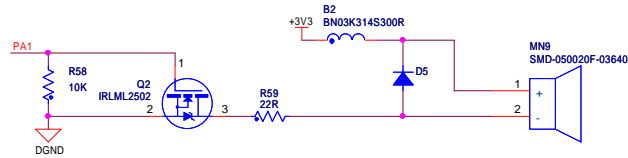
BUTTONS



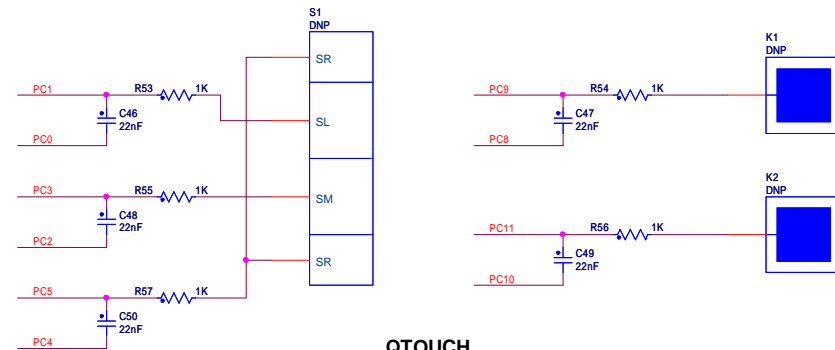
ZIGBEE





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