Tim Green

TI Precision Designs: Reference Design
AC Coupled Single Supply Comparator

TI Precision Designs

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Circuit Description

Sometimes a single supply comparator is required to use ac coupling to detect sine waves or square waves. Often this is needed due to differences in ground potential between two different modules. Whenever ac coupling is involved in single supply circuitry, negative voltages become a concern. Excessive negative voltages on comparators can cause the comparator to trip erroneously or to become stuck at unpredictable levels. Proper high pass filtering and dc offsetting are required for reliable operation. This design will show how to ac couple a wide range of input signal levels and frequencies into a high speed comparator to generate a robust and accurate clock signal.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
TLV3501	Product Folder

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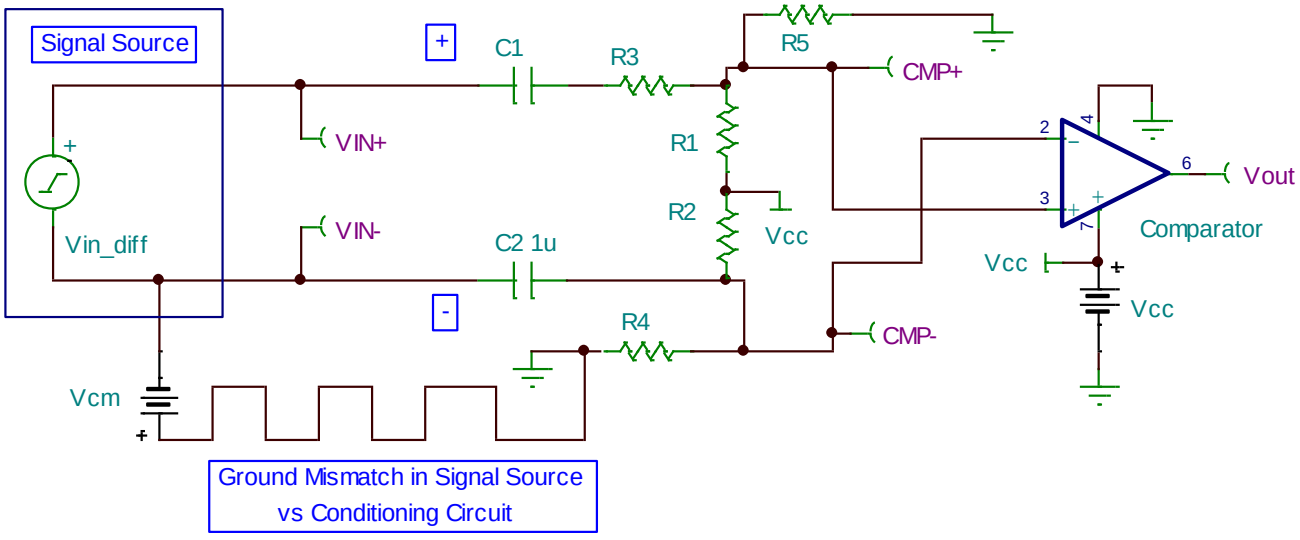


1 Design Summary

The design requirements are as follows:

- No Input Signal → Comparator Output = 0V
- Start-up Time < 1ms
- Supply Voltage: 3.3V, ±5% (3.135V to 3.465V)
- Input Signal Source Supplies:
  - Vcc = 3.3V, ±5% (3.135V to 3.465V)
  - Vcc = 5V, ±5%, (4.75V to 5.25V)
- Input Signal Levels:
  - VIL = GND+400mV @ Isink = 2mA
  - VIH = Vcc-400mV @ Isource = 2mA
  - Common Mode Range: ±100mV
- Propagation Delay: <5ns
- Duty Cycle Change from Input to Output: <10%
- Frequency Requirements – See Table 1

Table 1. Input Signal Frequency Requirements

Frequency	Min VIL	Max VIL	Min VIH	Max VIH	Vcm	Duty Cycle
2kHz	0V	400mV	+2.7V / +4.35V	+3.5V / +5.25V	+/-100mV	40% to 60%
32MHz	0V	400mV	+2.7V / +4.35V	+3.5V / +5.25V	+/-100mV	40% to 60%

Frequency	Period	Duty Cycle	t_{ON}
2kHz	500us	40%	200us
2kHz	500us	60%	300us
32MHz	31.25ns	40%	12.5ns
32MHz	31.25ns	60%	18.75ns

The design goals and performance are summarized in Table . Figure 1 depicts the simulated typical transient response of the design.

Table 2. Comparison of Design Goals and Simulated Performance

	Goal	Simulated
No Input Signal	Vout=0V	Vout=282pV
Start-up Time	<1ms	672us

Worst Case Test Case	Input Frequency	Input VIL	Input VIH	Input VCM	Input Duty Cycle	Comparator Vcc	Simulated Vout Duty Cycle	Simulated Delay
1	2kHz	0V	5.25V	+100mV	40%	3.135V	40%	0ns
2	2kHz	400mV	2.7V	+100mV	40%	3.135V	40%	0ns
3	2kHz	0V	5.25V	-100mV	40%	3.135V	40%	0ns
4	2kHz	400mV	2.7V	-100mV	40%	3.135V	40%	0ns
5	32MHz	0V	5.25V	+100mV	40%	3.135V	57%	3.6ns
6	32MHz	400mV	2.7V	+100mV	40%	3.135V	52%	3.6ns
7	32MHz	0V	5.25V	-100mV	40%	3.135V	57%	3.6ns
8	32MHz	400mV	2.7V	-100mV	40%	3.135V	51%	3.6ns

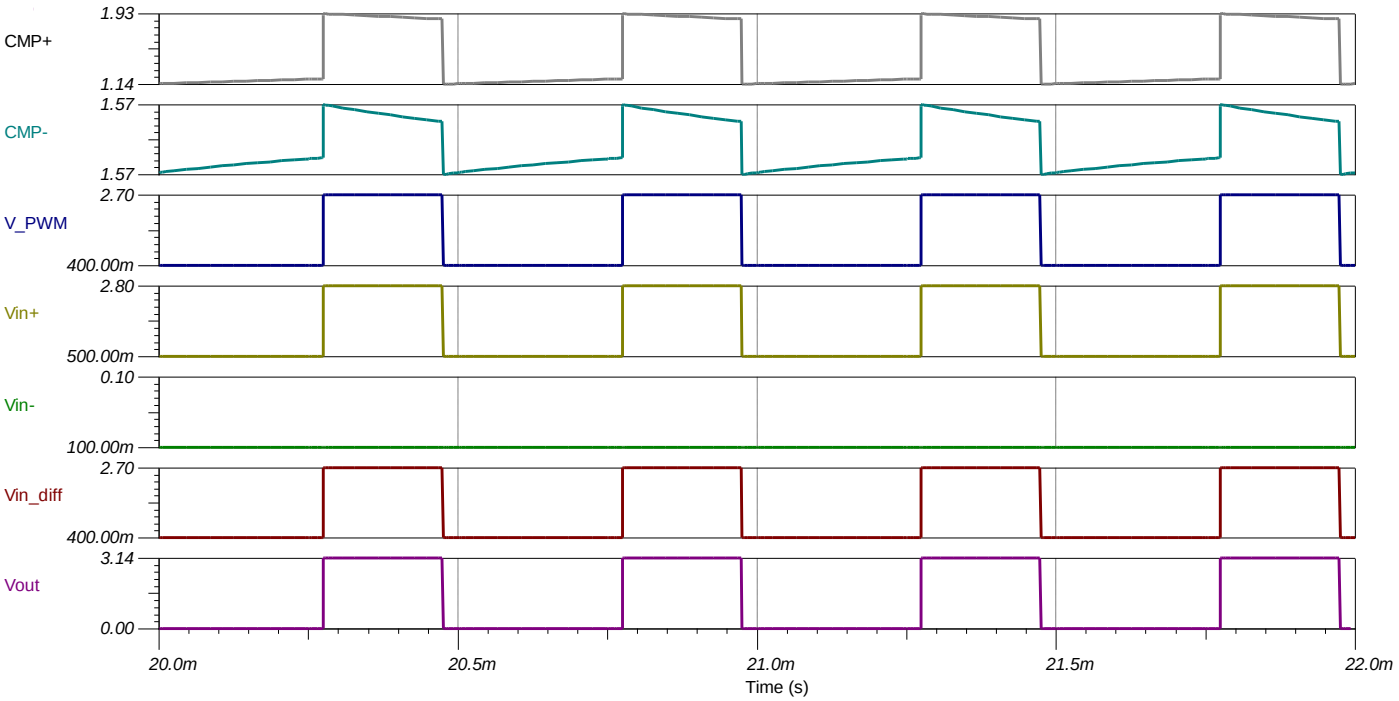


Figure 1: Simulated Typical Transient Response

2 Theory of Operation

The “AC Coupled Single Supply Comparator” circuit design provides a way to ignore ground differences between modules and to accommodate a wide range of both frequencies and amplitudes into a high speed comparator, resulting in a robust and accurate clock signal. Refer to Figure 2. C1 and C2 provide the ac coupling of the input signal Vin. R2 and R4 provide a dc offset of mid-supply for CMP-. R1 and R5 provide a dc offset of about 100mV less than mid-supply into CMP+. The differences in dc offset between CMP- and CMP+ ensure that, for no input signal, Vout will be at the comparator output low voltage (near zero volts). The dc offset on each input is necessary to counteract the negative voltages that will occur on these inputs due to ac coupling of Vin. R3 provides a way to divide the ac coupled input signal down in amplitude to be less than the common mode voltage of the comparator used. The input scaling resistors combined with the comparator input capacitance form a low pass input filter and attenuate the ac coupled signal into the comparator. For this reason it is desired to keep the resistor values as low as practical. The high pass cut-off frequency of the input signal conditioning can be viewed as a simple C-R high pass with C = C1||C2 and R = 1.964k (equivalent input resistance seen across the ends of C1 and C2 connected to CMP+ and CMP- through scaling resistors, R1, R2, R3, R4, R5).

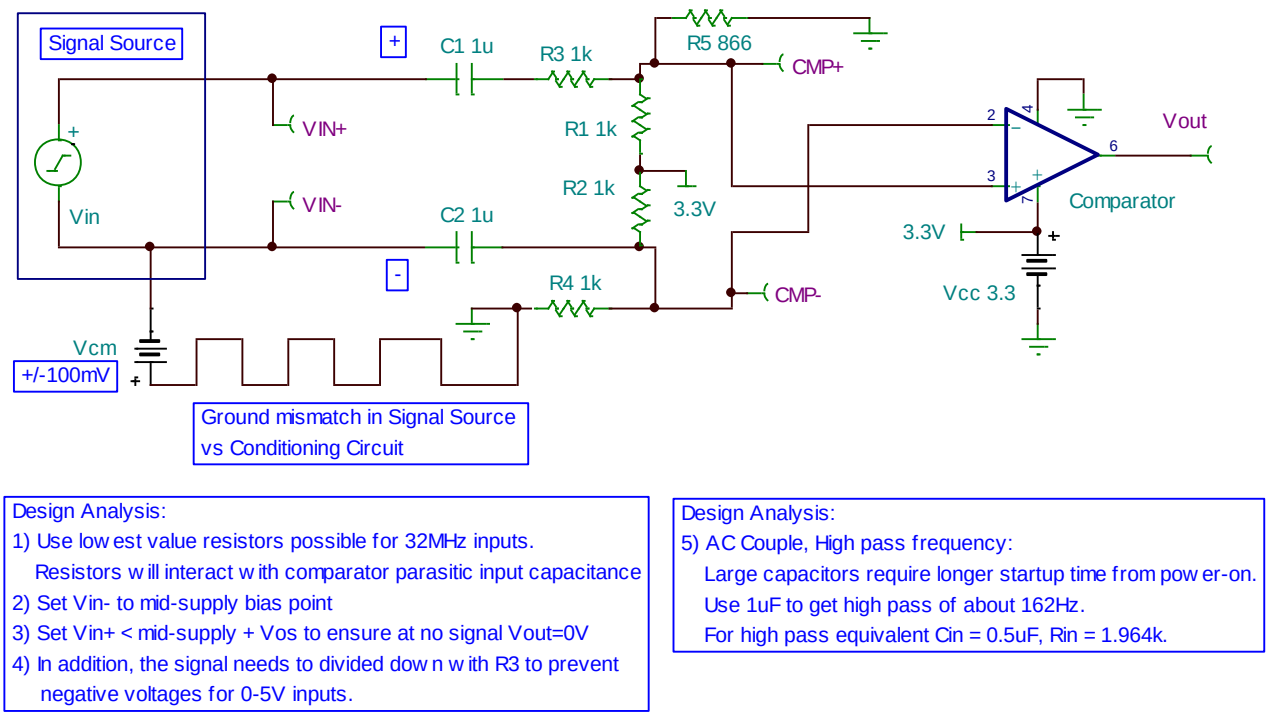


Figure 2: Complete Circuit Schematic

3 Component Selection

3.1 Comparator Selection

From Table 1 we see the minimum t_{ON} of 12.5ns is at 32MHz, 40% duty cycle. If our comparator has a propagation delay any longer than 12.5ns we will not detect a 32MHz signal of 40% duty cycle.

Table 3 highlights the key comparator specifications as single supply (2.5V to 3.5V), rail-to-rail input and propagation delay less than or equal to 12.5ns based on the maximum input frequency of 32MHz with a 40% duty cycle. The TLV3501 meets all of these criteria.

Table 3. Comparator Specifications

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, T_A = **−40°C to +125°C.**

At T_A = +25°C and V_S = +2.7V to +5.5V, unless otherwise noted.

PARAMETER		CONDITION	TLV3501, TLV3502 MIN	TLV3501, TLV3502 TYP	TLV3501, TLV3502 MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage(1)	V_{OS}	V_{CM} = 0V, I_O = 0mA		±1	±6.5	mV
vs Temperature	**dV_{OS}/dT**	**T_A = −40°C to +125°C**		±5		**µV/°C**
vs Power Supply	PSRR	V_S = 2.7V to 5.5V		100	400	µV/V
Input Hysteresis				6		mV
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = V_{CC}/2		±2	±10	pA
Input Offset Current(2)	I_{OS}	V_{CM} = V_{CC}/2		±2	±10	pA
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) − 0.2V		(V+) + 0.2V	V
Common-Mode Rejection	CMRR	V_{CM} = −0.2V to (V+) + 0.2V	57	70		dB
		V_{CM} = −0.2V to (V+) + 0.2V	**55**			**dB**
INPUT IMPEDANCE						
Common-Mode				10^{13} ||2		Ω ||pF
Differential				10^{13} ||4		Ω ||pF
SWITCHING CHARACTERISTICS						
Propagation Delay Time(3)	$T_{(pd)}$	ΔV_{IN} = 100mV, Overdrive = 20mV		4.5	6.4	ns
		ΔV_{IN} = 100mV, Overdrive = 20mV			**7**	**ns**
		ΔV_{IN} = 100mV, Overdrive = 5mV		7.5	10	ns
		ΔV_{IN} = 100mV, Overdrive = 5mV			**12**	**ns**
Propagation Delay Skew(4)	$\Delta t_{(SKEW)}$	ΔV_{IN} = 100mV, Overdrive = 20mV		0.5		ns
Maximum Toggle Frequency	f_{MAX}	Overdrive = 50mV, V_S = 5V		80		MHz
Rise Time(5)	t_R			1.5		ns
Fall Time(5)	t_F			1.5		ns
OUTPUT						
Voltage Output from Rail	V_{OH},V_{OL}	I_{OUT} = ±1mA		30	50	mV

3.2 Comparator Input Capacitance and Low Pass Frequency

Figure 3 is the equivalent input impedance of the TLV3501 comparator. Through series and parallel combination of the input capacitances we can arrive at the total equivalent differential input capacitance, Cin_eq, of 5pF.

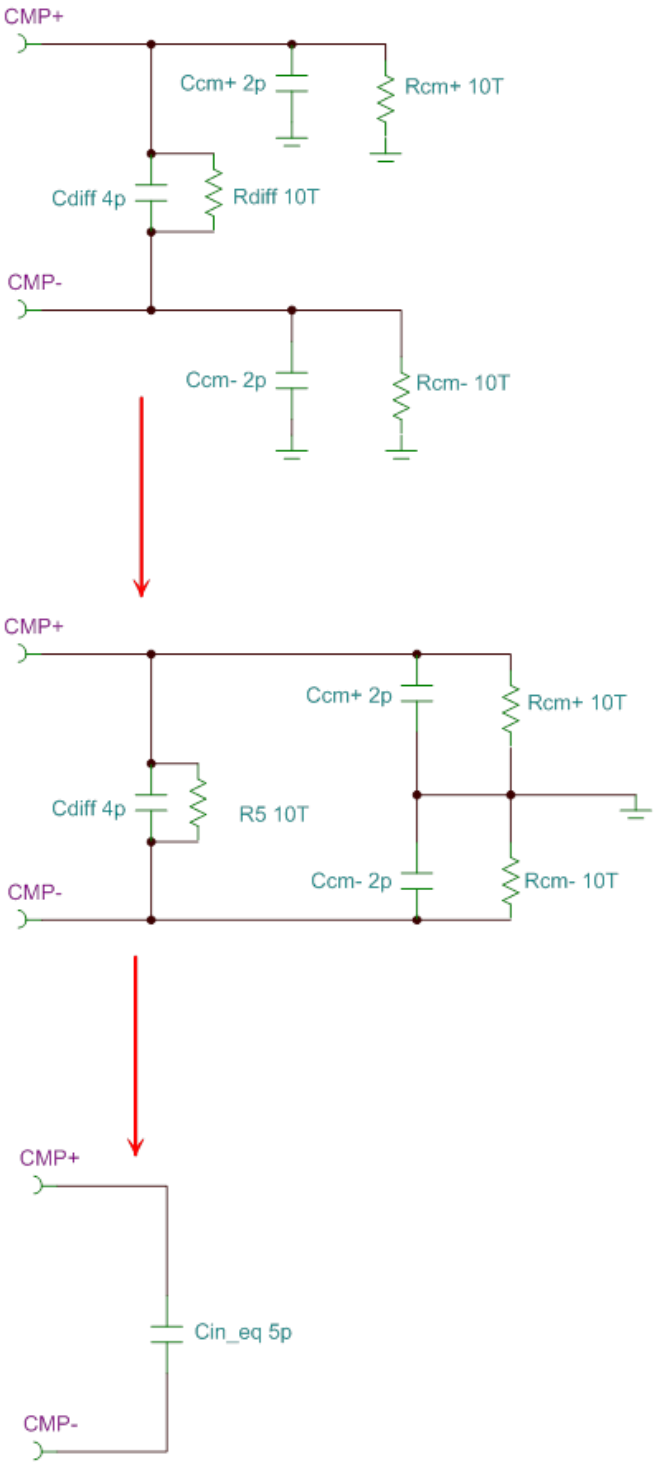
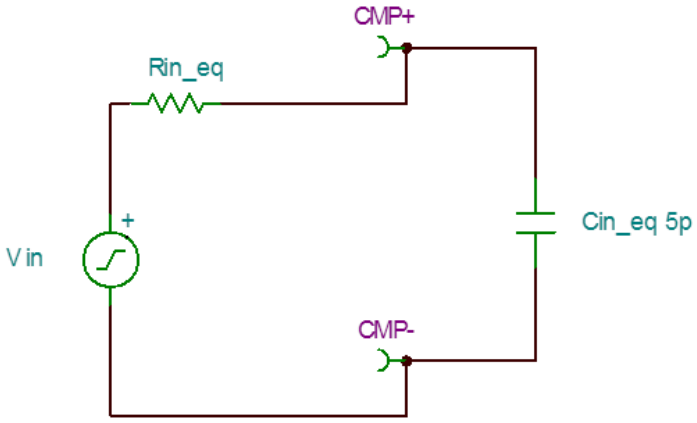


Figure 3: Comparator Input Capacitance

The total equivalent input capacitance, Ceq_in, combined with the total input resistance, Rin_eq, will form a single pole which will attenuate the input signal. Since our maximum input frequency is 32MHz we will choose a low pass frequency point no lower than this. As shown in Figure 4 we will need to limit Rin_eq to less than or equal to 995 ohms.



$$fmax = 32MHz$$

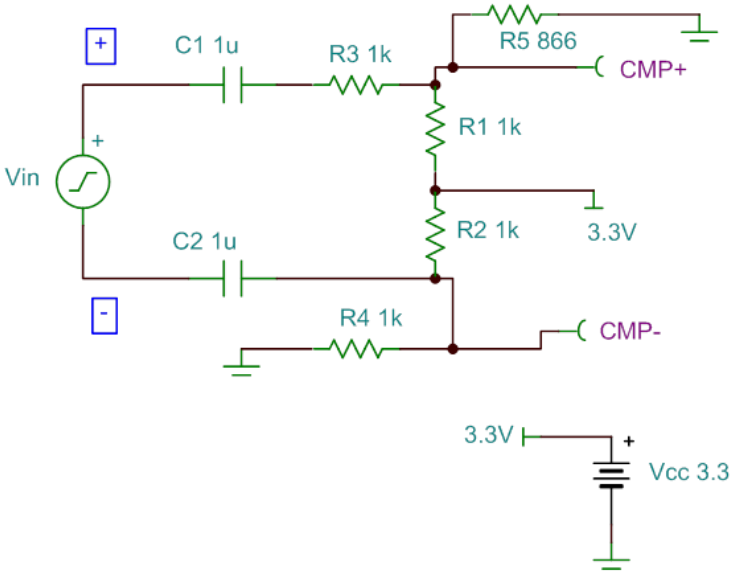
$$f\_3dB = \frac{1}{2\pi(Cin\_eq)(Rin\_eq)}$$

$$32MHz = \frac{1}{2\pi(5pF)(Rin\_eq)} \rightarrow Rin\_eq = 995\ ohm$$

Figure 4: Low Pass Filter Limitations

3.3 Input Scaling Offset

The input scaling offset circuit consists of R1, R2, R4, R5 and the supply voltage Vcc, as shown in Figure 5. The offset is computed for dc with no dynamic input signal. R2 and R4 divide Vcc to give CMP- a 1.65V offset. R1 and R5 divide down Vcc to yield a 1.53V offset on CMP+. Through the use of standard values CMP+ is about 100mV lower than CMP-. This ensures that with the TLV3501 input offset voltage of +/-6.5mV plus room for noise margin we will have the TLV3501 output forced to zero when no signal is present, as required by our design specifications.

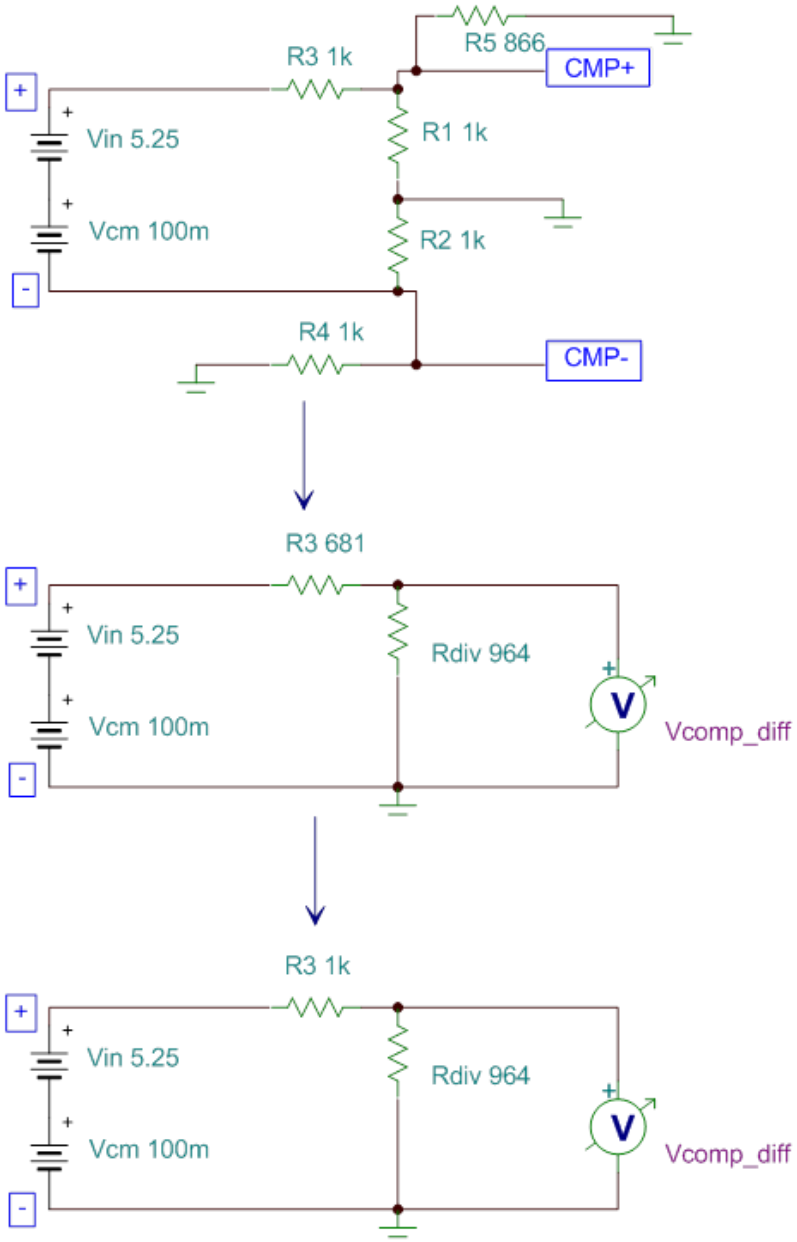


1) Offset both inputs to mid-supply so Vin negative voltages will be offset to a positive value to meet TLV3501common mode voltage range.
2) Set CMP- > (CMP+) + 100mV to ensure with Vin=0V TLV3501 Output = 0V.
3) From Figure 4 we know Rin_eq = 995 ohms to allow Vin to pass due to TLV3501 input capacitance.
4) Start by using 1k range values to yield Rin_eq = 995 ohms.
5) On CMP- use standard values and set R2=R4=1k for Vcm=Vcc/2
6) On CMP+ use standard values and set CMP+ < (CMP-) - 100mV.
Set R1=1k to keep near matched resistance from Vcc to GND. Select R5 for offset from CMP-.

Figure 5: Input Scaling Offset

3.4 Input Divider

Once the Vin signal is ac coupled into our comparator circuit, we need to ensure its amplitude is no larger than the minimum input common mode voltage range of the TLV3501. Figure 6 details our analysis for choosing the last scaling resistor, R3, to adequately divide down the maximum Vin amplitude to within our minimum common mode input of the TLV3501.

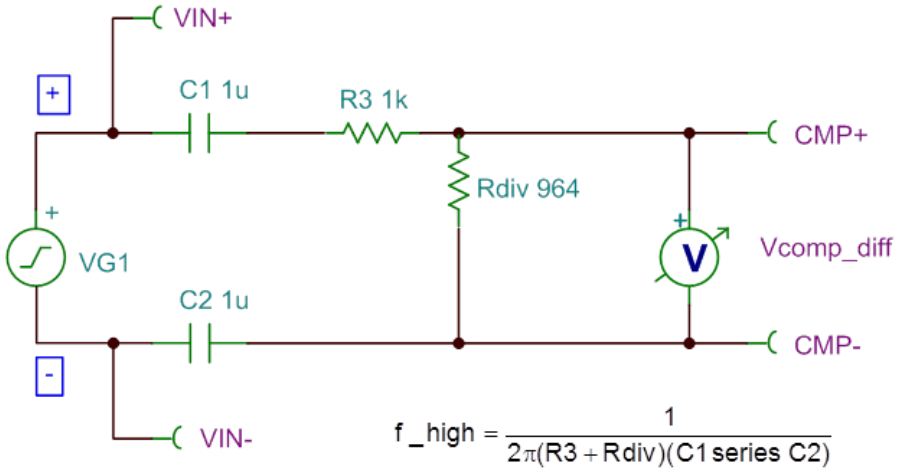


1) Vin_max = 5.25V + 100mV.
2) Equivalent resistor network in series with R3 is 964 ohms.
3) Minimum Vcc = 3.135V
4) Keep Vcomp_diff < 3.135V to meet Vcm specification of TLV3901.
5) R3_min = 681 ohms. Choose R3=1k for better margin and standard value already used.

Figure 6: Input Divider

3.5 Input High Pass Filter

The ac coupling of Vin into our comparator is set by R3, Rdiv, C1 and C2 as detailed in Figure 7.



1) fin_min = 2kHz
2) Set f_high < 200Hz. At least one decade under desired pass frequency for high pass cut frequency.
3) For standard capacitor value set C1=C2 = 1uF.
4) f_high calculates as 162Hz.

Figure 7: Input High Pass Filter

3.6 Recommend Component Properties

Table 4 gives recommended component properties for the parts used in the AC Coupled Comparator circuit.

Table 4. Recommended Component Properties

Ref Designator	Value	Recommended Properties
C1, C2	1uF	10%, Ceramic Capacitor, X5R or X7R tempco
R1, R2, R3, R4	1k ohm	1/8W, 1% Film Resistor, 100ppm tempco
R5	866 ohm	1/8W, 1% Film Resistor, 100ppm tempco
U1	TLV3501	Single Supply, +2.7V to +5.5V, Cin < 5pF, Propogation Delay < 12ns

4 Simulation

4.1 Input Scaling Frequency Check

The circuit in Figure 8 allows us to check the frequency response of the input scaling network. We have added an additional 4pF of differential input capacitance, Cdiff, to the TLV3501 in Figure 8 to properly model the complete input capacitance of the comparator. See Appendix A for details on this modification.

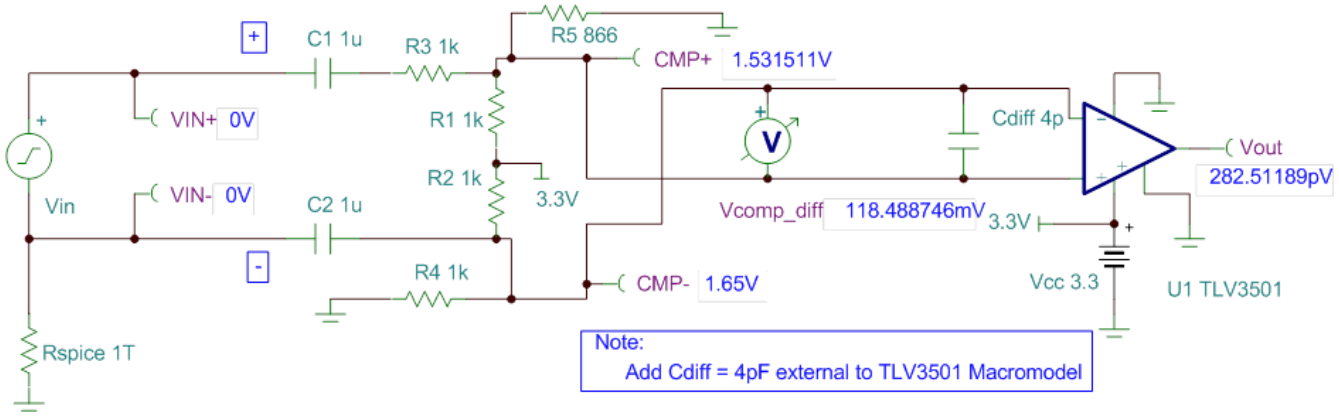


Figure 8: Input Scaling Frequency Test Circuit

From Figure 9, we see that the input scaling network will pass signals between the -3dB high-pass point of 162Hz to the low pass cut-off frequency of 64MHz. The 162Hz is about one decade away from our specified low frequency signal range of 2KHz. The 64MHz low pass is about twice our upper specified operating frequency of 32MHz.

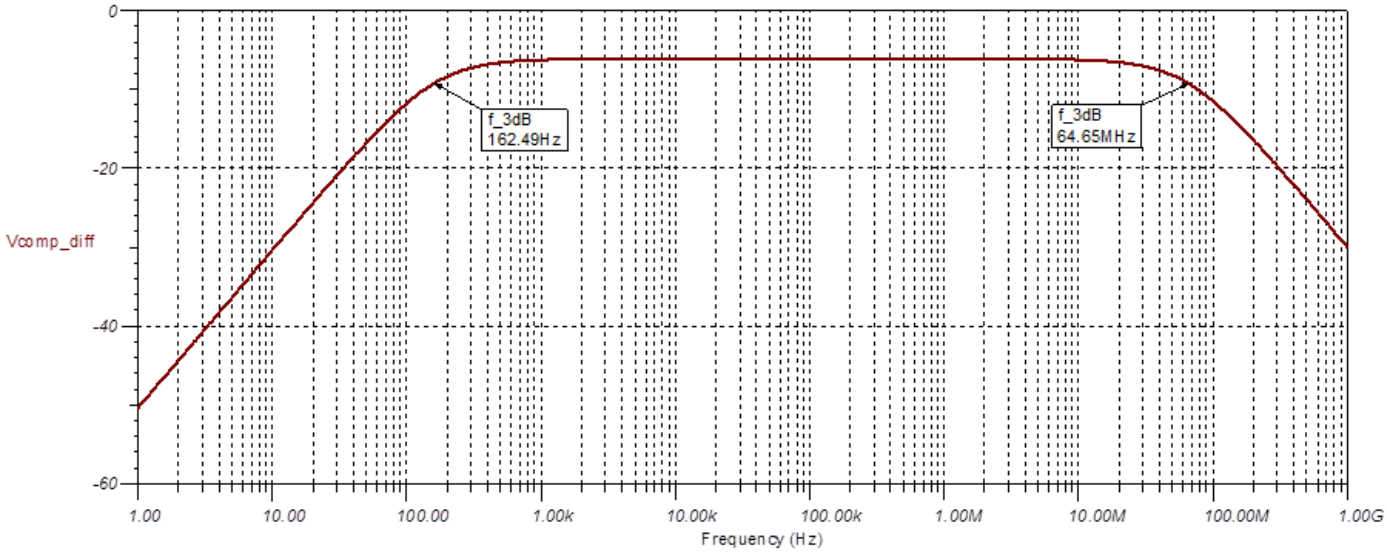


Figure 9: Input Scaling Frequency Response

4.2 AC Coupled Signals Yield Negative Voltages

If we remove our dc offset voltage of Vcc=3.3V, as shown in the test circuit of Figure 10, we can see the effects of ac coupling and the magnitudes of negative voltages that would appear at the TLV3501 inputs, CMP+ and CMP-. From superposition, whatever negative voltages that appear will be counteracted directly by our positive dc offsets of 1.65V on CMP- and 1.53V on CMP-. Figure 11 and Figure 12 show that we do indeed need our dc offsets on CMP+ and CMP-.

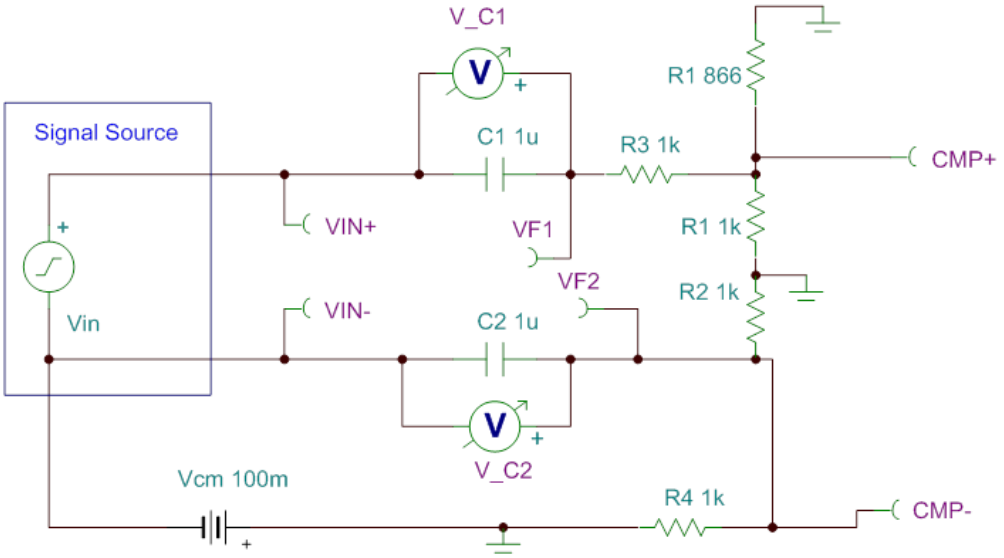


Figure 10: AC Coupled Signals - Negative Voltage Test

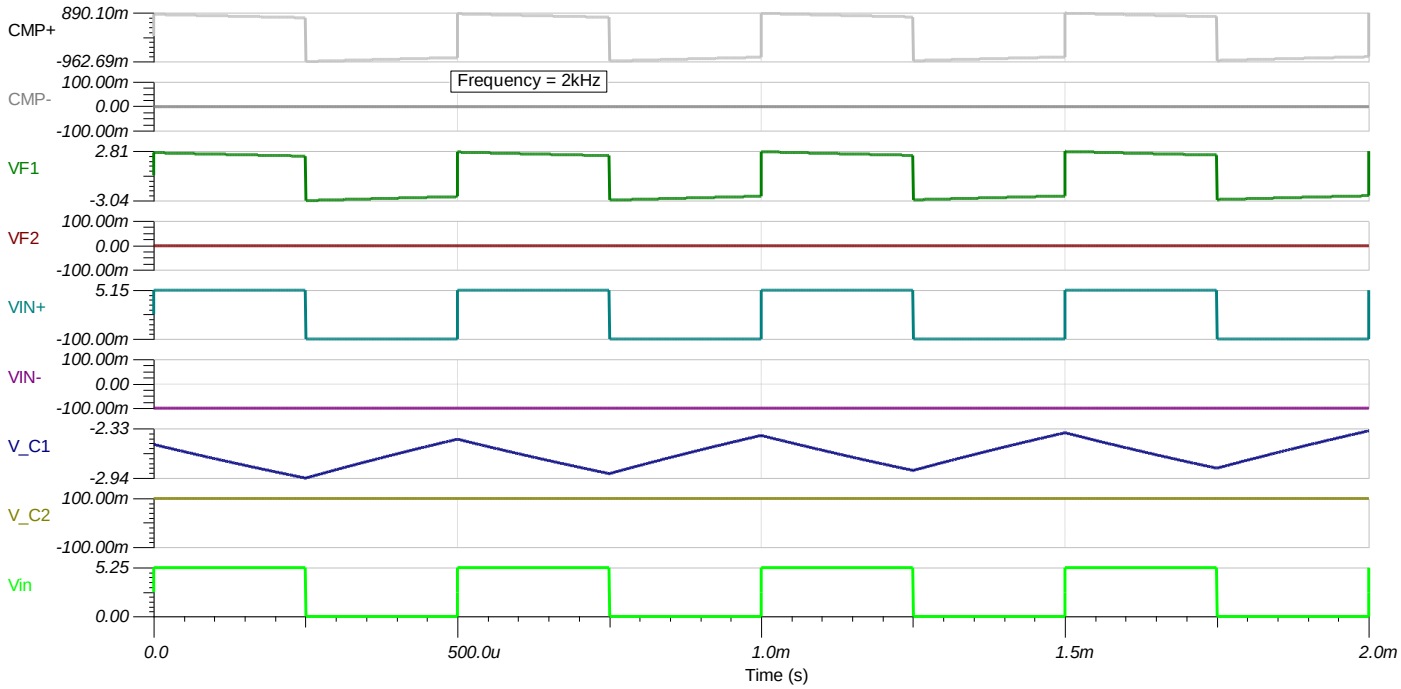


Figure 11: AC Coupled Signals - Negative Voltage 2kHz

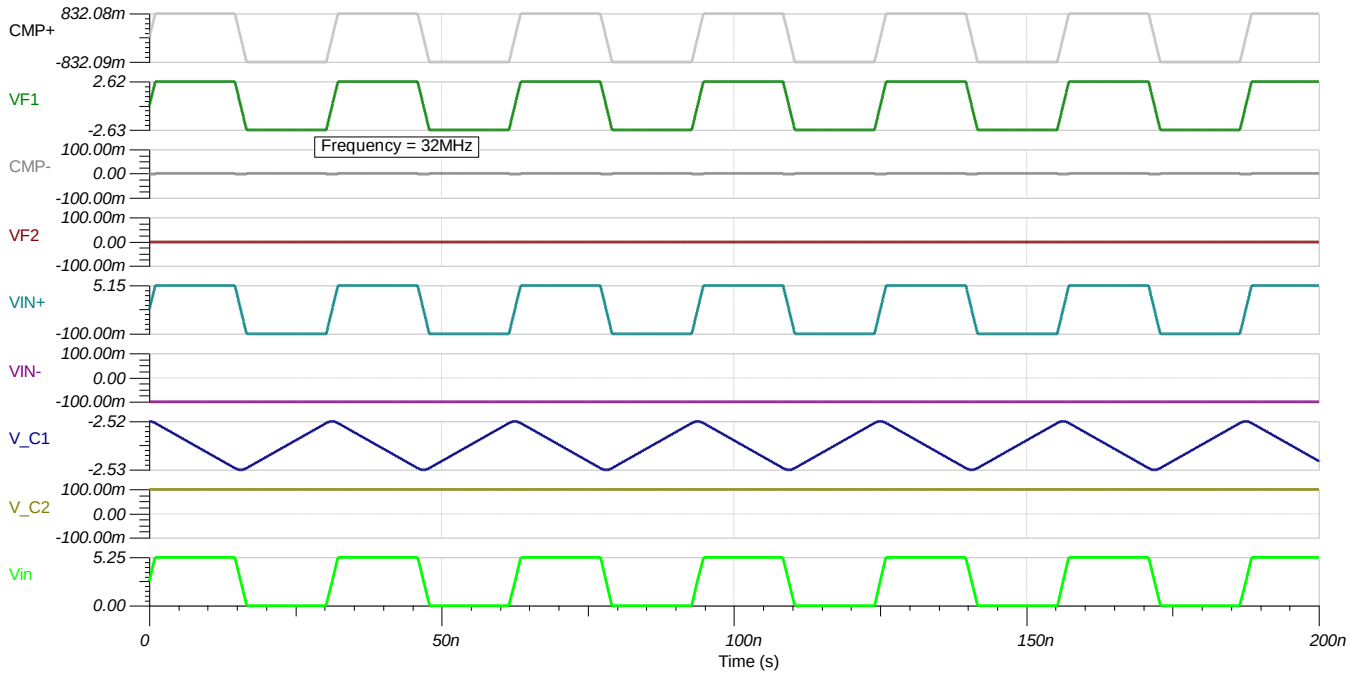


Figure 12: AC Coupled Signals - Negative Voltage 32MHz

4.3 Test Cases

The worst case test cases for our design are detailed in Table 5. To ensure the circuit works robustly at the extremes, minimum and maximum input amplitudes are checked along with minimum and maximum frequencies and minimum and maximum common mode input voltage. Figure 13 is the test circuit for checking our final design. Figure 14 shows the initial start-up time until reliable signals will be seen out of the TLV3501. By selecting “Zero Initial Values” in the Transient Analysis control window we can see how long it takes for the input AC coupling capacitors to charge resulting in reliable pulses out after about 672 microseconds. For Figure 15 through Figure 22 we set “Calculate Operating Point” in the Transient Analysis control window so we will ignore the start-up time and see the behavior of our circuit after C1 and C2 are past the initial start-up. The key thing we need to look at is how far CMP+ is swinging about CMP-. Input offset voltage for the TLV3501 comparator is +/-6.5mV. We want to stay way away from this in our high and low AC coupled input levels for reliable operation. In all test cases CMP+ is at least 120mV above or below CMP- in the high and low levels AC coupled into the TLV3501 comparator inputs.

Table 5. Worst Case Test Cases

Worst Case Test Cases for AC Coupled Comparator						
Test Case	**Frequency**	**VIL**	**VIH**	**VCM**	**Duty Cycle**	**Vcc**
1	2kHz	0V	5.25V	+100mV	40%	3.135V
2	2kHz	400mV	2.7V	+100mV	40%	3.135V
3	2kHz	0V	5.25V	-100mV	40%	3.135V
4	2kHz	400mV	2.7V	-100mV	40%	3.135V
5	32MHz	0V	5.25V	+100mV	40%	3.135V
6	32MHz	400mV	2.7V	+100mV	40%	3.135V
7	32MHz	0V	5.25V	-100mV	40%	3.135V
8	32MHz	400mV	2.7V	-100mV	40%	3.135V

To test our final design we will use an easy to adjust PWM signal generator as shown in Figure 13. This generator has adjustable frequency, duty cycle, Voh (output high voltage level), and Vol (output high voltage level). This allows us to easily test all corner conditions of our specification for our final circuit implementation compliance. Refer to Appendix B for design details of the PWM Signal Source. In addition we will add two common mode voltages, Vcm1 (+100mV) or Vcm2 (-100mV) to offset our PWM signal generator on the output of VCVS1 (voltage-controlled-voltage source) per our Vin common mode specification. A switch, SWB, will select our common mode input applied voltage. Note that both common mode voltages have a 1T ohm resistor in parallel with them t avoid SPICE convergence issues. The outputs of VCVS1 are each terminated with 1T ohm resistors for SPICE convergence when we connect to our ac coupled comparator inputs.

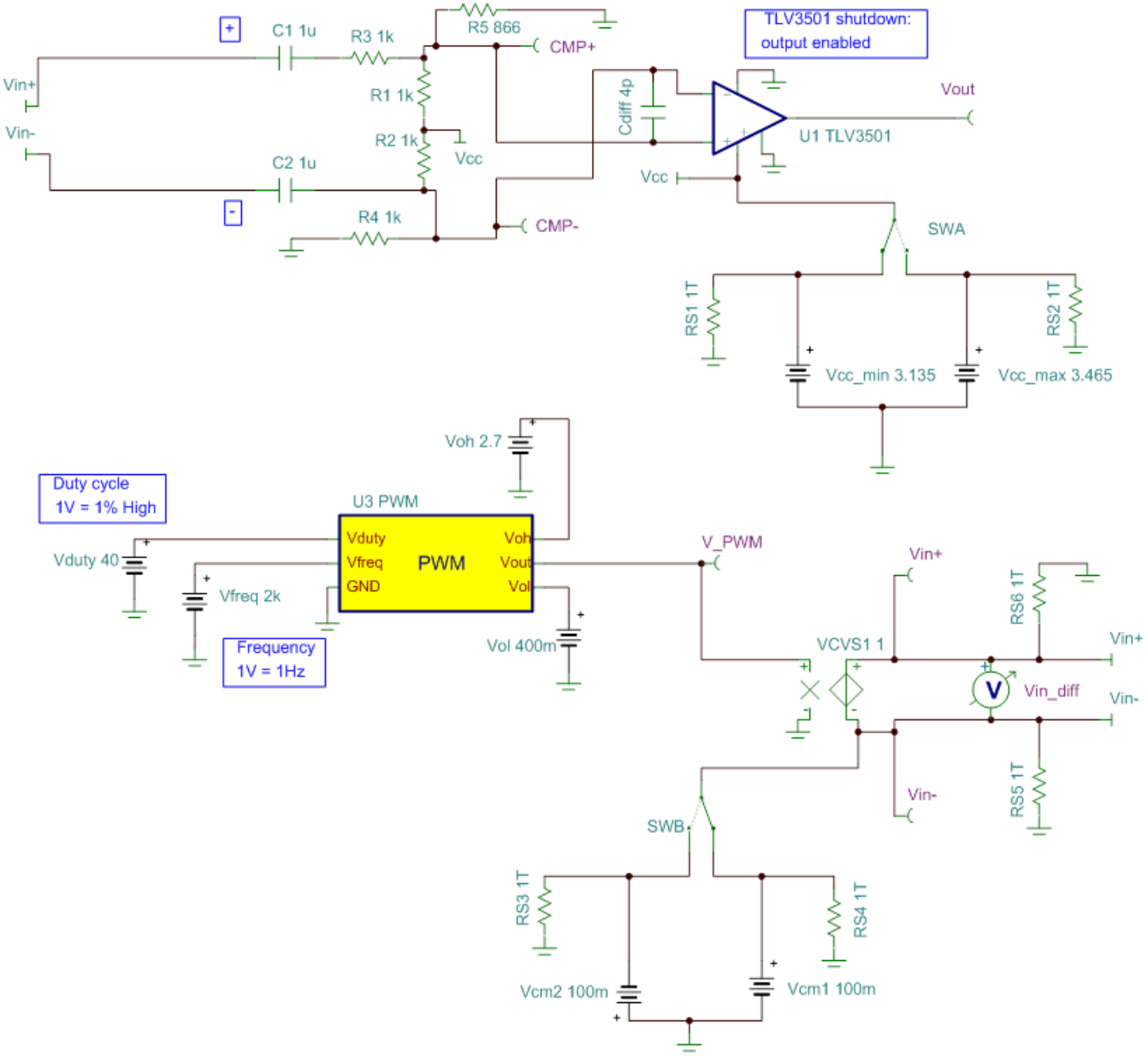


Figure 13: SPICE Test Case Circuit

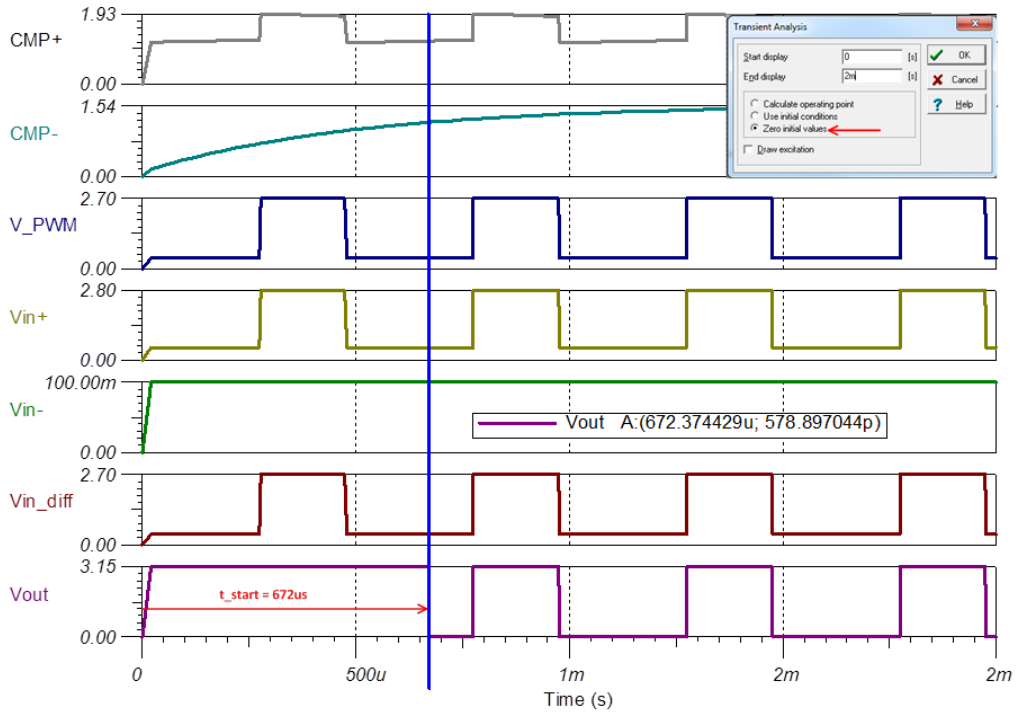


Figure 14: Initial Start Charge Time for CMP-

Test Case	Frequency	VIL	VIH	VCM	Duty Cycle	Vcc
1	2kHz	0V	5.25V	+100mV	40%	3.135V

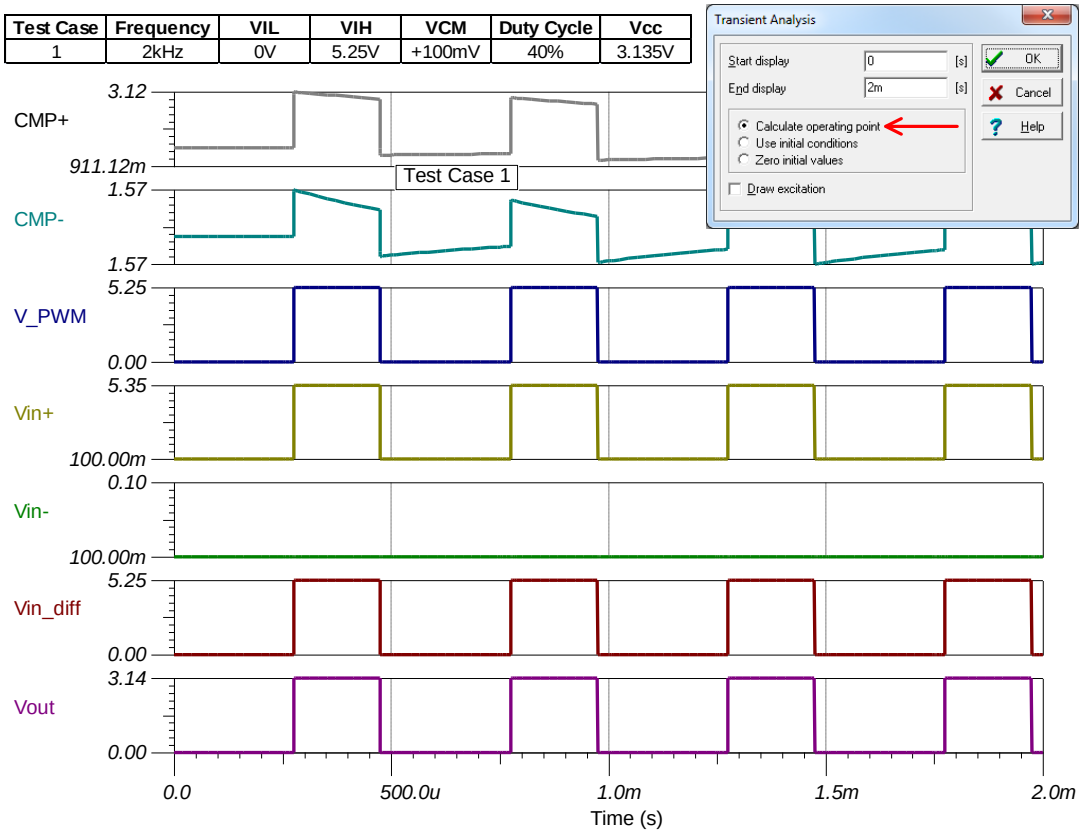


Figure 15: Test Case 1

Test Case	Frequency	VIL	VIH	VCM	Duty Cycle	Vcc
2	2kHz	400mV	2.7V	+100mV	40%	3.135V

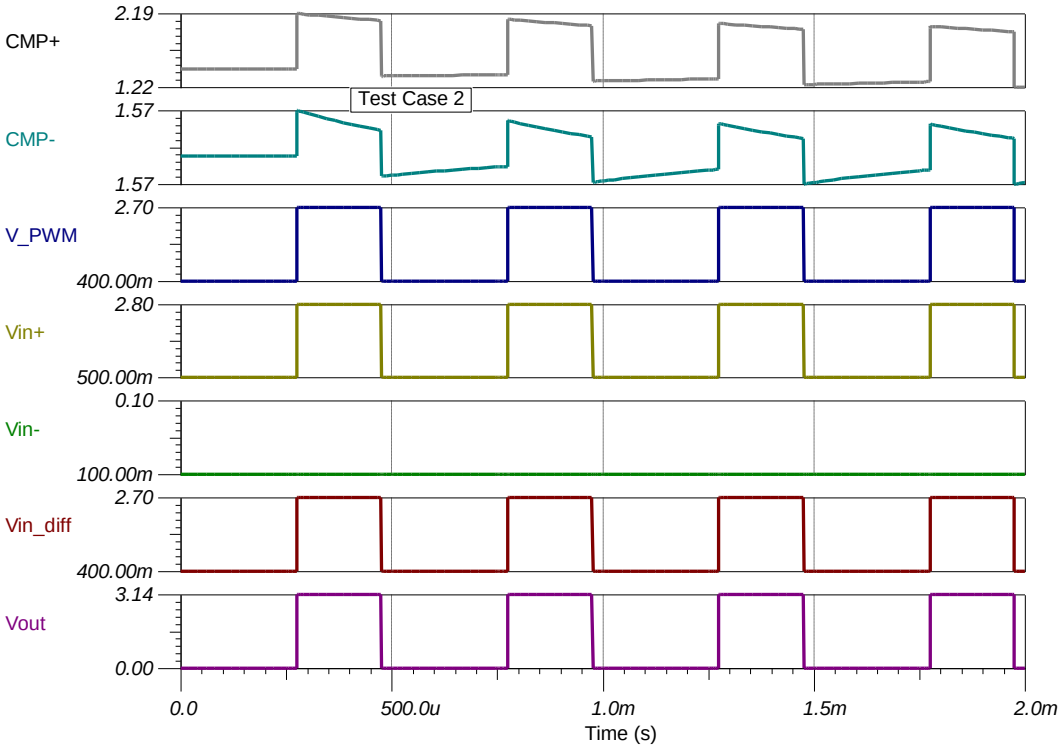


Figure 16: Test Case 2

Test Case	Frequency	VIL	VIH	VCM	Duty Cycle	Vcc
2kHz	0V	5.25V	-100mV	40%	3.135V	3.135V

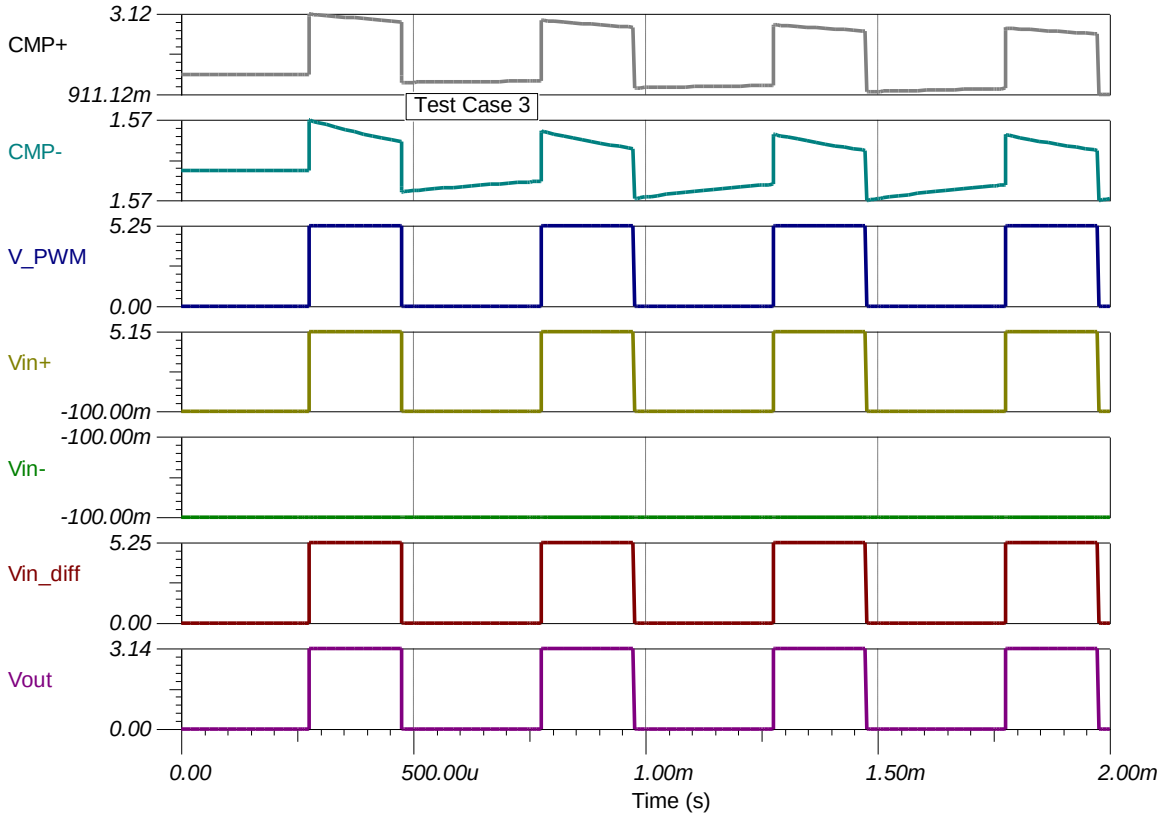


Figure 17: Test Case 3

Test Case	Frequency	VIL	VIH	VCM	Duty Cycle	Vcc
4	2kHz	400mV	2.7V	-100mV	40%	3.135V

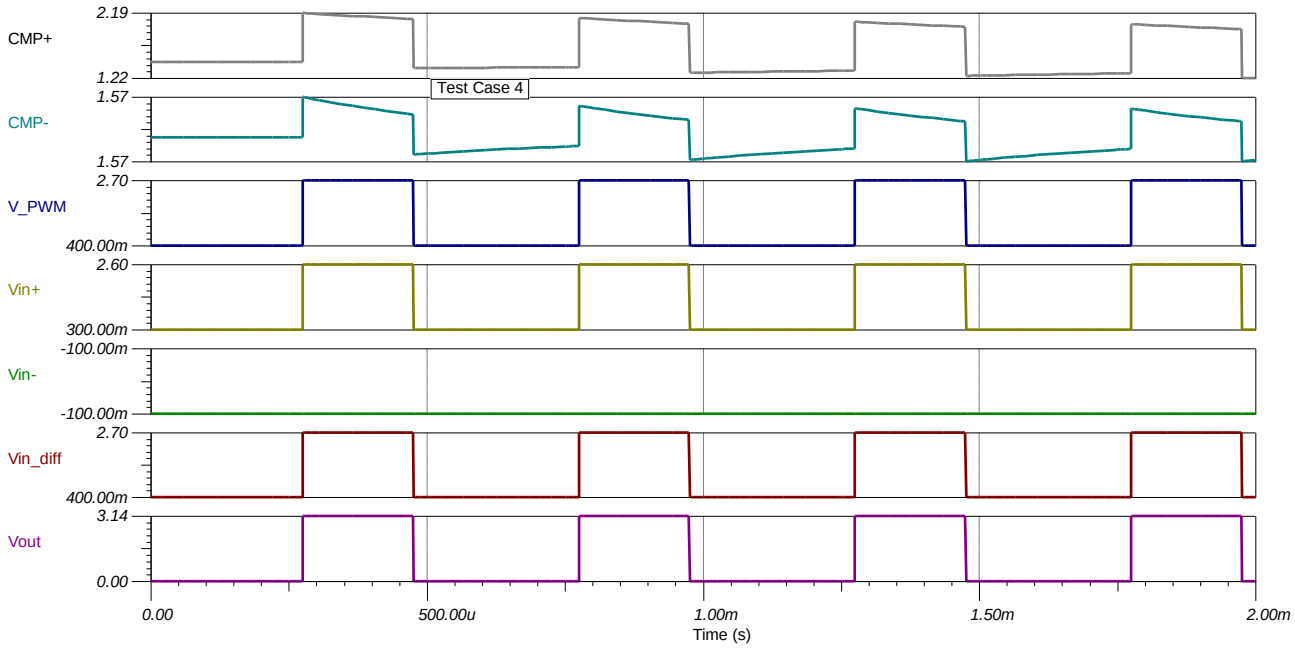


Figure 18: Test Case 4

Test Case	Frequency	VIL	VIH	VCM	Duty Cycle	Vcc
5	32MHz	0V	5.25V	+100mV	40%	3.135V

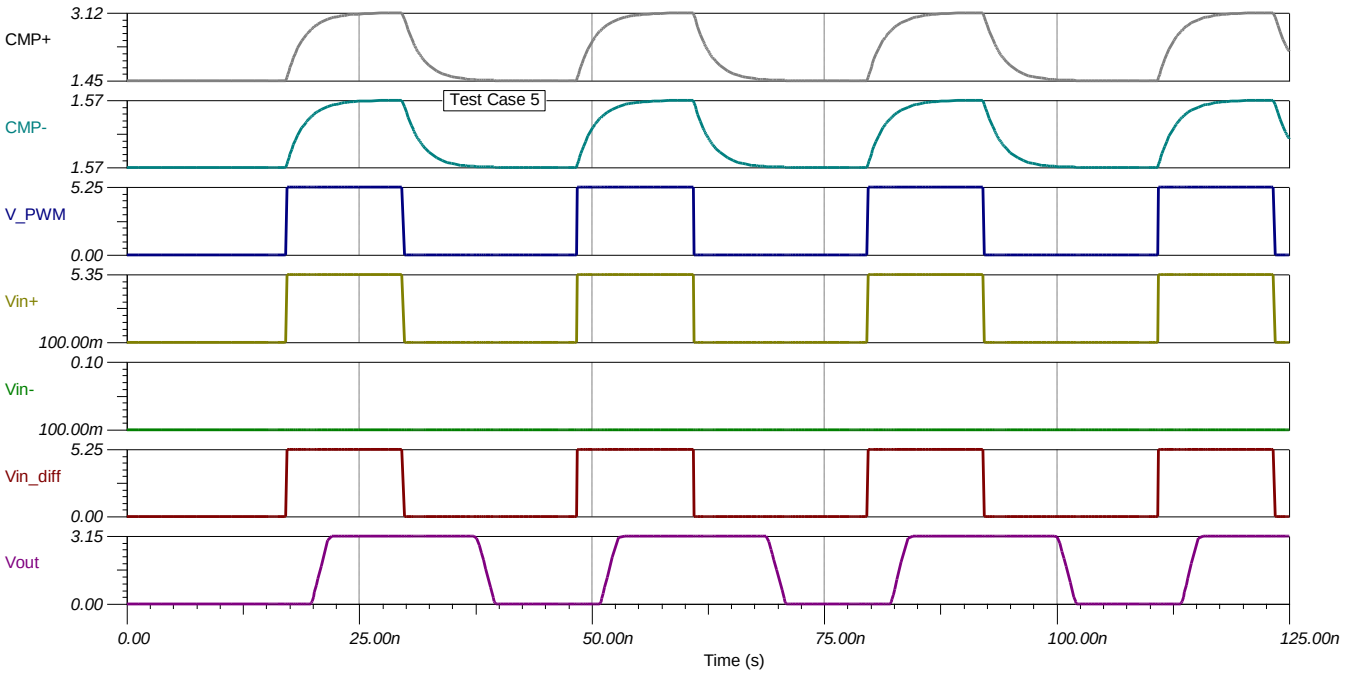


Figure 19: Test Case 5

Test Case	Frequency	VIL	VIH	VCM	Duty Cycle	Vcc
6	32MHz	400mV	2.7V	+100mV	40%	3.135V

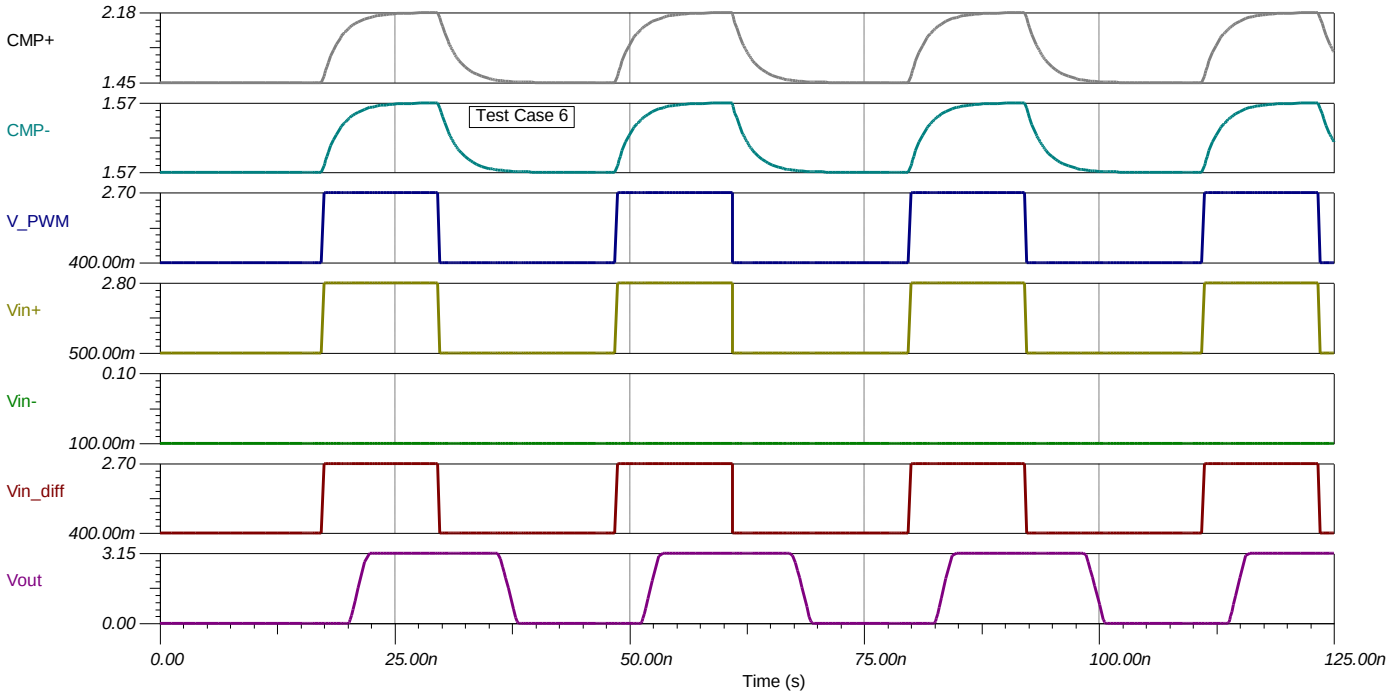


Figure 20: Test Case 6

Test Case	Frequency	VIL	VIH	VCM	Duty Cycle	Vcc
7	32MHz	0V	5.25V	-100mV	40%	3.135V

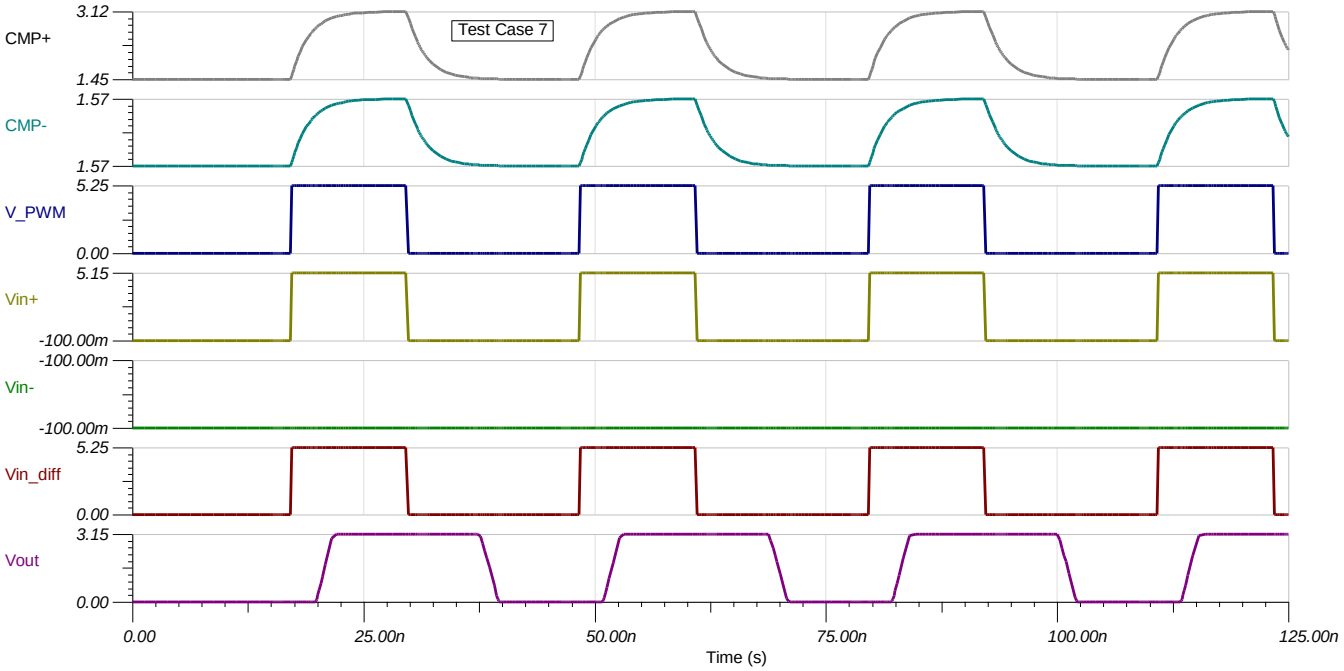


Figure 21: Test Case 7

Test Case	Frequency	VIL	VIH	VCM	Duty Cycle	Vcc
8	32MHz	400mV	2.7V	-100mV	40%	3.135V

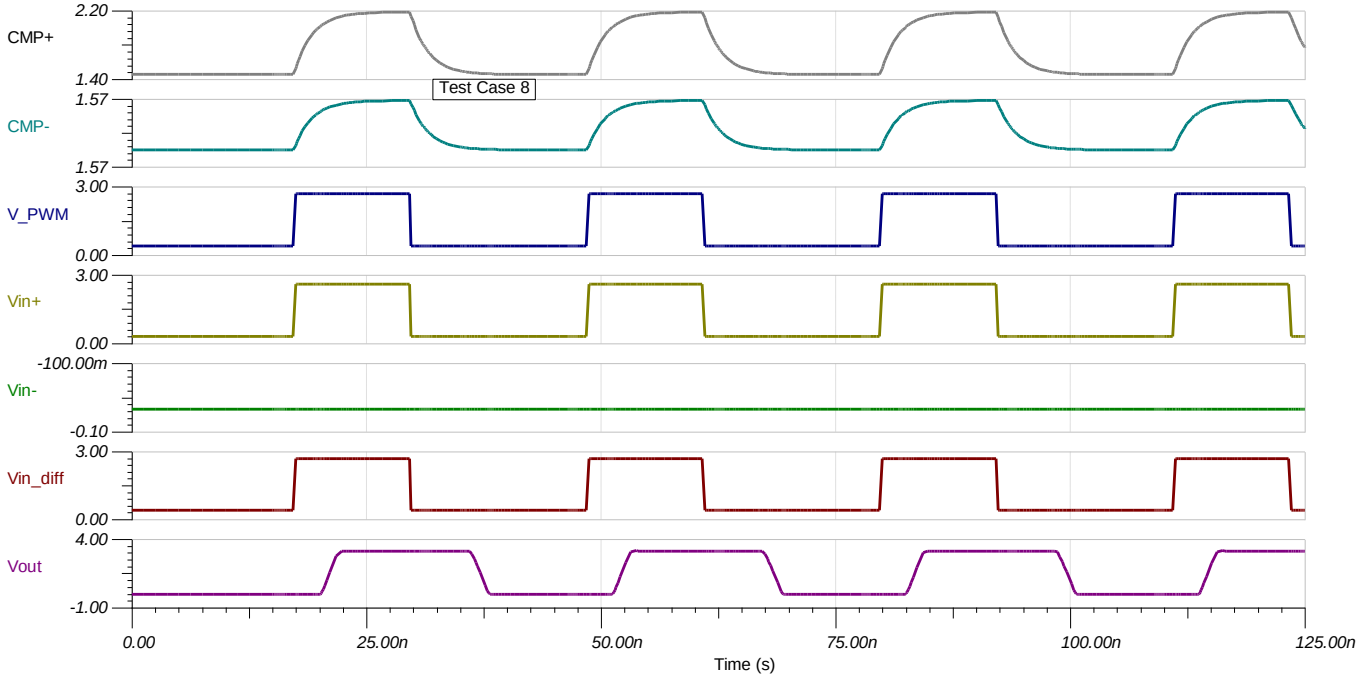


Figure 22: Test Case 8

5 Modifications

The components selected for this design were based on the design goals outlined at the beginning of the design process. Selecting a short propagation delay comparator such as the TLV3501 is critical in achieving the upper operating frequency of 32MHz. Initial tolerances and temperature coefficient of C1 and C2 should be analyzed for their effects on voltages coupled into the comparator inputs. Ensure all voltages remain within the common mode voltage range of the selected comparator. By using cut frequencies a decade away from the desired pass band frequencies, component sensitivities are minimized. Based on a minimum duty cycle of 40% and single supply operation from 2.7V < Vcc < 5.5V, Table 6 lists the maximum frequency possible, based on propagation delay, for rail to rail input comparators which are optimal for this type of design.

Table 6. Single Supply Comparators and Maximum Frequency for AC Coupled Comparator

Part	RRI	Channels	Vcc Min	Vcc Max	Output Type	Iq/Channel	Prop Delay	fmax
			(V)	(V)		(mA)	(us)	(Hz)
TLV3404	Yes	4	2.5	16	open drain	0.00095	300	1,333
TLV3402	Yes	2	2.5	16	open drain	0.00095	300	1,333
TLV3401	Yes	1	2.5	16	open drain	0.00095	300	1,333
TLV3704	Yes	4	2.7	16	push/pull	0.001	240	1,667
TLV3702	Yes	2	2.7	16	push/pull	0.001	240	1,667
TLV3701	Yes	1	2.7	16	push/pull	0.001	240	1,667
LMC7225	Yes	1	2	8	open dra*in*	1.2	29	13,793
LMC7215	Yes	1	2	8	push/pull	1.2	29	13,793
TLV3494	Yes	4	1.8	5.5	push/pull	0.0012	13.5	29,630
TLV3492	Yes	2	1.8	5.5	push/pull	0.0012	13.5	29,630
TLV3491	Yes	1	1.8	5.5	push/pull	0.0012	13.5	29,630
LPV7215	Yes	1	1.8	5.5	push/pull	0.013	12	33,333
TLV7211	Yes	1	2.7	15	push/pull	0.014	10	40,000
LMC7221	Yes	1	2.7	15	open drain	0.018	10	40,000
LMC7211	Yes	1	2.7	15	push/pull	0.014	10	40,000
LMC6762	Yes	2	2.7	15	push/pull	12.5	10	40,000
LMV7291	Yes	1	1.8	5.5	push/pull	0.016	1.3	307,692
LMV762	Yes	2	2.7	5.25	push/pull	0.7	0.27	1,481,481
LMV761	Yes	1	2.7	5.25	push/pull	0.7	0.27	1,481,481
LMV7239	Yes	1	2.7	5.5	push/pull	0.1	0.096	4,166,667
LMV7235	Yes	1	2.7	5.5	open drain	0.1	0.096	4,166,667
TLV3502	Yes	2	2.7	5.5	push/pull	5	0.012	33,333,333
TLV3501	Yes	1	2.7	5.5	push/pull	5	0.012	33,333,333

*fmax based on 40% duty cycle

6 About the Author

After earning a BSEE from the University of Arizona, in 1981, Tim Green has worked as an analog and mixed signal board/system design engineer, strategic marketing engineer, and linear applications engineer, for over 31 years. Product areas he has focused on are brushless motor control, aircraft jet engine control, missile systems, power op amps, data acquisition systems, CCD cameras, and analog/mixed signal semiconductors. Tim's most recent experience focused on Power Audio for the automotive market. He is currently a Senior Analog Applications Engineer in Precision Analog Linear Applications at Texas Instruments Inc, Tucson Design Center.

Appendix A.

A.1 TLV3501 Input Capacitance Test

Since a critical part of our design specification is high frequency operation, we will check that the TLV3501 SPICE macromodel matches the data sheet specifications for Ccm and Cdiff. Figure A-1 shows a simple test circuit in which we sweep an ac source through a known resistance, Rtest, and look at the 3dB frequency caused by this known resistance and the input capacitance of the SPICE macromodel. In Figure A-2 we compute the expected results of our test if just Ccm is modeled or if both Ccm and Cdiff are modeled. From Figure A-3, the results of our SPICE simulation, we see that only Ccm seems to be modeled in the TLV3501 SPICE macromodel. To make sure our design works robustly in the real world we will add Cdiff of 4pF external to the TLV3501 SPICE macromodel as shown in Figure A-4.

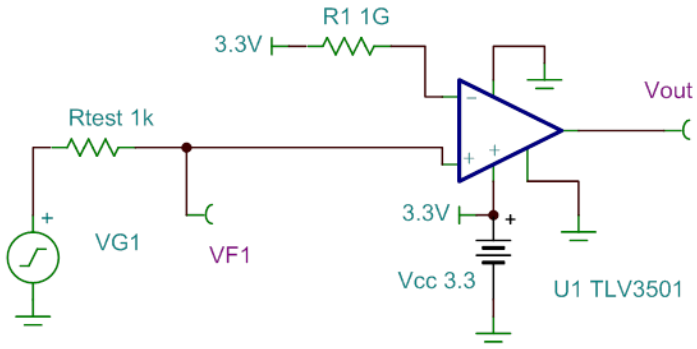
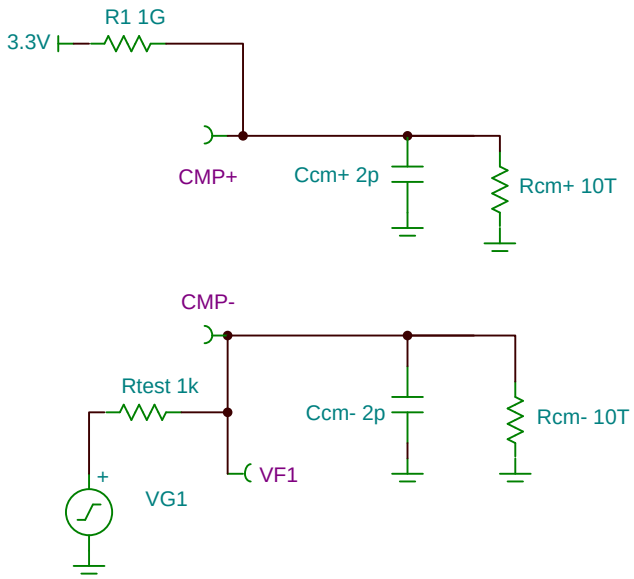


Figure A-1: TLV3501 Input Capacitance Test Circuit

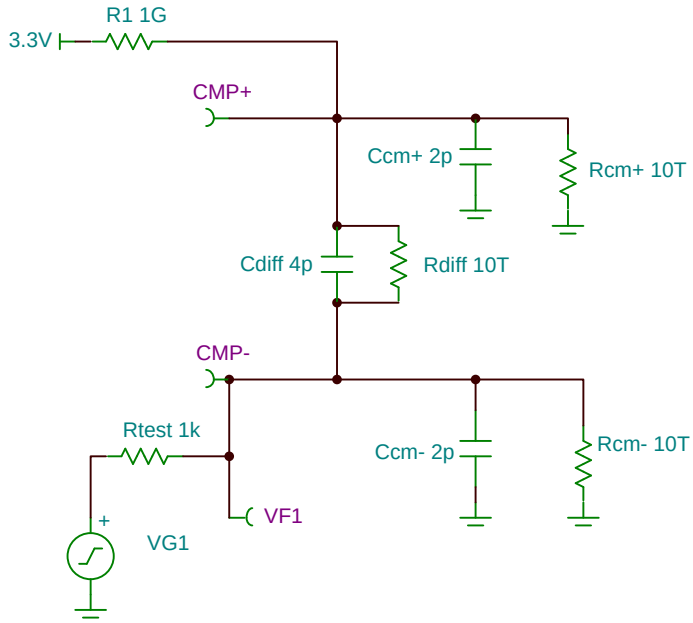
If TLV3501 has only Ccm Modeled



$$f\_3dB = \frac{1}{2\pi(Rtest)(Ccm-)}$$

$$f\_3dB = \frac{1}{2\pi(1k)(2pF)} = 79.58MHz$$

If TLV3501 has Ccm and Cdiff Modeled



$$f\_3dB = \frac{1}{2\pi[Rtest][(Ccm-)//(Cdiff\ in\ series\ with\ Ccm+)]}$$

$$f\_3dB = \frac{1}{2\pi(1k)(3.333pF)} = 47.75MHz$$

Figure A-2: TLV3501 Input Capacitance Check

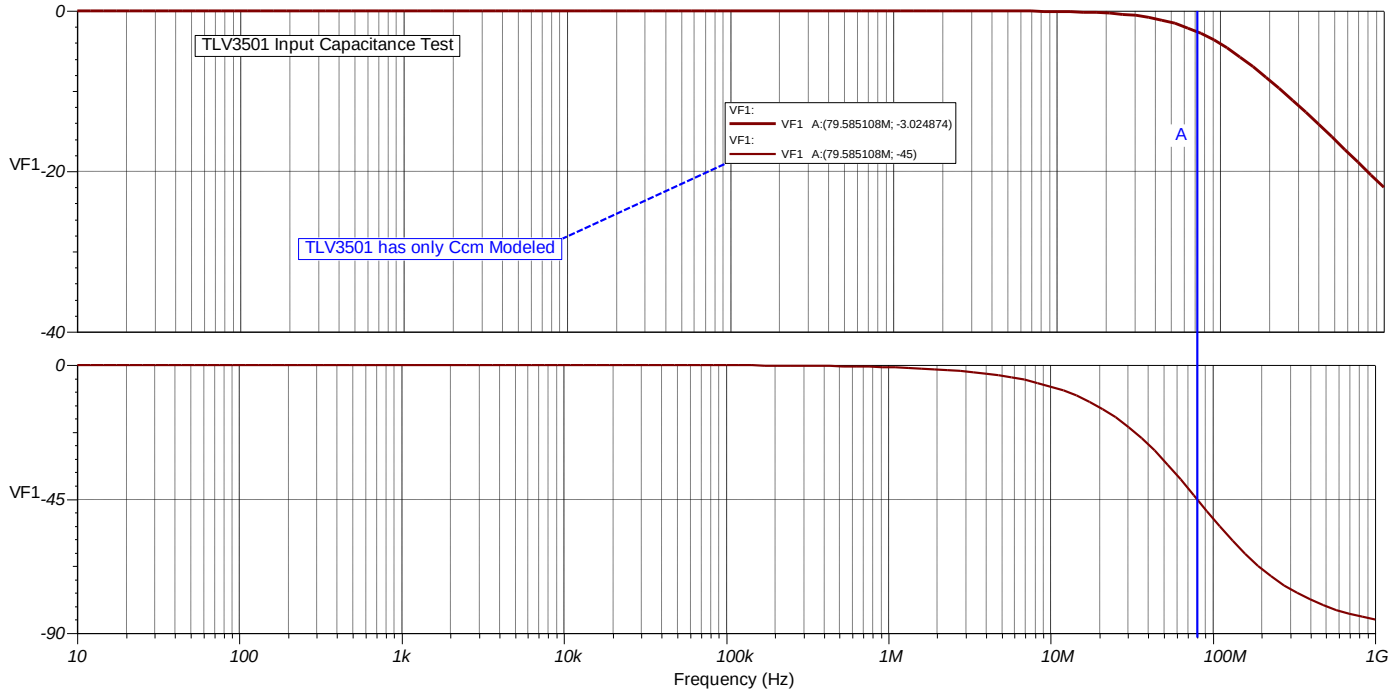


Figure A-3: TLV3501 Input Capacitance Simulation Results

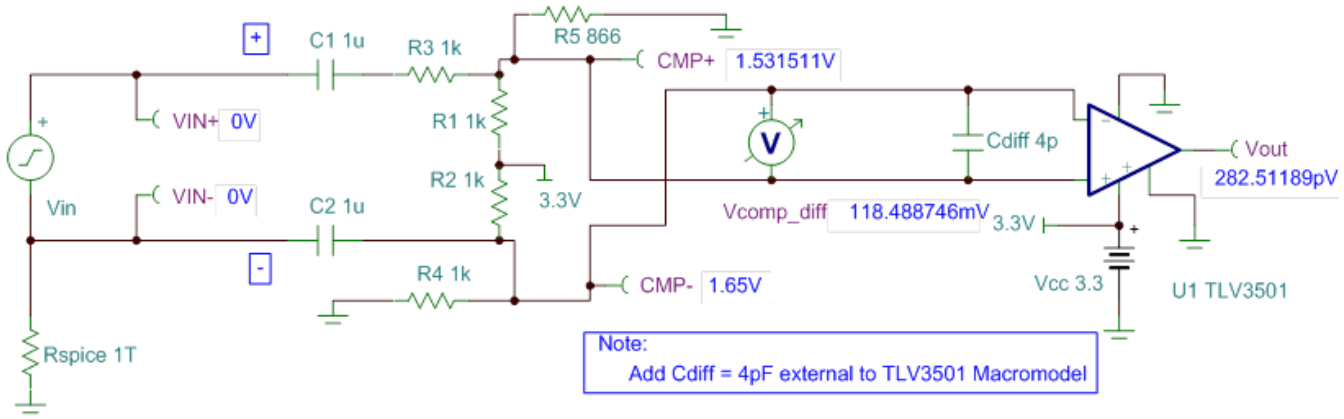


Figure A-4: Modified TLV3501 Comparator for Proper Input Capacitance

Appendix B.

B.1 Adjustable PWM Signal Source

To test our final design we will create an easy to adjust and use PWM signal generator shown in Figure B-1. This generator has adjustable frequency, duty cycle, Voh (output high voltage level), and Vol (output high voltage level). This will allow us to easily test all corner conditions of our specification for our final circuit implementation compliance. Figure B-2 shows the subcircuits used inside of the PWM Macromodel. VCO is a SPICE standard voltage-controlled-oscillator out of which we will use the triangle wave output scaled for 0V to 1V. Frequency is scaled for 1V=1Hz. External to the macromodel, duty cycle is scaled 0V to 100V for 0% to 100% respectively. Internally we scale this from 0 to 1V by VCVS2. An ideal comparator, VCVS1, compares the triangle waveform (0V to 1V) to the duty cycle setting (0V to 1V). The output high and low limits, Voh and Vol, are set externally and become the limit values of U2, a voltage-controlled-voltage source with clamp limits.

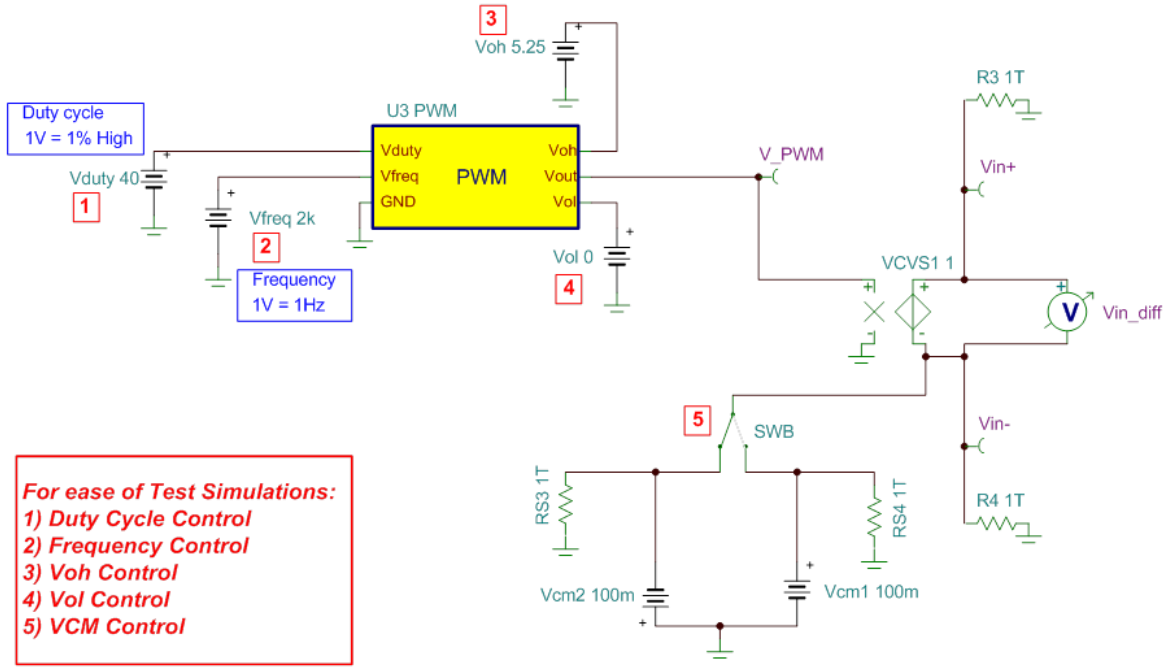


Figure B-1: Transient Analysis PWM Source

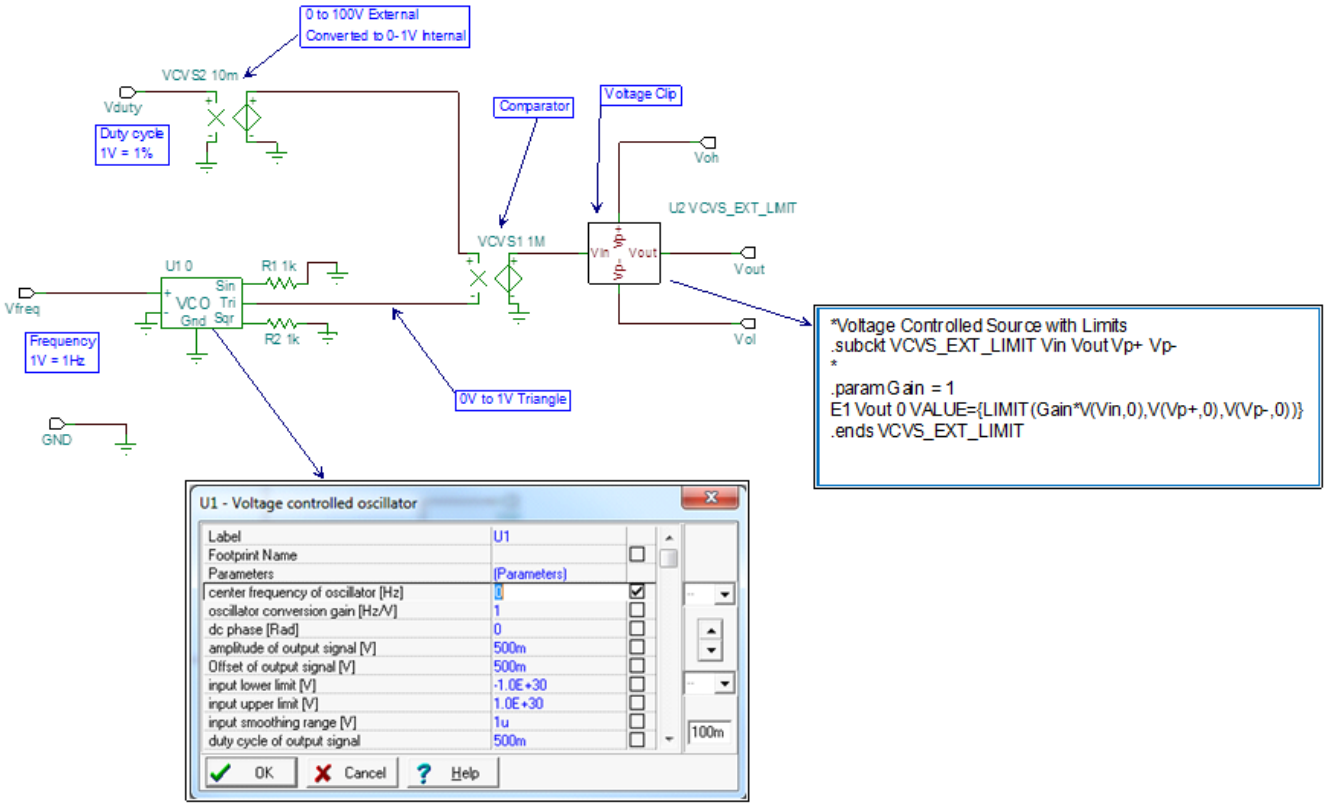


Figure B-2: PWM Macromodel Details

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