Critical Conduction Mode PFC Control IC
SSC2005S
Application Note

General Description
SSC2005S is a Critical Conduction Mode (CRM) control IC for power factor correction (PFC).
Since no input voltage sensing and no auxiliary winding for inductor current detection are required, the IC allows the realization of low standby power and the low number of external components. The product achieves high cost-performance and high efficiency PFC converter system.

Features and Benefits
- Inductor Current Detection
  (No auxiliary winding required)
- Low Standby Power
  (No input voltage sensing required)
- Minimum Off-time Limitation Function to restrict the Rise of Operation Frequency
- High Accuracy Overcurrent detection: \(-0.60 \text{ V} \pm 5\%\)
- Protection Functions
  Overcurrent Protection (OCP) ------ pulse-by-pulse
  Overvoltage Protection (OVP) --------- auto restart
  FB Pin Undervoltage Protection (FB_UVP) -------------------------------- auto restart
  Thermal Shutdown Protection with hysteresis (TSD) -------------------------------- auto restart

Typical Application Circuit

Electrical Characteristics
- VCC pin Absolute Maximum Ratings, \(V_{CC} = 28 \text{ V}\)
- OUT pin source current, \(I_{OUT(SRC)} = -500 \text{ mA}\)
- OUT pin sink current, \(I_{OUT(SNK)} = 1000 \text{ mA}\)

Applications
PFC Circuit up to 200 W of Output Power such as:
- AC/DC Power Supply
- Digital appliances for large size LCD/PDP television and so forth
- OA equipment for Computer, Server, Monitor, and so forth
- Communication facilities
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1. Absolute Maximum Ratings

- For additional details, refer to the datasheet.
- The polarity value for current specifies a sink as “+”, and a source as “−”, referencing the IC.
- Unless specifically noted $Ta = 25 \, ^{\circ}C$

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Pins</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC Pin Voltage</td>
<td>$V_{CC}$</td>
<td>8 – 6</td>
<td>28</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>OUT Pin Source Current</td>
<td>$I_{OUT(SRC)}$</td>
<td>7 – 6</td>
<td>−500</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>OUT Pin Sink Current</td>
<td>$I_{OUT(SNK)}$</td>
<td>7 – 6</td>
<td>1000</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>FB Pin Voltage</td>
<td>$V_{FB}$</td>
<td>1 – 6</td>
<td>−0.3 to 5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>COMP Pin Current</td>
<td>$I_{COMP}$</td>
<td>2 – 6</td>
<td>−200 to 200</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>RT Pin Current</td>
<td>$I_{RT}$</td>
<td>3 – 6</td>
<td>−500 to 0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>RDLY Pin Current</td>
<td>$I_{RDLY}$</td>
<td>4 – 6</td>
<td>−500 to 0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>CS Pin Voltage</td>
<td>$V_{CS}$</td>
<td>5 – 6</td>
<td>−5 to 0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Allowable Power Dissipation</td>
<td>$P_D$</td>
<td>–</td>
<td>0.5</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>Operating Ambient Temperature</td>
<td>$T_{OP}$</td>
<td>–</td>
<td>−40 to 110</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$T_{stg}$</td>
<td>–</td>
<td>−40 to 150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$T_j$</td>
<td>–</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

2. Recommended Operating Conditions

Recommended operating conditions means the operation conditions maintained normal function shown in electrical characteristics.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Pins</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC Pin Voltage in Operation</td>
<td>$V_{CC(OP)}$</td>
<td>8 – 6</td>
<td>14</td>
<td>26</td>
</tr>
<tr>
<td>RT Pin Resistance</td>
<td>$R_{RT}$</td>
<td>3 – 6</td>
<td>15</td>
<td>47</td>
</tr>
<tr>
<td>RDLY Pin Resistance</td>
<td>$R_{RDLY}$</td>
<td>4 – 6</td>
<td>15</td>
<td>47</td>
</tr>
<tr>
<td>Output Voltage – Input Voltage</td>
<td>$V_{OUT} - V_{IN}$</td>
<td>–</td>
<td>20</td>
<td>–</td>
</tr>
</tbody>
</table>
### 3. Electrical Characteristics

- For additional details, refer to the datasheet.
- The polarity value for current specifies a sink as “+”, and a source as “−”, referencing the IC.
- Unless specifically noted, $T_a = 25 \, ^\circ C$, $V_{CC} = 14 \, V$, $V_{CS} = 0.1 \, V$.

#### Power Supply Operation

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Pins</th>
<th>Rating</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation Start Voltage</td>
<td>$V_{CC(ON)}$</td>
<td></td>
<td>8–6</td>
<td>10.5</td>
<td>12.0</td>
<td>13.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operation Stop Voltage</td>
<td>$V_{CC(OFF)}$</td>
<td></td>
<td>8–6</td>
<td>8.2</td>
<td>9.5</td>
<td>11.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operation Voltage Hysteresis</td>
<td>$V_{CC(HYS)}$</td>
<td></td>
<td>8–6</td>
<td>1.4</td>
<td>2.5</td>
<td>3.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Circuit Current in Operation</td>
<td>$I_{CC(ON)}$</td>
<td>$V_{CC} = 9.5 , V$</td>
<td>8–6</td>
<td>2.0</td>
<td>3.1</td>
<td>4.4</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Circuit Current in Non-Operation</td>
<td>$I_{CC(OFF)}$</td>
<td></td>
<td></td>
<td>40</td>
<td>80</td>
<td>160</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

#### Oscillation Operation

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Pins</th>
<th>Rating</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum On-Time</td>
<td>$I_{ON(MAX)}$</td>
<td>$V_{FB} = 1.5 , V, R_{DLY} = 22 , k\Omega$</td>
<td>7–6</td>
<td>15</td>
<td>23</td>
<td>33</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>Minimum Off-Time</td>
<td>$I_{OFF(MIN)}$</td>
<td>$R_{DLY} = 22 , k\Omega$</td>
<td>7–6</td>
<td>1.8</td>
<td>2.5</td>
<td>3.2</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>RDLY Pin Voltage</td>
<td>$V_{RDLY}$</td>
<td></td>
<td>4–6</td>
<td>1.3</td>
<td>1.5</td>
<td>1.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>RT Pin Voltage</td>
<td>$V_{RT}$</td>
<td></td>
<td>3–6</td>
<td>1.3</td>
<td>1.5</td>
<td>1.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Feedback Control Voltage</td>
<td>$V_{FB}$</td>
<td></td>
<td>1–6</td>
<td>2.46</td>
<td>2.50</td>
<td>2.54</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Feedback Line Regulation</td>
<td>$V_{FB(LR)}$</td>
<td></td>
<td>1–6</td>
<td>−8</td>
<td>1</td>
<td>12</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>FB Pin Bias Current</td>
<td>$I_{FB}$</td>
<td></td>
<td>1–6</td>
<td>−3.2</td>
<td>−2.0</td>
<td>−1.0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Error Amplifier Transconductance Gain</td>
<td>$g_m$</td>
<td></td>
<td>1–6</td>
<td>60</td>
<td>103</td>
<td>150</td>
<td>µS</td>
<td></td>
</tr>
<tr>
<td>COMP Pin Sink Current</td>
<td>$I_{COMP(SNK)}$</td>
<td></td>
<td>2–6</td>
<td>18</td>
<td>40</td>
<td>72</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>COMP Pin Source Current</td>
<td>$I_{COMP(SRC)}$</td>
<td></td>
<td>2–6</td>
<td>−72</td>
<td>−40</td>
<td>−18</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Zero Duty COMP Voltage</td>
<td>$V_{COMP(ZD)}$</td>
<td></td>
<td>2–6</td>
<td>0.50</td>
<td>0.65</td>
<td>0.90</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Restart Time</td>
<td>$t_{RS}$</td>
<td></td>
<td></td>
<td>30</td>
<td>50</td>
<td>80</td>
<td>µs</td>
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</tr>
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</table>

#### Drive Output

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Pins</th>
<th>Rating</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage (High)</td>
<td>$V_{OH}$</td>
<td>$I_{OUT} = –100 , mA$</td>
<td>7–6</td>
<td>10.0</td>
<td>12.0</td>
<td>13.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Voltage (low)</td>
<td>$V_{OL}$</td>
<td>$I_{OUT} = 200 , mA$</td>
<td>7–6</td>
<td>0.40</td>
<td>0.75</td>
<td>1.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Rise Time</td>
<td>$t_{r}$</td>
<td>$C_{OUT} = 1000 , pF$</td>
<td>7–6</td>
<td>–</td>
<td>60</td>
<td>120</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Output Fall Time</td>
<td>$t_{f}$</td>
<td>$C_{OUT} = 1000 , pF$</td>
<td>7–6</td>
<td>–</td>
<td>20</td>
<td>70</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

#### Zero Current Detection and Overcurrent Protection Function

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Pins</th>
<th>Rating</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero Current Detection Threshold Voltage</td>
<td>$V_{CS(ZCD)}$</td>
<td></td>
<td>5–6</td>
<td>−20</td>
<td>−10</td>
<td>0</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Zero Current Detection Delay Time</td>
<td>$t_{DLY(ZCD)}$</td>
<td>$R_{DLY} = 22 , k\Omega$</td>
<td>5–6</td>
<td>1.00</td>
<td>1.35</td>
<td>1.70</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>Overcurrent Protection Threshold Voltage</td>
<td>$V_{CS(OCP)}$</td>
<td></td>
<td>5–6</td>
<td>−0.63</td>
<td>−0.60</td>
<td>−0.57</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Overcurrent Protection Delay Time</td>
<td>$t_{DLY(OCP)}$</td>
<td></td>
<td>5–6</td>
<td>100</td>
<td>250</td>
<td>400</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CS Pin Source Current</td>
<td>$I_{CS}$</td>
<td></td>
<td>5–6</td>
<td>−110</td>
<td>−75</td>
<td>−40</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

---

(1) Design assurance item
(2) Shown in Figure 3-1
### Characteristic

<table>
<thead>
<tr>
<th>FB Pin Protection Function</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Pins</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overvoltage Protection</td>
<td>$V_{OVP}$</td>
<td>1 – 6</td>
<td>1.075 x$V_{FB}$</td>
<td>1.090 x$V_{FB}$</td>
<td>1.105 x$V_{FB}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Hysteresis</td>
<td>$V_{OVP(HYS)}$</td>
<td>1 – 6</td>
<td>55</td>
<td>90</td>
<td>125</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Overvoltage Protection</td>
<td>$V_{UVP}$</td>
<td>1 – 6</td>
<td>200</td>
<td>300</td>
<td>400</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Undervoltage Protection</td>
<td>$V_{UVP(HYS)}$</td>
<td>1 – 6</td>
<td>80</td>
<td>120</td>
<td>160</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Undervoltage Protection</td>
<td>$V_{UVP}$(HYS)</td>
<td>1 – 6</td>
<td>200</td>
<td>300</td>
<td>400</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Thermal Shutdown Protection</td>
<td>$T_{J(TSD)}$</td>
<td>(1)</td>
<td>–</td>
<td>135</td>
<td>150</td>
<td>–</td>
<td>°C</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>$T_{J(TSDHYS)}$</td>
<td>(1)</td>
<td>–</td>
<td>–</td>
<td>10</td>
<td>–</td>
<td>°C</td>
</tr>
<tr>
<td>Junction to Ambient</td>
<td>$\theta_{JA}$</td>
<td>(1)</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>180</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) Design assurance item

---

**Figure 3-1** Switching time
4. Functional Block Diagram

![Functional Block Diagram](image)

5. Pin Configuration Definitions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FB</td>
<td>Feedback signal input, overvoltage protection signal input and undervoltage protection signal input</td>
</tr>
<tr>
<td>2</td>
<td>COMP</td>
<td>Phase compensation</td>
</tr>
<tr>
<td>3</td>
<td>RT</td>
<td>Maximum on-time adjustment</td>
</tr>
<tr>
<td>4</td>
<td>RDLY</td>
<td>Turn-on delay time adjustment</td>
</tr>
<tr>
<td>5</td>
<td>CS</td>
<td>Overcurrent protection signal input and zero current detection signal input</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>7</td>
<td>OUT</td>
<td>Gate drive output</td>
</tr>
<tr>
<td>8</td>
<td>VCC</td>
<td>Power supply input for control circuit</td>
</tr>
</tbody>
</table>

6. Typical Application Circuit

![Typical Application Circuit](image)
7. Package Outline

SOIC8

NOTES:
1) All linear dimensions are in millimeters
2) Pb-free. Device composition compliant with the RoHS directive.

8. Marking Diagram

- **Part Number**: SC2005
- **Lot Number**: SKYM D
  - Y is the last digit of the year (0 to 9)
  - M is the month (1 to 9, O, N or D)
  - D is a period of days
    1: 1st to 10th
    2: 11th to 20th
    3: 21st to 31st

- **Sanken Control Number**
9. Operational Description

- All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.
- With regard to current direction, "+" indicates sink current (toward the IC) and "-" indicates source current (from the IC).

9.1 Critical Conduction Mode: CRM

Figure 9-1 and Figure 9-2 show the PFC circuit and CRM operation waveform. The IC performs the on/off operation of switching device Q1 in critical mode (the inductor current is zero) as shown in Figure 9-1. Thus the low drain current variation di/dt of power MOSFET is accomplished. Also, adjusting the turn-on timing at the bottom point of VDS free oscillation waveform (quasi-resonant operation), low noise, low switching loss and high efficiency PFC circuit is realized.

![Figure 9-1 PFC circuit](image)

![Figure 9-2 CRM operation waveform](image)

Figure 9-3 shows the internal CRM control circuit.

The power MOSFET Q1 starts switching operation by self-oscillation.

The control of on-time is as follows: the detection voltage \( R_{SS} \) is compared with the reference voltage \( V_{FB} = 2.50 \text{ V} \) by using error amplifier (Error AMP) connected to FB pin. The output of the Error AMP is averaged and phase compensated. This signal \( V_{COMP} \) is compared with the ramp signal \( V_{OSC} \) to achieve on-time control. The ON time becomes almost constant in commercial cycle by setting \( V_{COMP} \) respond to below 20 Hz (Figure 9-4). This is achieved by tuning the capacitor connected to COMP pin.

The off-time and the bottom on timing of \( V_{DS} \) are set by both zero current detection of drain current and the delay time configured by RDLY pin resistance. Thus simple PFC circuit with inductor having no auxiliary winding is realized.

![Figure 9-3 CRM control circuit](image)

![Figure 9-4 CRM operation waveforms](image)
9.2 Startup Operation

Figure 9-5 shows the VCC pin peripheral circuit.

VCC pin is a control circuit power supply input. The voltage is supplied by using external power supply. As shown in Figure 9-6, when VCC pin voltage rises to the Operation Start Voltage $V_{CC(ON)} = 12.0$ V, the control circuit starts operation.

When the VCC pin voltage decreases to $V_{CC(OFF)} = 9.5$ V, the control circuit stops operation by Undervoltage Lockout (UVLO) circuit, and reverts to the state before startup.

Since the COMP pin voltage rises from zero during startup period, the $V_{COMP}$ signal shown in Figure 9-3 gradually rises from low voltage. The on-width gradually increased to restrict the rise of output power by the Softstart Function. Thus the stress of the peripheral component is reduced.

![Figure 9-5 VCC pin peripheral circuit](image)

Figure 9-6 Relationship between VCC pin voltage and $I_{CC}$

9.3 Restart Circuit

Since the IC is self-oscillation type, when the duration of off-state of OUT pin voltage exceeds the Restart Time $t_{RS} = 50$ μs or more, OUT pin outputs on-signal as a trigger of switching operation and switching operation starts. At startup and intermittent oscillation period at light load, the restart circuit is activated and the switching operation is stabilized.

Since $t_{RS} = 50$ μs corresponds to the operational frequency of 20 kHz, the minimum frequency should be set to higher than 20 kHz at the inductance value design. In normal operation, the zero current detection circuit determines off-time.

9.4 Maximum On-time setting

In order to reduce audible noise of transformer at transient state, the IC has the Maximum on-time, $t_{ON(MAX)}$. This $t_{ON(MAX)}$ is adjusted by the resistance $R_T$ which is connected to RT pin.

Figure 9-7 shows the relation between $R_T$ value and $t_{ON(MAX)}$ in IC design. The $t_{ON(MAX)}$ is made into a larger value than $t_{ONSET\_MAX}$ that is result of Equation (1) in Section 10.1 Inductor.

![Figure 9-7 Relationship between $R_T$ value and $t_{ON(MAX)}$ value (IC design)](image)

9.5 Zero Current Detection

Figure 9-8 shows the peripheral circuit of RDLY pin and CS pin. Figure 9-9 shows the waveform of each pin.

The off-time and the bottom on timing of $V_{DS}$ are set by both zero current detection of drain current, $I_D$ and the delay time. Thus simple PFC circuit with inductor having no auxiliary winding is realized.

The zero current detection signal of $I_D$ is detected by $R_{CS}$ and it is inputted to CS pin as shown in Figure 9-8. While the power MOSFET is in OFF state, the CS pin voltage decrease to the absolute value of Zero Current Detection Threshold Voltage, $V_{CS\_ZCD} = -10$ mV, or less, the OUT pin outputs ON signal after turn-on delay time, $t_{DLY}$.

![Figure 9-8 The peripheral circuit of RDLY pin and CS pin](image)
9.6 Minimum Off-time Limit Function

In order to prevent the rise of operation frequency at light load, the IC have the Minimum Off-Time \( t_{\text{OFF(MIN)}} = 2.5 \mu s \).

If this Minimum Off-Time is shorter than the freewheeling time of inductor, the IC operates in discontinuous condition mode (DCM).

9.7 Overvoltage Protection (OVP) Function

Figure 9-12 shows the waveforms of Overvoltage Protection operation. When the FB pin voltage increase to Overvoltage Protection Threshold Voltage, \( V_{\text{OVP}} \). OUT pin voltage become Low immediately and the switching operation stops. As a result, the rise of output voltage is prevented. \( V_{\text{OVP}} \) is \( 1.090 \text{ times the Feedback Control Voltage, } V_{\text{FB}} = 2.50 \text{ V}. \) When the cause of the overvoltage is removed and FB pin voltage decreases to \( V_{\text{OVP}} - V_{\text{OVPHYS}} \), the switching operation restarts.

![Figure 9-12 Overvoltage protection waveform](image)

9.8 FB pin Under Voltage Protection (FB_UVP) Function

FB pin Under Voltage Protection (FB_UVP) is activated when the FB pin voltage is decreased by the malfunctions in feedback loop such as the open of \( R_{\text{VS1}} \) or the short of \( R_{\text{VS2}} \).

Figure 9-13 shows the FB pin peripheral circuit and internal circuit. When the FB pin voltage is decreased to \( V_{\text{UVP}} = 300 \text{ mV} \) or less, the OUT pin output is turned-off immediately and switching operation stops. This prevents the rise of output voltage. When the cause of malfunction is removed and the FB pin voltage rises to \( V_{\text{OVP}} + V_{\text{OVPHYS}} \), the switching operation restarts.

![Figure 9-13 The FB pin peripheral circuit and internal circuit](image)
In case the FB pin is open the FB pin voltage is increase and Overvoltage Protection (OVP) Function is activated as described in Section 9.7.

When the cause of malfunction is removed and the IC becomes normal control, the switching operation restarts.

9.9 Overcurrent Protection (OCP) Function

Figure 9-14 shows the CS pin peripheral circuit and internal circuit. The current of inductance, I_L is detected by the detection resistor, R_CS. The detection voltage, V_RCS, is feed into CS pin. The OCP COMP compares the detection voltage, V_RCS with Overcurrent Protection Threshold Voltage, V_CS(OCP) = −0.6 V. When V_RCS increases to absolute value of V_CS(OCP) or more, the OUT pin output is turned off by pulse-by-pulse.

As shown in Figure 9-14, the CS pin is connected to capacitor-resistor filter (R4 and C5) and zener diode, DZ_CS, for CS pin overvoltage protection.

![Figure 9-14 The CS pin peripheral circuit and internal circuit.](image)

10. Design Notes

10.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

- **Inductor**

Apply proper design margin to temperature rise by core loss and copper loss.

Inductance L_P of PFC in CRM mode are calculated as follows:

1) **Operational Frequency, f_SW(SET) and Maximum On-time, t_ON(SET)MAX**

At first, determine f_SW(SET) that is minimum operational frequency at the peak of the AC line waveform. The frequency becomes higher with lowering the input voltage. The frequency at the peak of the AC line waveform, f_SW(SET) should be set above frequency of 25 kHz.

The \( t_{\text{ON}(\text{SET})\text{MAX}} \) at \( f_{\text{SW}(\text{SET})} \) is calculated by Equation (1). The \( t_{\text{ON} \text{(MAX)}} \) described in “9.4 Maximum on-time setting” should be set above \( t_{\text{ON}(\text{SET})\text{MAX}} \).

\[
\frac{V_{\text{OUT}} - \sqrt{2 \times V_{\text{ACRMS\{MIN\}}}}}{P_{\text{OUT}} \times f_{\text{SW}(\text{SET})} \times V_{\text{OUT}}}
\]

Where,

\( V_{\text{OUT}} \) : Output voltage (V)

\( V_{\text{ACRMS\{MIN\}}} \) : Maximum AC input voltage rms value (V)

2) **Output Voltage, V_OUT**

The output voltage \( V_{\text{OUT}} \) of boost-converter is higher than input voltage.

Set the voltage of \( V_{\text{OUT}} \) higher than the peak value of the AC input voltage by approximately 20 V, according to following equation:

\[
V_{\text{OUT}} \geq \sqrt{2 \times V_{\text{ACRMS\{MAX\}}} + 20(V)
\]

Where,

\( V_{\text{ACRMS\{MAX\}}} \) : Maximum AC input voltage rms value (V)

3) **Inductance, L_P**

Substituting both minimum and maximum of AC input voltage to \( V_{\text{ACRMS}} \) choose a smaller one as \( L_P \) value.

\( L_P \) is calculated as follows:

\[
L_P = \frac{\eta \times \left( V_{\text{ACRMS}} \right)^2}{2 \times P_{\text{OUT}} \times f_{\text{SW}(\text{SET})} \times V_{\text{OUT}}}
\]

Where,

\( V_{\text{ACRMS}} \) : AC input voltage rms value (V)

\( P_{\text{OUT}} \) : Output power (W)

\( \eta \) : Efficiency of PFC (In general, the range of \( \eta \) is 0.90 to 0.97, depending on on-resistance of power MOSFET \( R_{\text{DS\{ON\}}} \) and forward voltage drop of rectifier diode \( V_F \))

4) **Inductor peak current, I_LP**

\( I_LP \) is peak current of the peak at the minimum AC input voltage.

\( I_LP \) calculated as follows:

\[
I_LP = \frac{2 \times \sqrt{2 \times P_{\text{OUT}}}}{\eta \times V_{\text{ACRMS\{MIN\}}}}
\]
Figure 10-1 shows the IC peripheral circuit.

- **FB Pin Peripheral Circuit (Output Voltage Detection)**
  The output voltage \( V_{OUT} \) is set using \( R_{VS1} \) and \( R_{VS2} \). It is expressed by the following formula:
  \[
  V_{OUT} = \left( \frac{V_{FB}}{R_{VS2}} + I_{FB} \right) \times R_{VS1} + V_{FB}
  \]
  \[\text{Where,} \]
  \( V_{FB} \) : Feedback reference voltage = 2.50 V
  \( I_{FB} \) : Bias current = −2 μA
  \( R_{VS1} \), \( R_{VS2} \) : Combined resistance to set \( V_{OUT} \)

  Since \( R_{VS1} \) have applied high voltage and have high resistance value, \( R_{VS1} \) should be selected from resistors designed against electromigration or use a combination of resistors for that.

  The value of capacitor C6 between FB pin and GND pin is set approximately 100 pF to 3300 pF, in order to reduce the switching noise.

- **COMP Pin Peripheral Circuit, \( R_s \), \( C_s \), \( C_p \)**
  Figure 10-1 shows the IC peripheral circuit.
  The FB pin voltage is induced into internal Error AMP. The output voltage of the Error AMP is averaged by the COMP pin. The on-time control is achieved by comparing the signal \( V_{COMP} \) and the ramp signal \( V_{OSC} \).
  \( C_s \) and \( R_s \) adjust the response speed of changing on-time according to output power.
  The typical value of \( C_s \) and \( R_s \) are 1 μF and 10 kΩ, respectively. When \( C_s \) value is too large, the response becomes slow at dynamic variation of output and the output voltage decreases.
  Since \( C_s \) and \( R_s \) affect on the soft-start period at startup, adjustment is necessary in actual operation.
  The ripple of output detection signal is averaged by \( C_p \). When the \( C_p \) value is too small, the IC operation may become unstable due to the output ripple. The value of capacitor \( C_p \) is approximately 0.47 μF.

- **RT Pin Peripheral Circuit, \( R_T \), \( C_3 \)**
  \( R_T \) shown in Figure 10-1 is for the adjustment of maximum on-time, \( t_{ON(MAX)} \). The \( t_{ON(MAX)} \) is made into a larger than \( t_{ON(SET)} \) value which is the result of Equation (1) in page 11 "Inductor" (see Figure 9-7).
  The value of capacitor \( C_3 \) in parallel with \( R_T \) is approximately 0.01 μF, in order to reduce the switching noise.

- **RDLY Pin Peripheral Circuit, \( R_{DLY} \), \( C_4 \)**
  \( R_{DLY} \) shown in Figure 10-1 is for the adjustment of the turn-on delay time, \( t_{DLY} \) of the Power MOSFET. As shown in Section 9.5 Zero Current Detection, adjust the value of \( R_{DLY} \) and turn-on timing to the bottom point of \( V_{DS} \) free oscillation waveform on actual operation in the application. The value of capacitor \( C_4 \) is approximately 0.01 μF, in order to reduce the switching noise.

- **CS Pin Peripheral Circuit**
  \( R_{CS} \) shown in Figure 10-1 is current sensing resistor. \( R_{CS} \) is calculated using the following Equation (6), where Overcurrent Protection Threshold Voltage \( V_{CS(OC)} \) is −0.6 V and \( I_{LP} \) is calculated using Equation (4).
  \[
  R_{CS} \leq \frac{|V_{CS(OC)}|}{I_{LP}}
  \]
  Both CR filter (R4 and C5) and DZCS (zener diode) are connected to CS pin.
  CR filter (R4 and C5) prevents IC from responding to the drain current surge at MOSFET turn-on and avoids the unstable operation of the IC.
  R4 value of approximately 47 Ω is recommended, since the CS Pin Source Current affects the accuracy of OCP detection (see Section 9.5).
  C5 value is recommended to be calculated by using following formula in which cut-off frequency of CR filter (C5 and R4) is approximately 1 MHz.
  \[
  C_5 = \frac{1}{2 \pi \times 1\text{MHz} \times R_5}
  \]
  In case R4 value is 47 Ω, C5 value is approximately 3300 μF.
  The absolute voltage of CS pin is −5 V. The CS pin voltage may exceed the absolute value when the startup current to charge output capacitor, C2, flows \( R_{CS} \). Thus \( DZ_{CS} \) is used for the overvoltage protection of the CS pin.
  \( DZ_{CS} \) value of approximately 3.9 V is recommended. The value should be higher than \( V_{CS(OC)} \) and be lower than CS pin absolute maximum rating of −5 V.

- **OUT Pin Peripheral Circuit (Gate Drive Circuit)**
  Figure 10-2 shows the OUT pin peripheral circuit.
  The OUT pin is the gate drive output which can drive the external power MOSFET directly.
Figure 10-2 the OUT pin peripheral circuit.

The maximum output voltage of OUT pin is the VCC pin voltage. The maximum current is −500 mA for source and 1 A for sink, respectively. R1 is for source current limiting. Both R2 and D2 are for sink current limiting. The values of these components are adjusted to decrease the ringing of Gate pin voltage and the EMI noise. The reference value is several ohms to several dozen ohms. R3 is used to prevent malfunctions due to steep dv/dt at turn-off of the power MOSFET, and the resistor is connected near the MOSFET, between the gate and source. The reference value of R3 is from 10 kΩ to 100 kΩ. R1, R2, D2 and R3 are affected by the printed circuit board trace layout and the power MOSFET capacitance. Thus the optimal values should be adjusted under actual operation of the application.

**VCC Pin Peripheral Circuit**

Figure 10-3 shows the VCC pin peripheral circuit. VCC pin is power supply input. VCC pin is supplied from an external power. When VCC pin and the external power supply are distant from each other, placing a film capacitor Cf between the VCC pin and the GND pin is recommended. The value of capacitor Cf is set approximately 0.47 μF, in order to reduce the switching noise.

![External Power Supply](image)

Figure 10-3 VCC pin peripheral circuit

**Power MOSFET Q1**

Choose a power MOSFET having proper margin of V\text{DSS} against output voltage V\text{OUT}. The size of heat sink is chosen taking into account some loss by switching and ON resistance of MOSFET. The RMS value of drain current, I_{\text{DRMS}} is expressed as follows:

\[
I_{\text{DRMS}} = \frac{2 \times \sqrt{2} \times P_{\text{OUT}}}{\eta \times V_{\text{ACRMS(MIN)}}} \times \sqrt{\frac{1}{6} - \frac{4 \times \sqrt{2} \times V_{\text{ACRMS(MEN)}}}{9 \times \pi \times V_{\text{OUT}}}}
\]

(8)

The loss \(P_{\text{RDS(ON)}}\) by on-resistance \(R_{\text{DS(ON)}}\) of power MOSFET is calculated as follows:

\[
P_{\text{RDS(ON)}} = (I_{\text{DRMS}})^2 \times R_{\text{DS(ON)25°C}}
\]

(9)

where,

\(V_{\text{ACRMS(MIN)}}\) : Minimum AC input voltage rms value (V)
\(P_{\text{OUT}}\) : Output power (W)
\(\eta\) : Efficiency of PFC
\(R_{\text{DS(ON)25°C}}\) : ON resistance of MOSFET at \(T_{\text{ab}} = 125 \, ^\circ\text{C}\)

**Boost Diode, D\text{FW}**

Choose a boost diode having proper margin of a peak reverse voltage \(V_{\text{RSM}}\) against output voltage \(V_{\text{OUT}}\). A fast recovery diode is recommended to reduce the switching noise and loss. Please ask our staff about our lineup. The size of heat sink is chosen taking into account some loss by \(V_{\text{F}}\) and recovery current of boost diode. The loss of \(V_{\text{F}}, P_{\text{DFW}}\) is expressed as follows:

\[
P_{\text{DFW}} = V_{\text{F}} \times I_{\text{OUT}}
\]

(10)

Where,

\(V_{\text{F}}\) : Forward voltage of boost diode (V)
\(I_{\text{OUT}}\) : Output current (A)

**Bypass Diode, D\text{BYP}**

Bypass diode protects the boost diode from a large current such as an inrush current. A high surge current tolerance diode is recommended. Please ask our staff about our lineup.

**Output Capacitor, C2**

Apply proper design margin to accommodate the ripple current, the ripple voltage and the temperature rise. Use of high ripple current and low impedance types, designed for switch-mode power supplies, is recommended, depending on their purposes. In order to obtain C2 value Co, calculate both Equation (11) and (12) described in following and select a larger value.

1) Given the C2 ripple voltage \(V_{\text{OUTRIPPLE}}\) (V\text{PP} for example), \(C_{O}\) is expressed as follows:

\[
C_{O} > \frac{I_{\text{OUT}}}{2 \times \pi \times f_{\text{LINE}} \times V_{\text{OUT(RI)}}}
\]

(11)

where,

\(f_{\text{LINE}}\) : Line frequency (Hz)
\(I_{\text{OUT}}\) : Output current (A)

The C2 voltage is expressed as follows:

\[
V_{\text{C2}} = V_{\text{OUT}} \pm \frac{V_{\text{OUT(RI)}}}{2}
\]
When the output ripple is high, the $V_{C2}$ voltage may reach to Overvoltage Protection voltage, $V_{OVP}$, in near the maximum value of $V_{C2}$, or input current waveform may be distorted due to the stop of the boost operation in near the minimum value of $V_{C2}$. It is necessary to select large $C_O$ value or change the setting of output voltage (boost voltage).

2) Given the output hold time as $t_{HOLD}$ (s), $C_O$ is expressed as follows:

$$C_O > \frac{2 \times P_{OUT} \times t_{HOLD}}{\left(V_{OUT}^2 - \left(V_{OUT\,(MIN)}\right)^2\right) \times \eta}$$  \hspace{1cm} (12)

where,

- $t_{HOLD}$ : Output hold time (s)
- $V_{OUT\,(MIN)}$ : Minimum output voltage of C2 during output hold (V)
- $\eta$ : Efficiency

In case $t_{HOLD} = 20$ ms, $P_{OUT} = 200$ W, $\eta = 90$ % and the output voltage = 330 V to 390 V, $C_O$ value is derived as 205 $\mu$F. Thus, $C_O$ value of approximately 220 $\mu$F is connected.

### 10.2 PCB Trace Layout and Component Placement

PCB circuit trace design and component layout affect proper functioning during operation, EMI noise, and power dissipation. Therefore, wide, short traces, and small circuit loops are important to reduce line impedance where high frequency current traces form a loop as shown in Figure 10-4. In addition, local GND and earth ground traces affect radiated EMI noise, and the same measures should be taken into account.

Switching mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layouts should be done to comply with all safety guidelines.

Furthermore, because an integrated power MOSFET is being used as the switching device, take account of the positive thermal coefficient of $R_{DS\,(ON)}$ when preparing a thermal design.

![Figure10-4 High-frequency current loops (hatched areas)](image)

Figure10-5 shows a circuit layout design example.

1. **Main Circuit Trace**
   - This trace contains switching current, and thus it should be as wide and short as possible.

2. **GND Trace Layout**
   - In order to reduce the effect of switching current in main circuit trace, the control ground circuit and the main circuit ground should be connected at point A in Figure10-5. Control ground should be connected by dedicated trace.

3. **Current Detection Resistor $R_{CS}$ Trace Layout**
   - In order to reduce the noise in current detection, the connection between $R_{CS}$ and R5 which is connected to CS pin should be dedicated trace.

4. **Peripheral Component of IC**
   - Place the components for phase compensation connected to COMP pin close to both COM pin and GND pin.

![Figure10-5 Example of connection of peripheral components](image)
11. Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

- Circuit schematic

<table>
<thead>
<tr>
<th>IC</th>
<th>SSC2005S</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>AC 85 to AC 265 V</td>
</tr>
<tr>
<td>Input power</td>
<td>200 W</td>
</tr>
<tr>
<td>Output voltage</td>
<td>398 V</td>
</tr>
<tr>
<td>Operation frequency (at maximum AC input)</td>
<td>60 kHz (AC 265 V)</td>
</tr>
</tbody>
</table>

- Bill of materials

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Part type</th>
<th>Ratings</th>
<th>Recommended Sanken Parts</th>
</tr>
</thead>
<tbody>
<tr>
<td>BR1</td>
<td>General</td>
<td>600 V</td>
<td></td>
</tr>
<tr>
<td>F1</td>
<td>Fuse</td>
<td>AC 250 V</td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>Inductor</td>
<td>160 μH</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>Ceramic</td>
<td>450 V, 0.68 μF</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>Ceramic</td>
<td>450 V, 0.68 μF</td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>Ceramic</td>
<td>450 V, 180 μF</td>
<td></td>
</tr>
<tr>
<td>C4</td>
<td>Ceramic</td>
<td>1kV, 470μF</td>
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</tr>
<tr>
<td>C5</td>
<td>Ceramic</td>
<td>1000 μF</td>
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<tr>
<td>C6</td>
<td>Ceramic</td>
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</tr>
<tr>
<td>C7</td>
<td>Ceramic</td>
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<td></td>
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<tr>
<td>C8</td>
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<td>C9</td>
<td>Ceramic</td>
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</tr>
<tr>
<td>R13</td>
<td>General</td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td>R14</td>
<td>General</td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td>R15</td>
<td>General</td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td>R16</td>
<td>General</td>
<td>1%</td>
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</tr>
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<tr>
<td>D2</td>
<td>Schottky</td>
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</tr>
<tr>
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<td>General</td>
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</tr>
<tr>
<td>U1</td>
<td>IC</td>
<td>SSC2005S</td>
<td></td>
</tr>
</tbody>
</table>

(1) Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.
(2) It is necessary to be adjusted based on actual operation in the application.
(3) Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
OPERATING PRECAUTIONS

In the case that you use Sanken products or design your products by using Sanken products, the reliability largely depends on the degree of derating to be made to the rated values. Derating may be interpreted as a case that an operation range is set by derating the load from each rated value or surge voltage or noise is considered for derating in order to assure or improve the reliability. In general, derating factors include electric stresses such as electric voltage, electric current, electric power etc., environmental stresses such as ambient temperature, humidity etc. and thermal stress caused due to self-heating of semiconductor products. For these stresses, instantaneous values, maximum values and minimum values must be taken into consideration. In addition, it should be noted that since power devices or IC’s including power devices have large self-heating value, the degree of derating of junction temperature affects the reliability significantly.

Because reliability can be affected adversely by improper storage environments and handling methods, please observe the following cautions.

Cautions for Storage

- Ensure that storage conditions comply with the standard temperature (5 to 35°C) and the standard relative humidity (around 40 to 75%); avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust on leads and solderability of the products that have been stored for a long time.

Cautions for Testing and Handling

When tests are carried out during inspection testing and other standard test periods, protect the products from power surges from the testing device, shorts between the product pins, and wrong connections. Ensure all test parameters are within the ratings specified by Sanken for the products.

Soldering

- When soldering the products, please be sure to minimize the working time, within the following limits:
  - $260 \pm 5 \, ^\circ C$  $10 \pm 1 \, \text{s (Flow, 2 times)}$
  - $380 \pm 10 \, ^\circ C$  $3.5 \pm 0.5 \, \text{s (Soldering iron, 1 time)}$

Electrostatic Discharge

- When handling the products, the operator must be grounded. Grounded wrist straps worn should have at least $1M\Omega$ of resistance from the operator to ground to prevent shock hazard, and it should be placed near the operator.
- Workbenches where the products are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should be grounded.
- When soldering the products, the head of soldering irons or the solder bath must be grounded in order to prevent leak voltages generated by them from being applied to the products.
- The products should always be stored and transported in Sanken shipping containers or conductive containers, or be wrapped in aluminum foil.
IMPORTANT NOTES

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