PR208

Spartan™-IIE Design 1

Dual Linear Regulator Power Management Solution Providing up to 800 mA from V_{IN} = 5.0 V

FEATURES:

- Dual channel low-dropout (LDO) linear regulator in thermally enhanced PowerPAD^{TM} package saves cost and space.
- Linear regulators start-up fast, allowing large in-rush currents for charging decoupling capacitors and FPGA start-up. The current draw on the input power supply is minimized by the use of the:
    - External supervisory (SVS) IC, U1, which monitors the input rail and prevents the regulator from enabling until the input bulk capacitors (not shown in the schematic) are fully charged.
    - Soft-start circuit consisting of the external PMOS transistor Q1 and supporting passive components to provide 10 ms rise time for V_{CCINT}
        - Soft-start circuit (Q1) forces sequencing of V_{CCO}, then V_{CCINT}, regardless of how SEQ is connected
- The design meets Xilinx's V_{CCINT} and V_{CCO} start-up profile requirements, where applicable, including monotonic voltage ramp, in-rush current and power voltage ramp time requirements.

IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at http://www.ti.com/xilinxfpga for more information and other reference designs.
- Link to datasheets at http://focus.ti.com/lit/ds/symlink/TPS70351.pdf and http://focus.ti.com/lit/ds/symlink/tlc7705.pdf.
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations in using linear regulators.
- Link to application note SLVA156 http://focus.ti.com/lit/an/slva156/slva156.pdf for more details on the soft start circuit.

IMPLEMENTATION NOTES:

- **Sequencing:** Although Xilinx FPGAs **do NOT require it**, this reference design employs sequencing. This practice is consistent with good power supply design and prevents the input power supply from being pulled down due to supporting in-rush currents for charging large capacitive loads.
- **V_{CCINT} minimum ramp time:** Met by Q1 softstart circuit.
- **I_{CCINT} inrush current:** Mitigated by softstart.
- **Power Dissipation/Thermal Issues:** The dual regulator, U2, is limited to 2W @ $T_A = 55^o$ C and no airflow, due to power dissipation limitation of the PowerPAD^{TM} package.

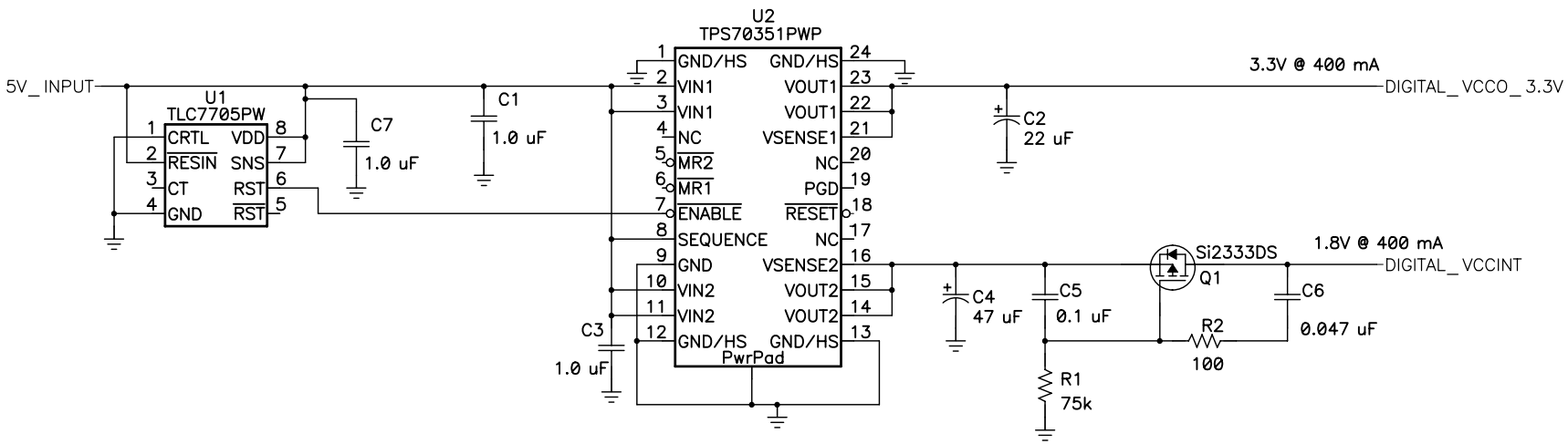
- Refer to the application section of the datasheet for maximum power dissipation at different ambient conditions and guidance on sizing the ground plane area underneath the package for heatsinking.
- The following equation can be used to solve for the maximum current on one rail if the other rail current is known:
  $P_{Dmax} = (V_{IN} - V_{CCINT}) * I_{CCINTmax} + (V_{IN} - V_{CCO})*I_{CCOmax}$

  As an example, with V_{IN} = 5 V, V_{CCINT} = 1.8V, V_{CCO} = 3.3 V, P_{Dmax} = 2 W and assuming that the linear regulator's total output current from both rails (I_{CCINT} + I_{CCO}) is split equally between the rails:
  - $P_{Dmax} = (V_{IN} - V_{CCINT}) * (I_{CCINTmax} + I_{CCOmax})/2 + (V_{IN} - V_{CCO})*(I_{CCINTmax} + I_{CCOmax})/2$ yields $I_{CCINTmax} + I_{CCOmax}$ = 800 mA so $I_{CCINTmax}=I_{CCOmax}$=400mA

- **Soft Start Circuitry:**
  - PMOS transistor Q1 should be selected so that its threshold voltage, V_{TH}, is at least 0.9 V below the V_{CCINT} voltage or lower (e.g., V_{TH} < 1.8 V – 0.9 V = 0.9 V). In addition, the transistor's R_{DSon} should be low enough, when driven by V_{CCINT}, that the voltage drop across the transistor at maximum current (e.g., $I_{CCINTmax}*R_{DSon}$) does not cause V_{CCINT} to fall below its -5% tolerance.
  - The drain of Q1 needs at least 47 uF of total capacitance in order for the soft-start circuit to work properly. The additional bulk bypass capacitance (not shown in the schematic) required for the V_{CCINT} rail of the FPGA will most likely meet this requirement.
- **Layout:** The 1.0 uF capacitor, C7, should be placed as close as possible between VDD and GND of the TLC7705 SVS IC.
- **Modifications:**
  - CT of TLC7705 is not connected, but can be used with a capacitor to add a delay between 5V rail coming up and RST = /EN of TPS70351.
  - Select the appropriate TPS703xx option. TPS70302 is the adjustable version, and $_{VOUT}$ is set by a voltage divider (external resistors) on the Vsense/FB pin.
  - Select the appropriate TLC77xx option to monitor the input supply voltage.
  - For a low-cost, discrete Supply Voltage Supervisory Circuit alternative to U1, please see reference design PR286 (Active-High Reset Output) or PR281 (Active-Low Reset Output).
  - Note that with lower input supplies, such as 3.3V, the TPS703xx can support higher output currents (see previously presented power dissipation calculations).

QUESTIONS?

- Send an email to **mailto:fpgasupport@list.ti.com**



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PR208 BOM

COUNT	RefDes	DESCRIPTION	SIZE	MFR	PART NUMBER
3	C1, C3, C7	Capacitor, Ceramic, 1.0-uF, 6.3-V, X5R, 10%	603	muRata	GRM188R60J105KA01
1	C2	Capacitor, Tantalum, 22-uF, 6.3-V, 20%	3528 (B)	Vishay	594D226X06R3B2T
1	C4	Capacitor, Tantalum, 47-uF, 10-V, 20%	3528 (B)	Vishay	594D476X010B2T
1	C5	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	603	muRata	GRM188R71E104KA01
1	C6	Capacitor, Ceramic, 0.047-uF, 16-V, X7R, 10%	603	muRata	GRM188R71C473KA01
1	Q1	MOSFET, P-ch, -12 V, 4 A, 51 milliohm	SOT23	Vishay	Si2333DS
1	R1	Resistor, Chip, 75k-Ohms, 1/16-W, 1%	603	Std	Std
1	R2	Resistor, Chip, 100-Ohms, 1/16-W, 1%	603	Std	Std
1	U1	IC, Voltage Supervisor, Micropower	35630	TI	TLC7705PW
1	U2	IC, Dual 1-A/2-A Low-dropout Regulator	PWP24	TI	TPS70353PWP

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