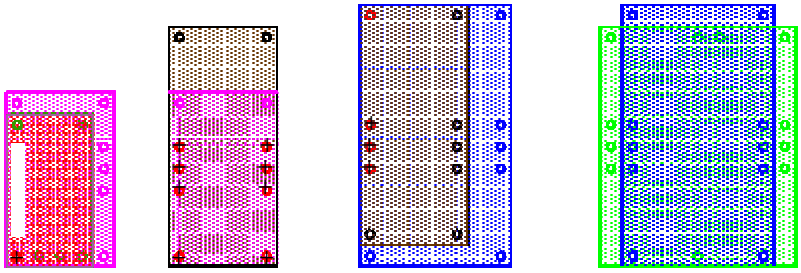
PR217
Virtex™-II Design 1
Module-based (PTHxxxx series) Power Management Solution Providing I_{CCINT} = 6 A from V_{IN} = 3.3 V

FEATURES:

- Simple to use plug-in modules enables fast time-to-market
- High efficiency minimizes heat
- Interchange modules to support
  - 6A to 30A load currents
  - If current requirements decrease, easy to use dual footprints allow cost reduction without redesign



  - 3.3V, 5V, or 12V input supply
- High UVLO trip point and integrated soft-start (5 ms fixed for the PTH03000) of the PTH series modules eliminates the need for an external Supply Voltage Supervisor (SVS) to monitor the input rail.
- If the Auto-track™ (sequencing) feature of the PTH series modules is desired, please refer to Virtex-II Design 3 (PR221 for Sequential Sequencing or PR251 for Simultaneous Sequencing).
- The design meets Xilinx's V_{CCINT} and V_{CCO} start-up profile requirements, where applicable, including monotonic voltage ramp, in-rush current and power voltage ramp time requirements.

IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at http://www.ti.com/xilinxfpga for more information and other reference designs.
- Link to datasheet at http://focus.ti.com/lit/ds/symlink/pth03000w.pdf

IMPLEMENTATION NOTES:

- **Additional Capacitance:**
  - The PTH03000 input capacitance requirement may change depending on the application. See the minimum input capacitance required at the bottom

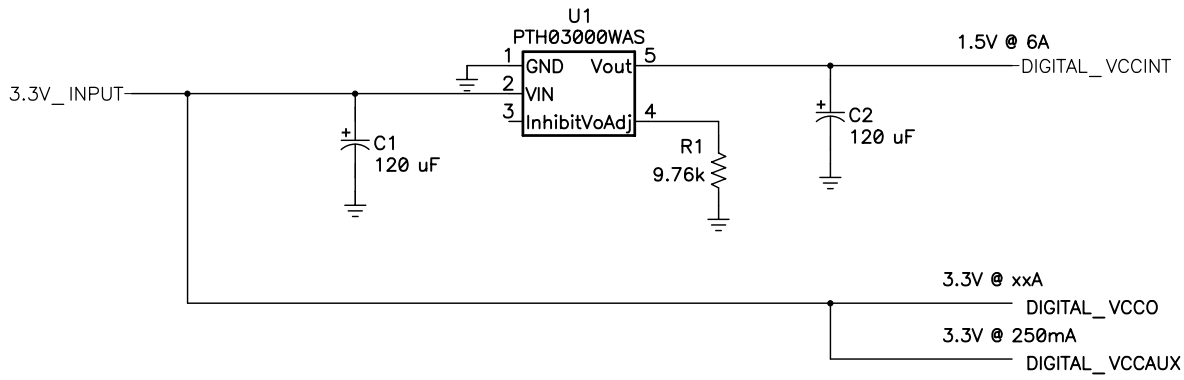
of page 3, the computation for determining input capacitance on page 5 as well as recommended capacitors on page 6 of the datasheet.

- The PTH03000 device has a limitation to the amount and type of additional capacitance that can be added to its output. See the specifications for external output capacitance and associated ESR at the bottom of page 3 as well as the application note (including recommended output caps) on pages 5-6 of the datasheet.

- **V_{CCAUX}:** V_{CCAUX} powers time-critical resources in the FPGA, including the Digital Clock Managers (DCMs). Therefore, this supply voltage is especially susceptible to power supply noise. V_{CCAUX} can share a power plane with V_{CCO}, but only if V_{CCO} does not have excessive noise. Changes in V_{CCAUX} voltage beyond 200 mV peak-to-peak should take place no faster than 10 mV per milli-second.

QUESTIONS?

- Send an email to mailto:**fpgasupport@list.ti.com**



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Date: 04/22/2004

PR217 BOM

COUNT	RefDes	DESCRIPTION	SIZE	MFR	PART NUMBER
2	C1, C2	Capacitor, Tantalum, 120-uF, 10-V, 140-milliohm, 20%	7343 (D)	Vishay	593D127X0010D2T35
1	R1	Resistor, Chip, 9.76k-Ohms, 1/16-W, 1%	603	Std	Std
1	U1	Module Module, Wide Output Adj, 6A, 0.9V to 2.5V, 3.3V Input	0.745 x 0.495	TI	PTH03000WAS

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