

TIDA- 00140

***XGA digital video SerDes 18bit to 24bit Upscaler Solution for Automotive TFT
LCD Displays - Test Data***

This document shares the test results of the DS90UR916 DEMO. Results provided are the Eye Diagram.

Eye Diagram

The test data shown illustrates the quality of the differential signal received by the FPD-Link II deserializer. The FPD-Link II signal is transmitted by the serializer over the shielded twisted pair cable, and the signal quality enhanced by the built-in equalizer within the deserializer. The eye diagram is measured at the CMLOUT test-point offering a view of the internally equalized differential signal. The CMLOUT test point should always be used to measure the quality of the differential signal to include the effect of the adaptive equalizer. The CMLOUT is enabled via I2C register control.

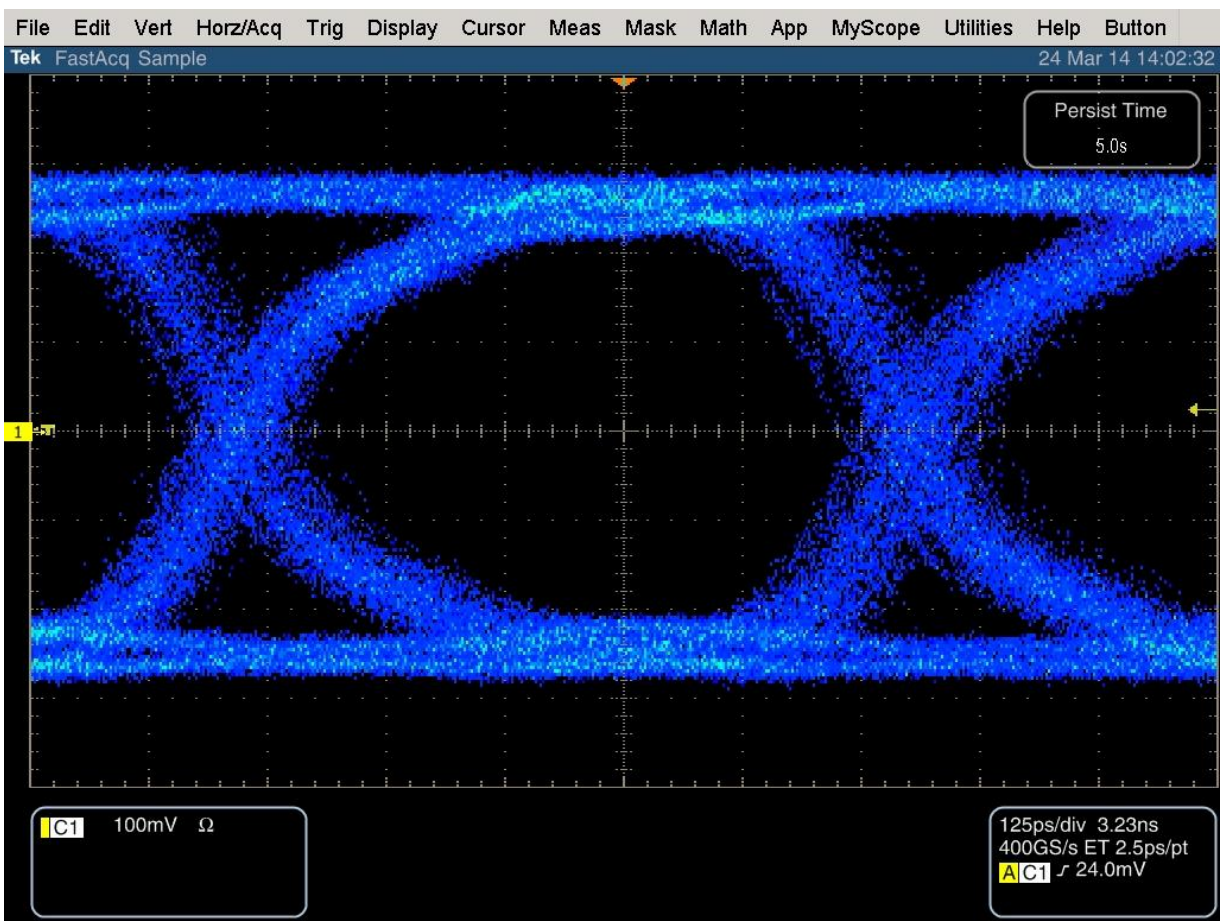


Figure 1. Eye diagram for DS90UR916. Clock speed was 50Mhz

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