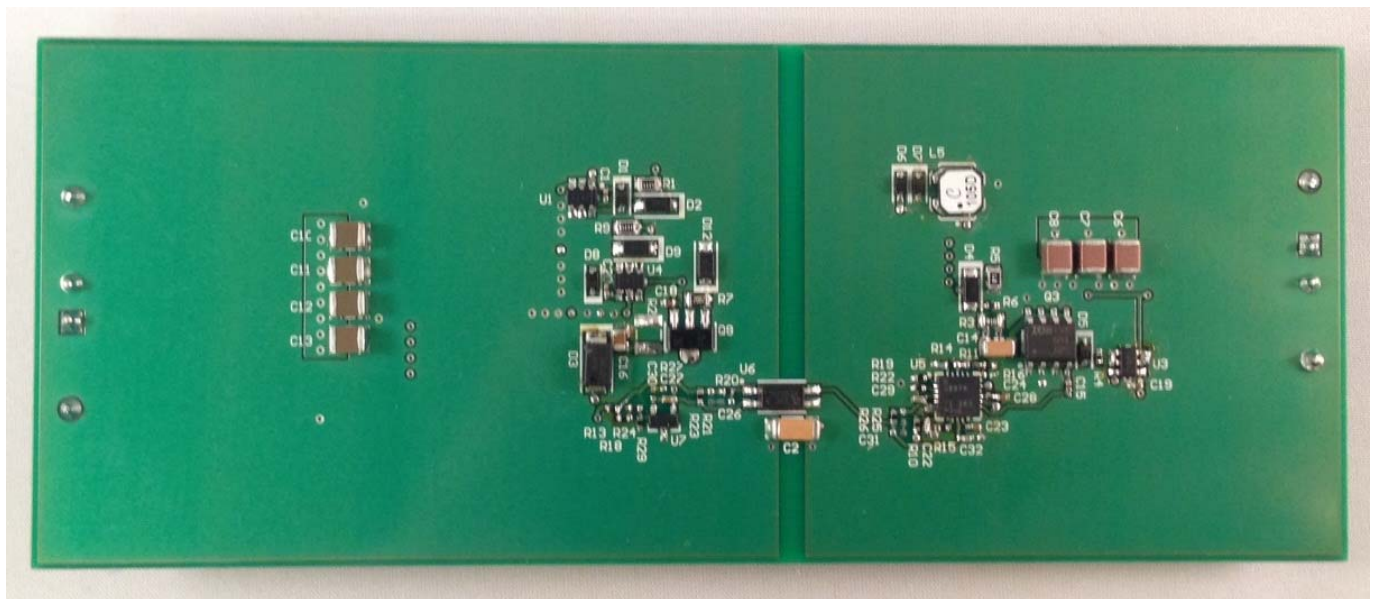
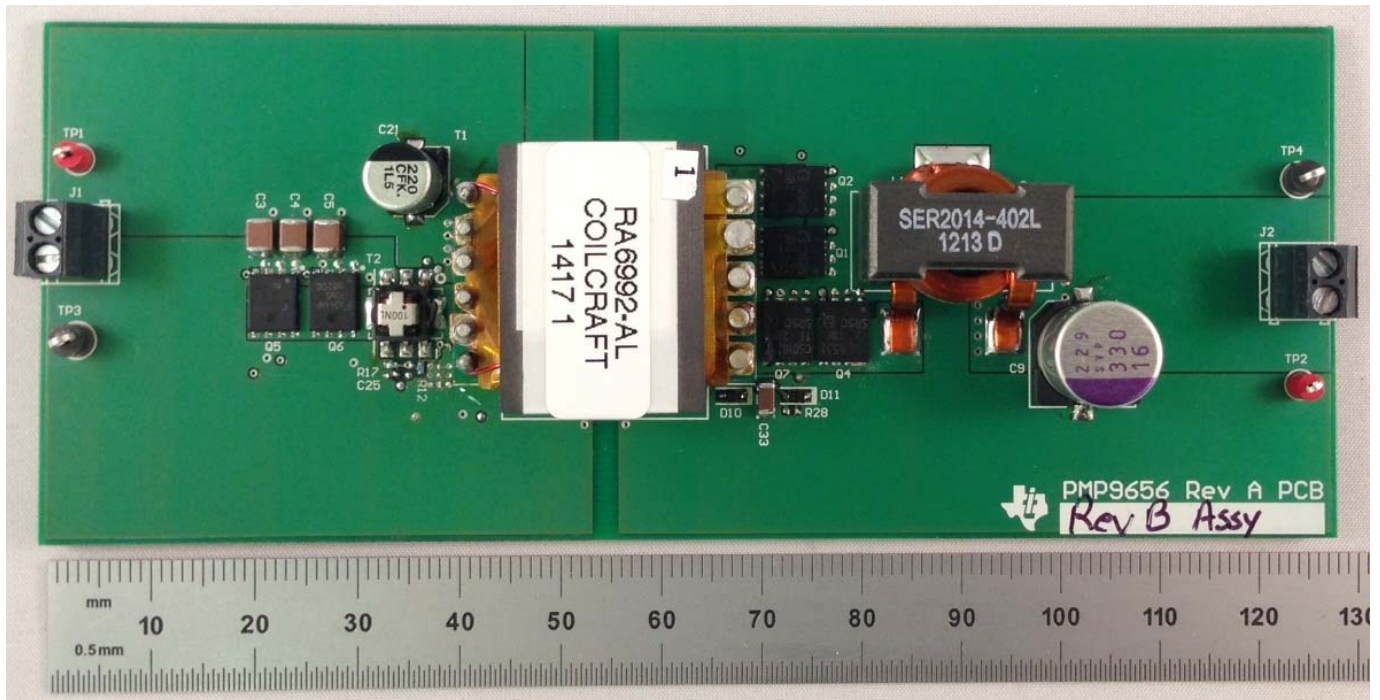
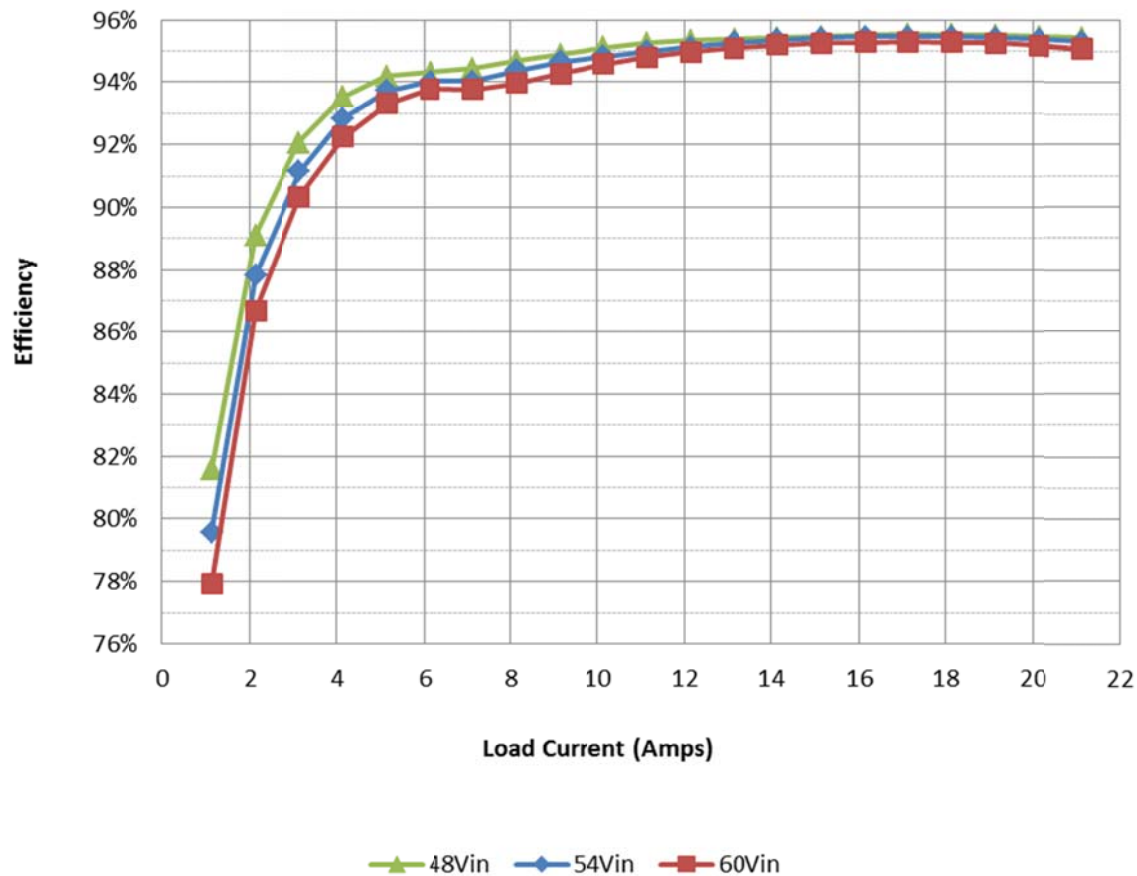


## 1 Photos

The circuit was built using a PMP9656 Rev A PCB.



## 2 Efficiency



Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.002	12.07	48.0	0.065	0.02	3.077	0.7%
1.143	12.07	48.0	0.353	13.80	3.119	81.6%
2.145	12.07	48.0	0.605	25.89	3.163	89.1%
3.148	12.07	48.0	0.860	37.99	3.277	92.1%
4.149	12.07	48.0	1.116	50.07	3.468	93.5%
5.15	12.07	48.0	1.375	62.18	3.829	94.2%
6.15	12.07	48.0	1.641	74.25	4.481	94.3%
7.16	12.07	48.0	1.905	86.36	5.079	94.4%
8.16	12.07	48.0	2.166	98.44	5.516	94.7%
9.16	12.07	48.0	2.428	110.54	5.951	94.9%
10.16	12.07	48.0	2.687	122.63	6.286	95.1%
11.16	12.07	48.0	2.946	134.68	6.693	95.3%
12.16	12.07	48.0	3.207	146.75	7.156	95.4%
13.16	12.07	48.0	3.470	158.83	7.681	95.4%
14.16	12.07	48.0	3.733	170.93	8.205	95.4%
15.16	12.07	48.0	3.995	183.00	8.699	95.5%
17.16	12.07	48.0	4.516	207.08	9.651	95.5%
18.17	12.07	48.0	4.781	219.20	10.253	95.5%
19.17	12.07	48.0	5.045	231.27	10.857	95.5%
20.17	12.07	48.0	5.311	243.36	11.536	95.5%
21.17	12.07	48.0	5.578	255.44	12.249	95.4%

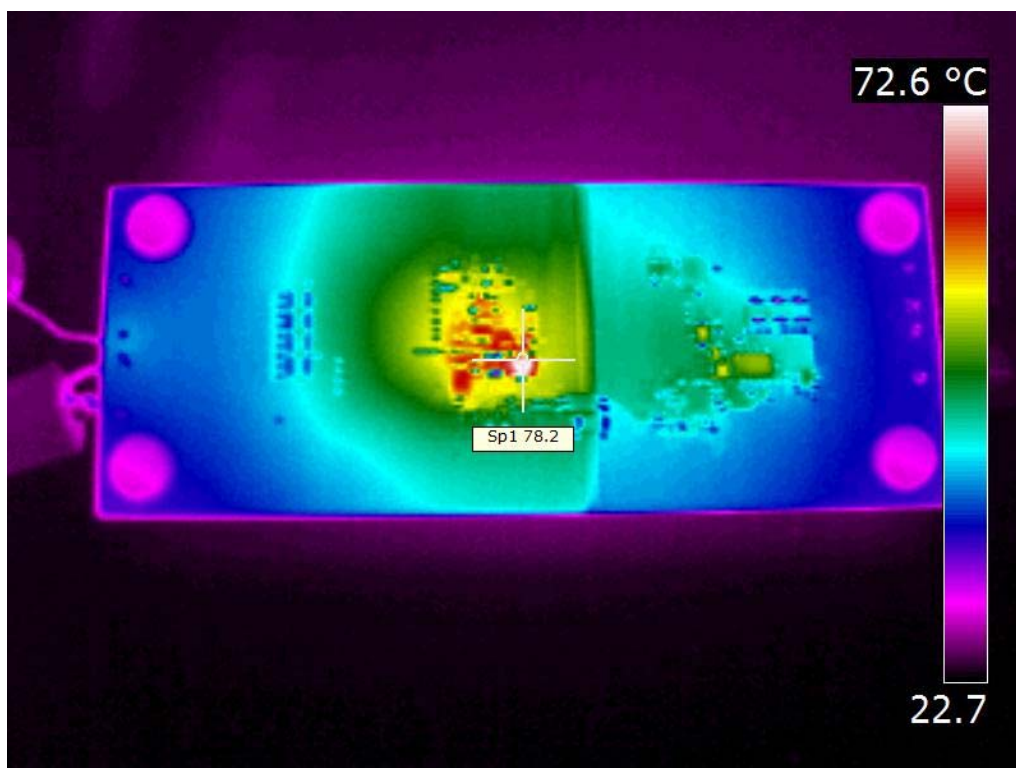
## PMP9656 Rev B Test Results

lout	Vout	Vin	lin	Pout	Losses	Efficiency
0.002	12.09	54.0	0.066	0.03	3.531	0.8%
1.148	12.08	54.0	0.323	13.88	3.560	79.6%
2.150	12.08	54.0	0.548	25.97	3.602	87.8%
3.152	12.08	54.0	0.774	38.08	3.707	91.1%
4.152	12.08	54.0	1.001	50.17	3.874	92.8%
5.16	12.08	54.0	1.231	62.27	4.178	93.7%
6.15	12.08	54.0	1.464	74.34	4.720	94.0%
7.16	12.08	54.0	1.703	86.45	5.487	94.0%
8.16	12.08	54.0	1.934	98.54	5.864	94.4%
9.16	12.08	54.0	2.165	110.63	6.245	94.7%
10.16	12.08	54.0	2.397	122.72	6.688	94.8%
11.16	12.08	54.0	2.628	134.77	7.109	95.0%
12.16	12.07	54.0	2.859	146.84	7.488	95.1%
13.16	12.07	54.0	3.090	158.93	7.882	95.3%
14.16	12.07	54.0	3.322	171.02	8.314	95.4%
15.16	12.07	54.0	3.554	183.09	8.783	95.4%
16.16	12.07	54.0	3.786	195.14	9.277	95.5%
17.16	12.07	54.0	4.021	207.23	9.834	95.5%
18.17	12.07	54.0	4.255	219.31	10.421	95.5%
19.16	12.07	54.0	4.491	231.37	11.071	95.4%
20.17	12.07	54.0	4.727	243.44	11.780	95.4%
21.17	12.07	54.0	4.965	255.51	12.564	95.3%

lout	Vout	Vin	lin	Pout	Losses	Efficiency
0.003	12.09	60.0	0.066	0.04	3.918	1.1%
1.149	12.09	60.0	0.297	13.89	3.936	77.9%
2.150	12.09	60.0	0.500	25.99	3.992	86.7%
3.152	12.09	60.0	0.703	38.10	4.076	90.3%
4.152	12.09	60.0	0.907	50.18	4.223	92.2%
5.15	12.08	60.0	1.113	62.29	4.470	93.3%
6.15	12.08	60.0	1.322	74.36	4.929	93.8%
7.16	12.08	60.0	1.537	86.47	5.753	93.8%
8.16	12.08	60.0	1.748	98.55	6.326	94.0%
9.16	12.08	60.0	1.956	110.64	6.720	94.3%
10.16	12.08	60.0	2.163	122.73	7.027	94.6%
11.157	12.08	60.0	2.370	134.78	7.384	94.8%
12.157	12.08	60.0	2.577	146.85	7.757	95.0%
13.159	12.08	60.0	2.786	158.94	8.178	95.1%
14.160	12.08	60.0	2.995	171.03	8.626	95.2%
15.160	12.08	60.0	3.204	183.09	9.122	95.3%
16.158	12.08	60.0	3.414	195.14	9.674	95.3%
17.16	12.08	60.0	3.625	207.22	10.228	95.3%
18.16	12.08	60.0	3.837	219.29	10.855	95.3%
19.16	12.08	60.0	4.049	231.36	11.524	95.3%
20.16	12.07	60.0	4.264	243.43	12.312	95.2%
21.16	12.07	60.0	4.480	255.50	13.202	95.1%

### 3 Thermal

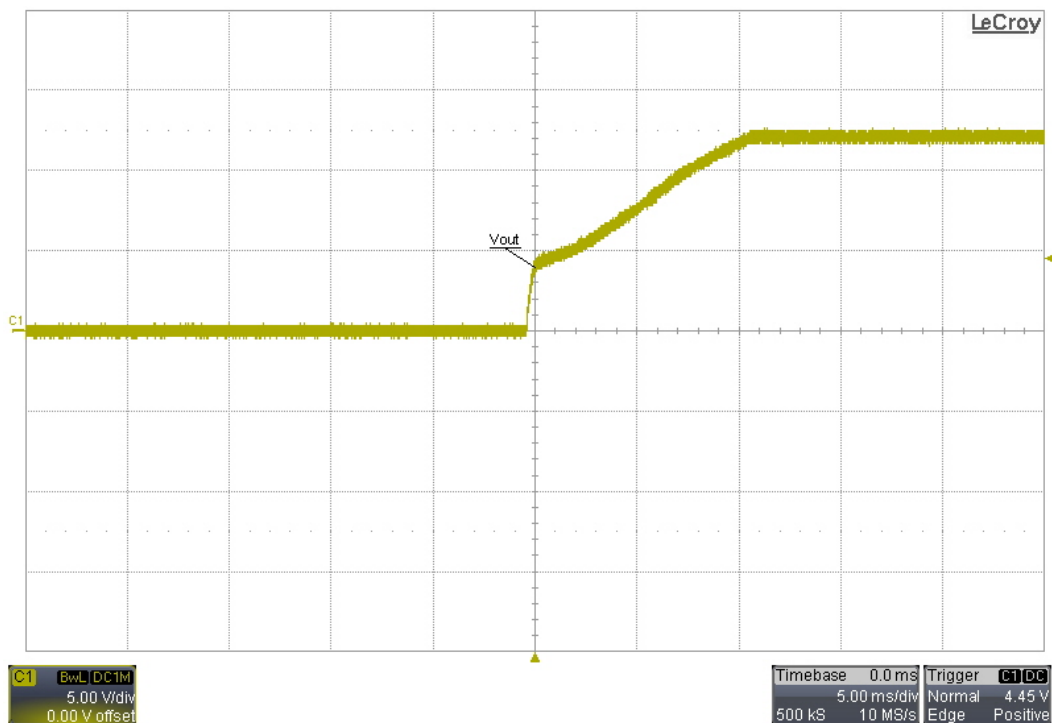
The thermal images below show the circuit board with a 54V input and 21A load. The ambient temperature was 25C and the air flow rate was approximately 200lfm (1m/s).



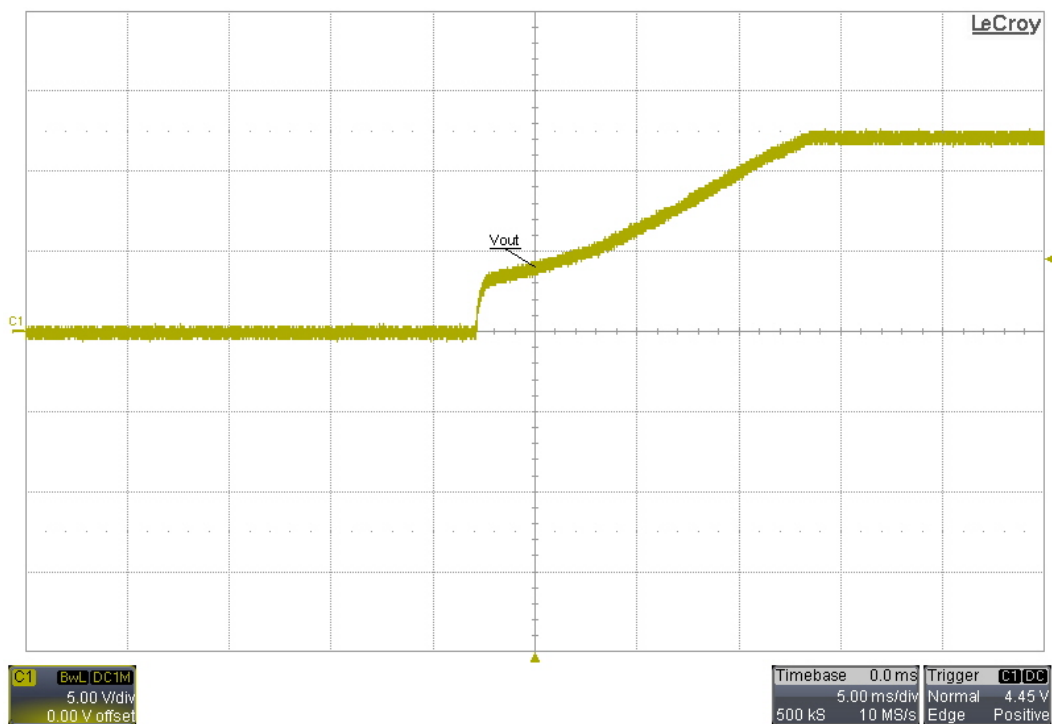


## 4 Startup

### 4.1 54V Input, No Load

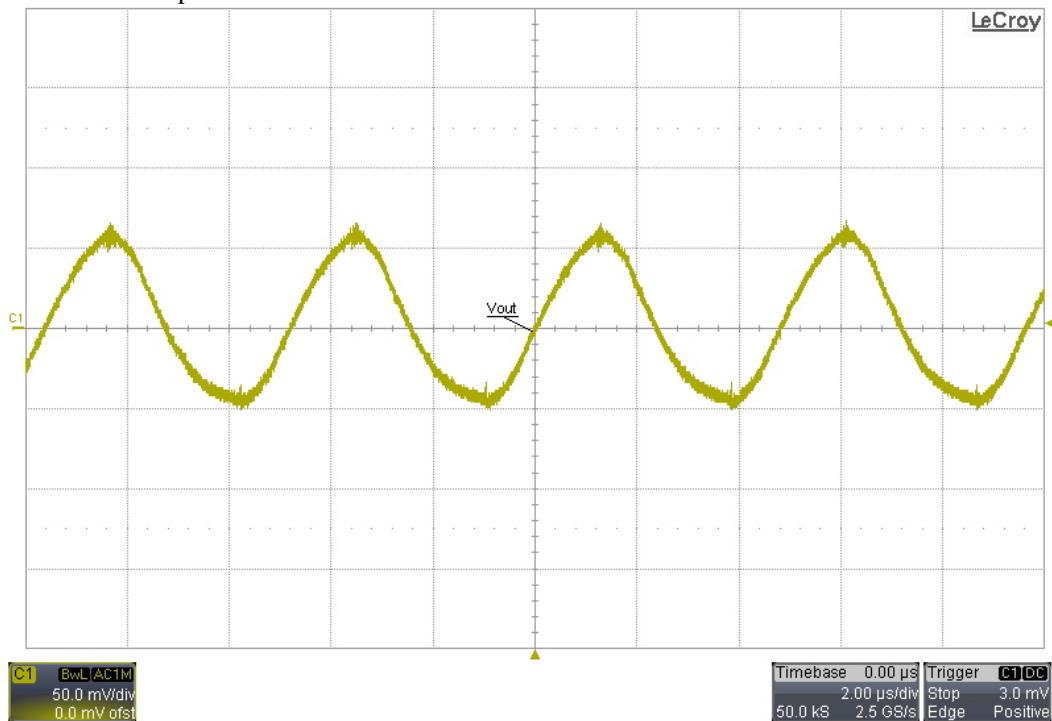


### 4.2 54V Input, 1Ω Load



## 5 Output Ripple Voltage

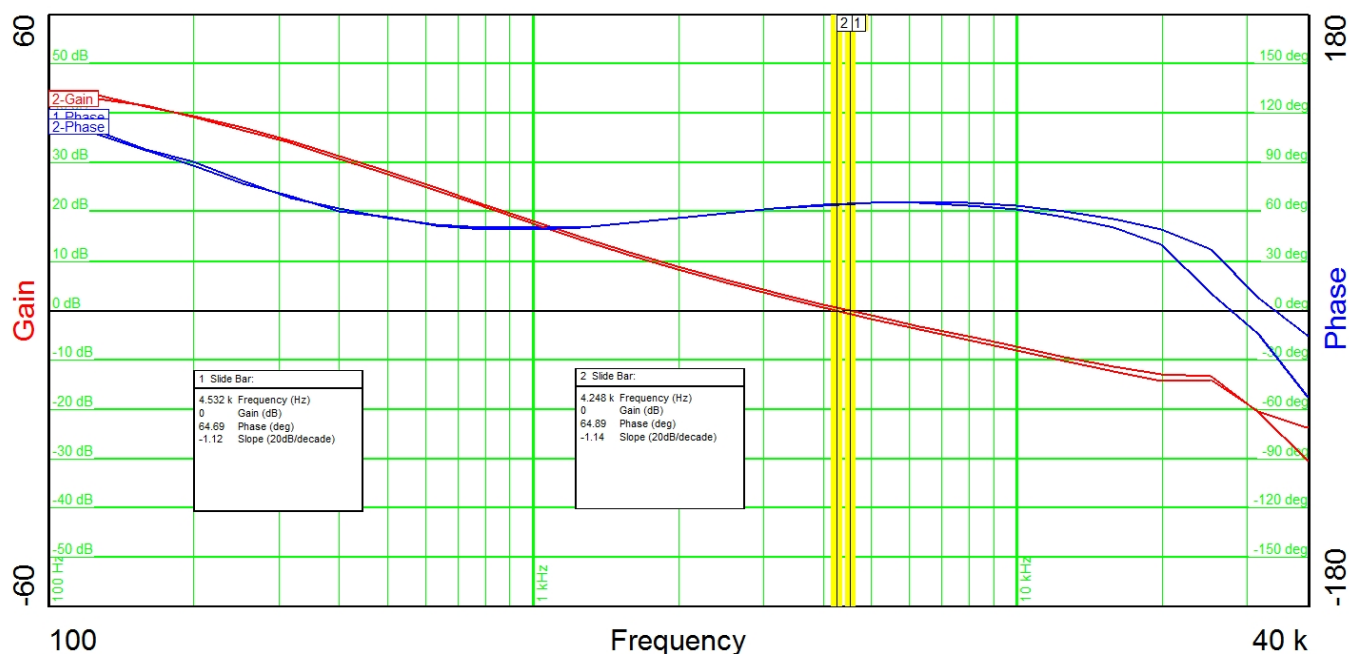
The input was 54V and the output was loaded with 21A.



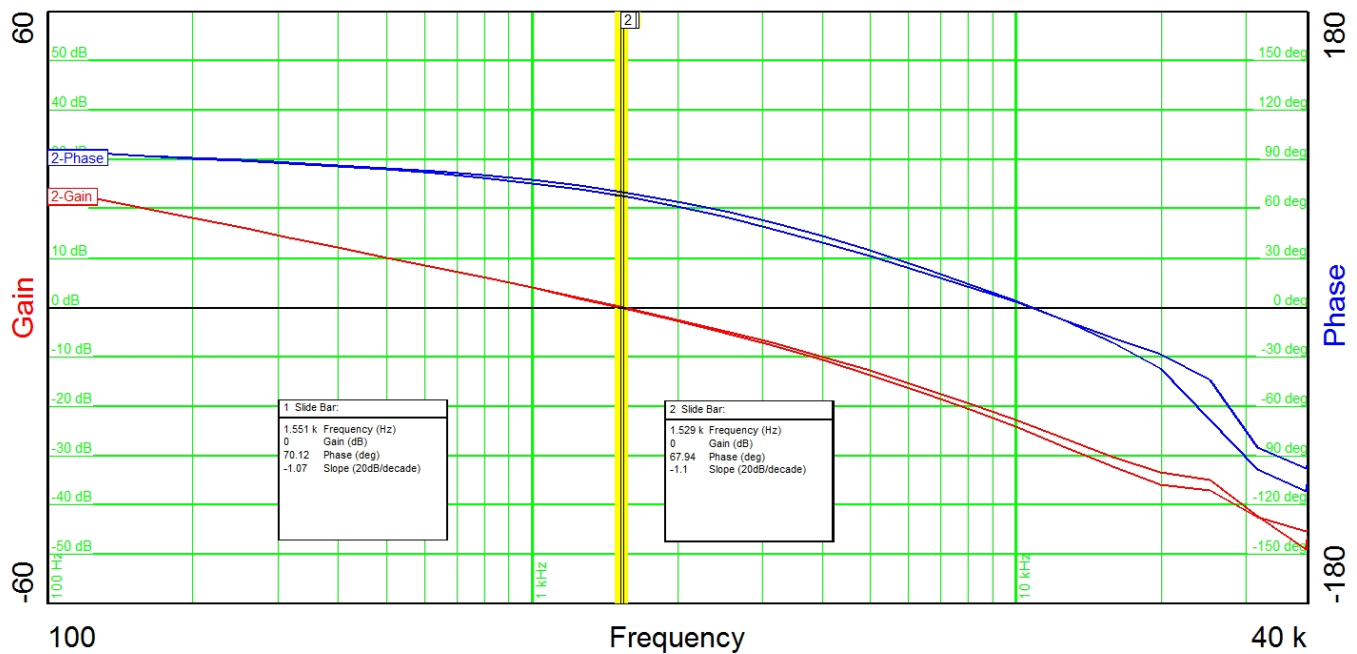
## 6 Frequency Response

The output was loaded with 21A. For gain/phase plot #1, the input was 48V. For gain/phase plot #2, the input was 60V.

### 6.1 Loop Broken at R13



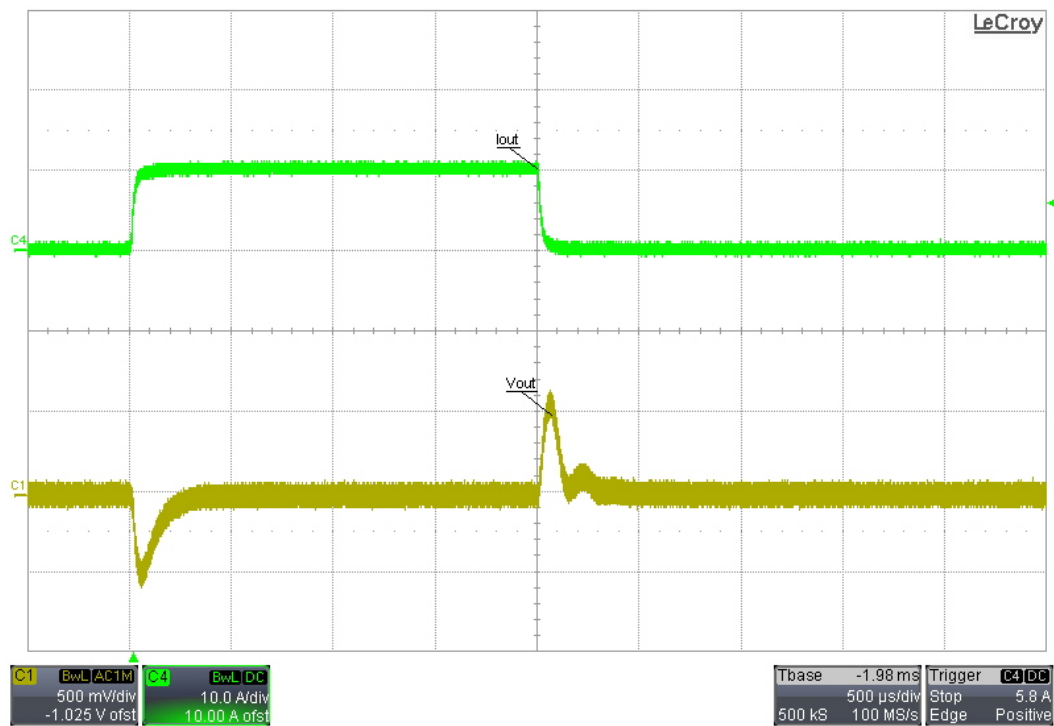
## 6.2 Loop Broken at R18



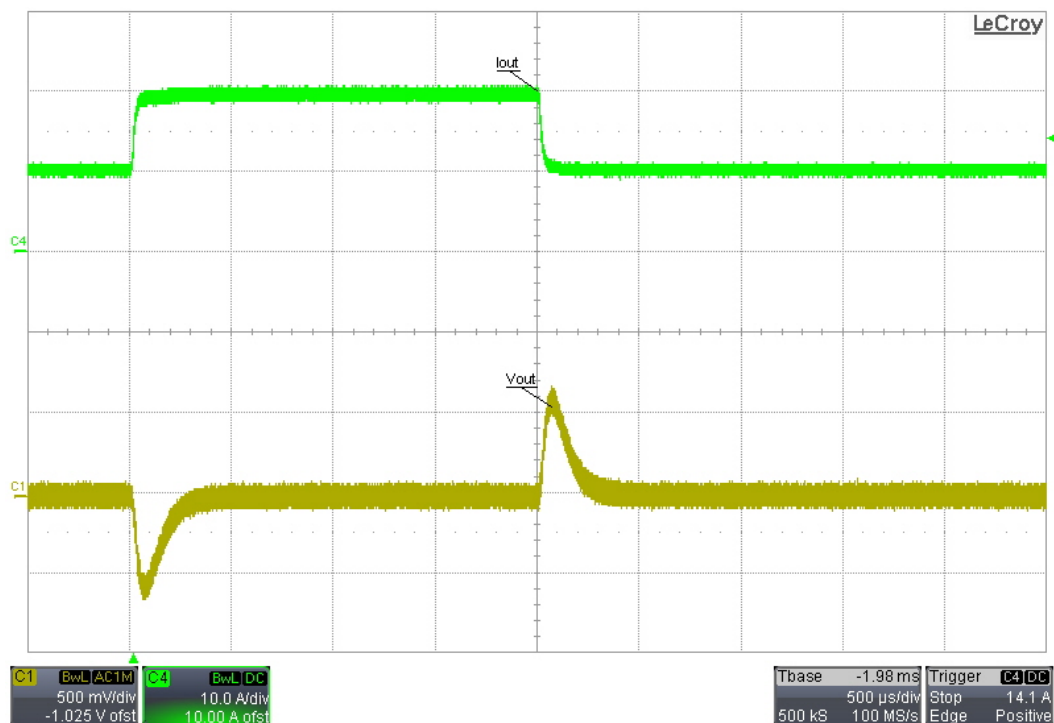
## 7 Load Transients

The input was set to 54V.

### 7.1 0A to 10A

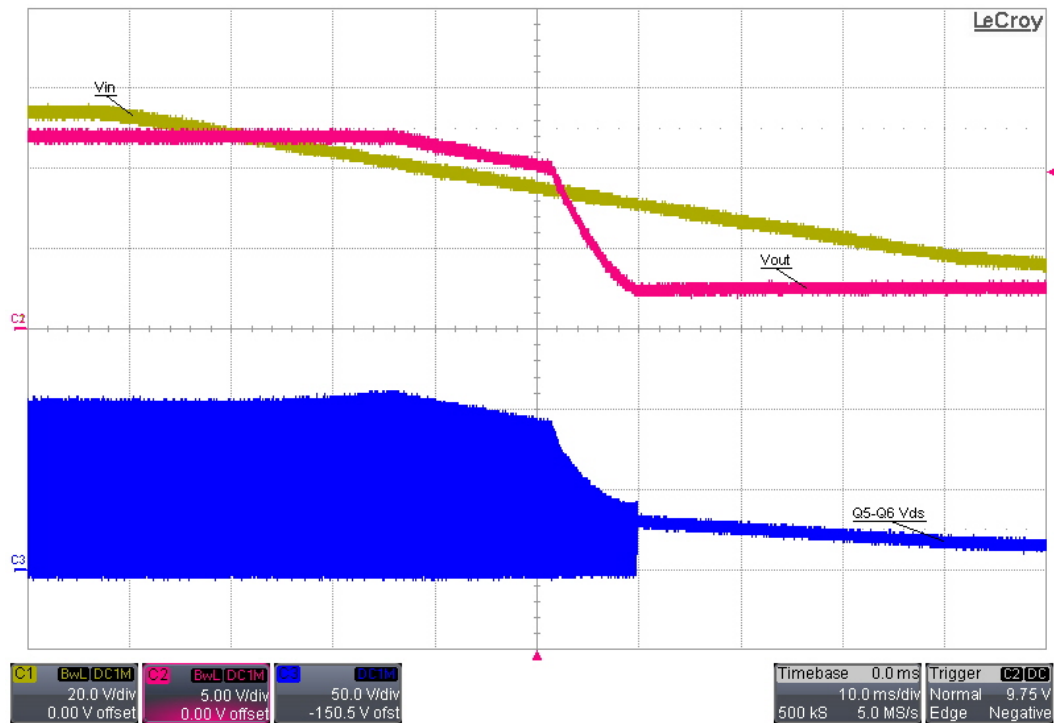


## 7.2 10A to 20A



## 8 Shutdown

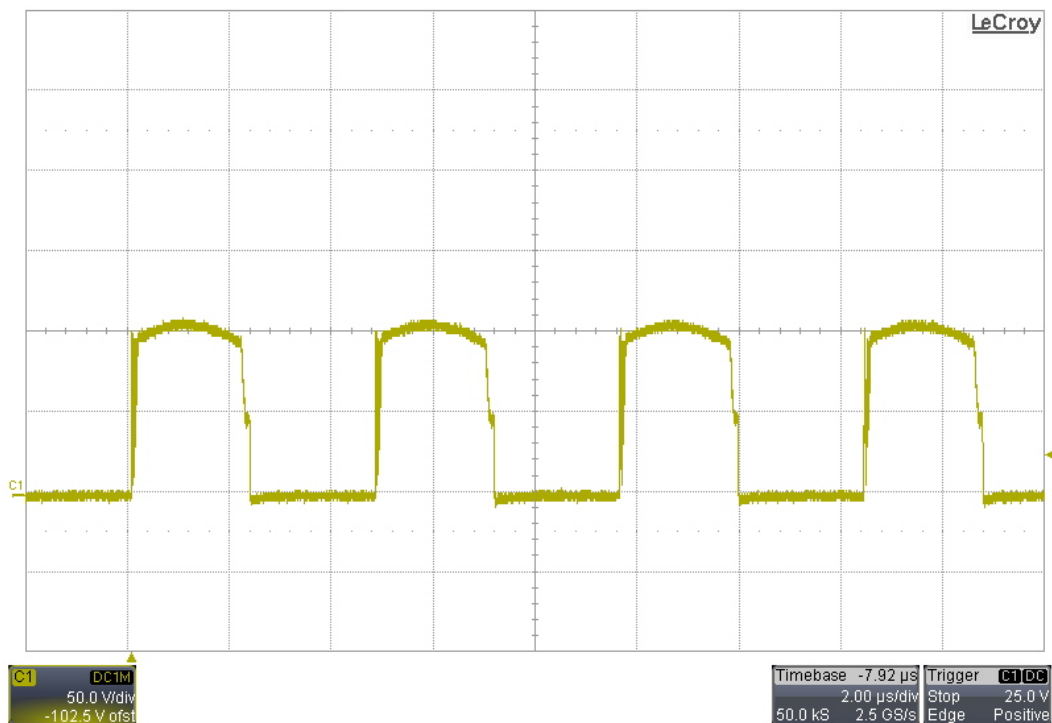
The output was unloaded.



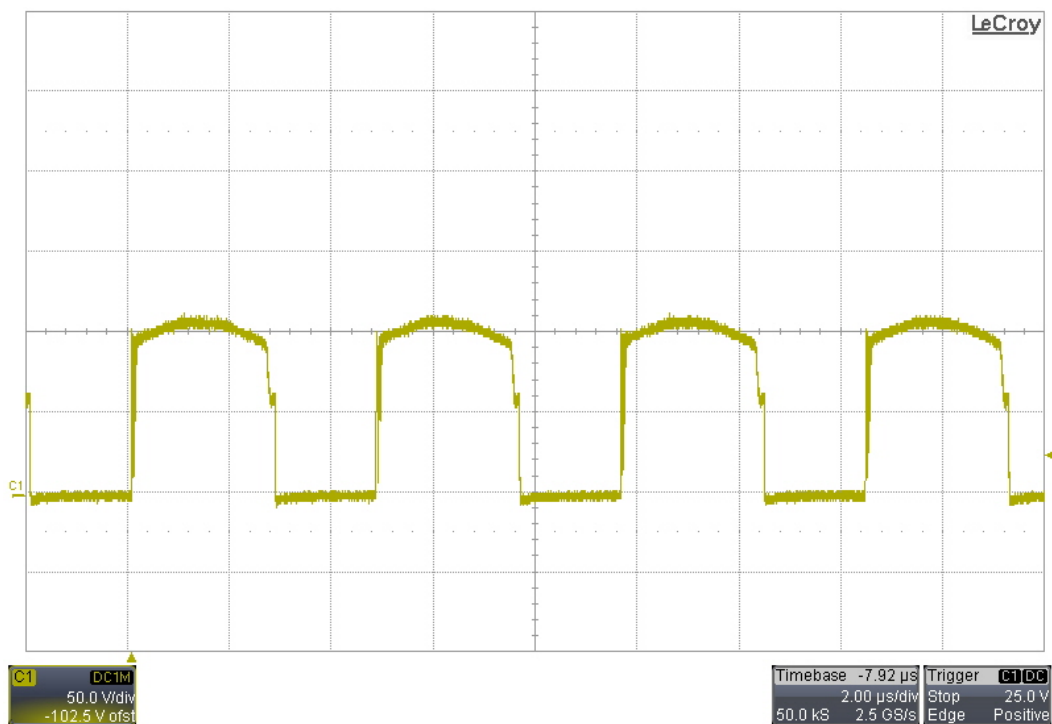


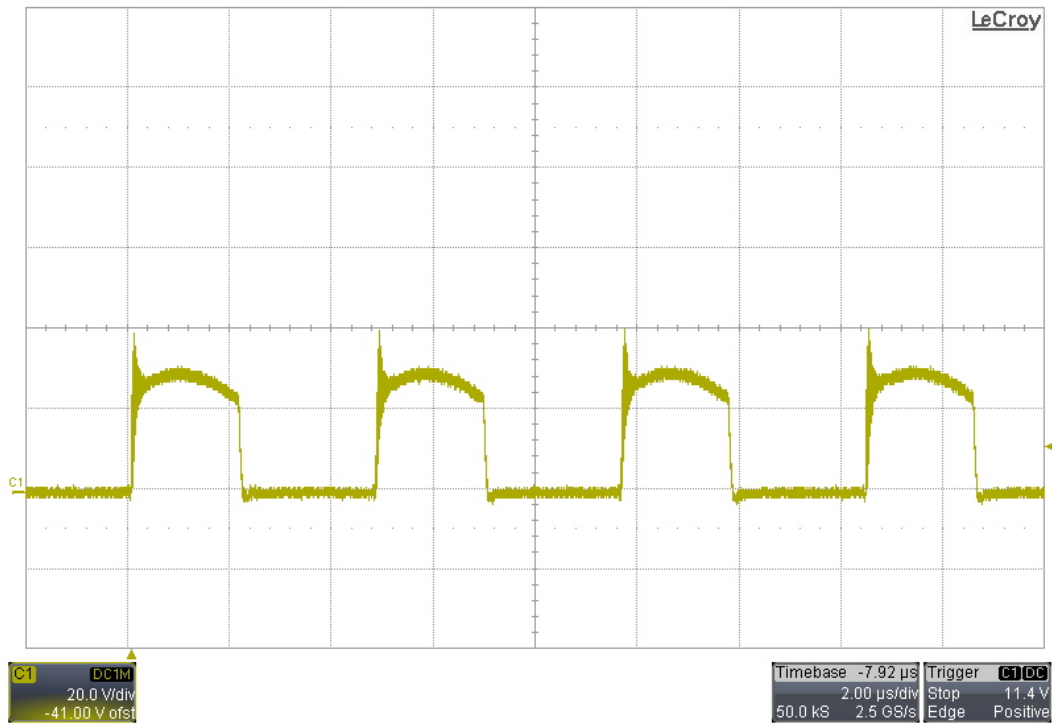
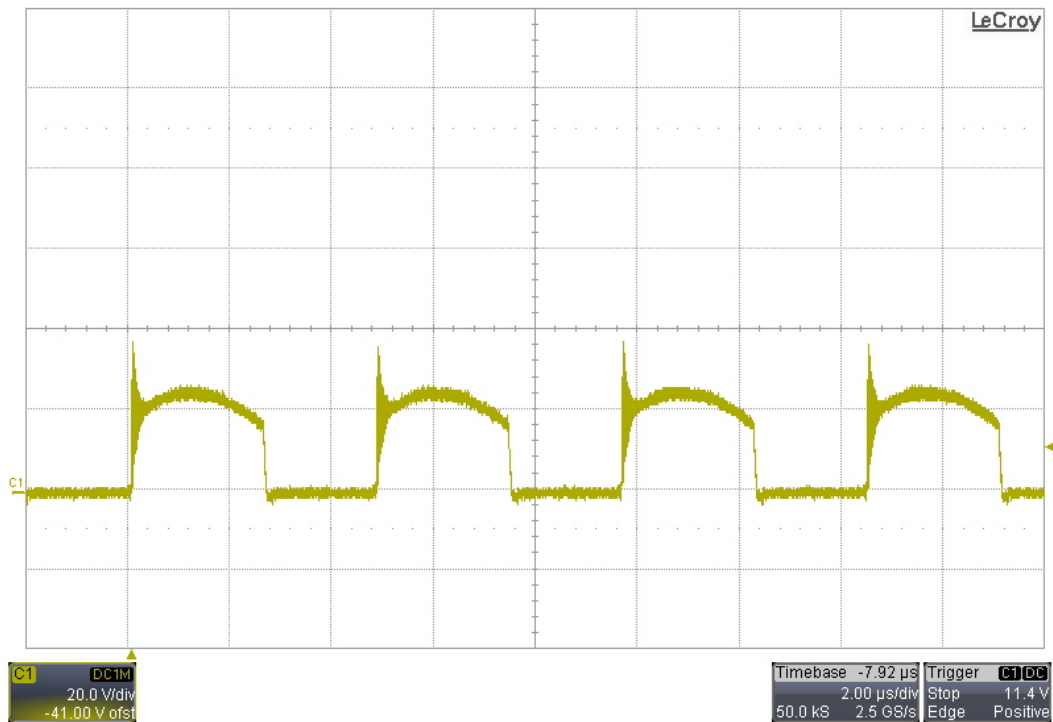
## 9 Switching Waveforms

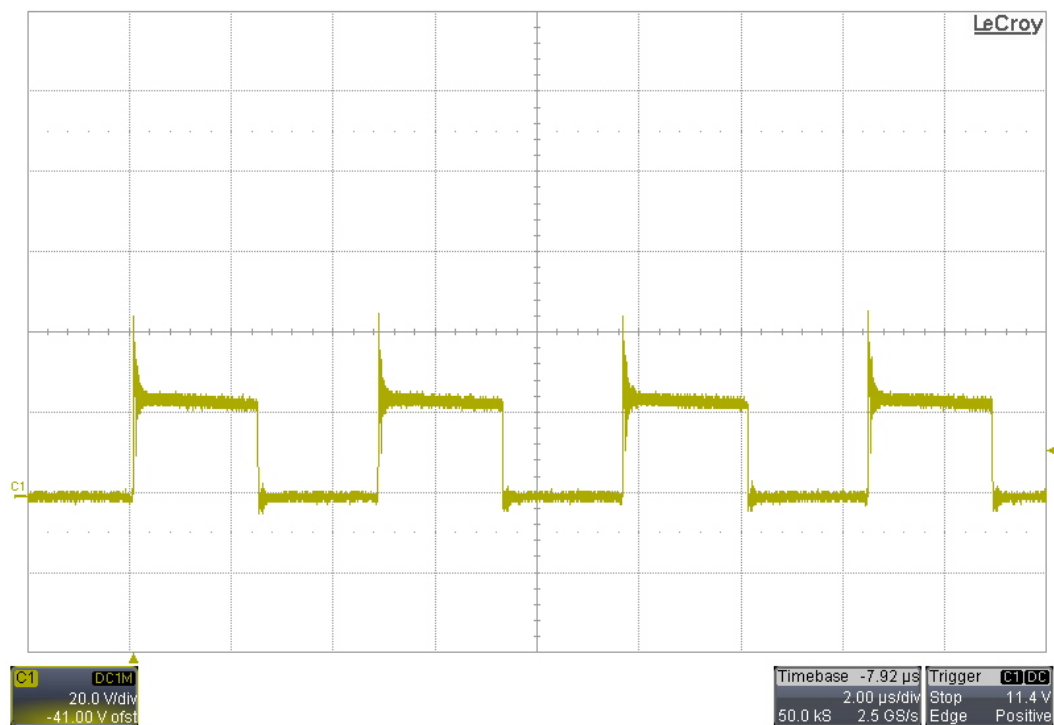
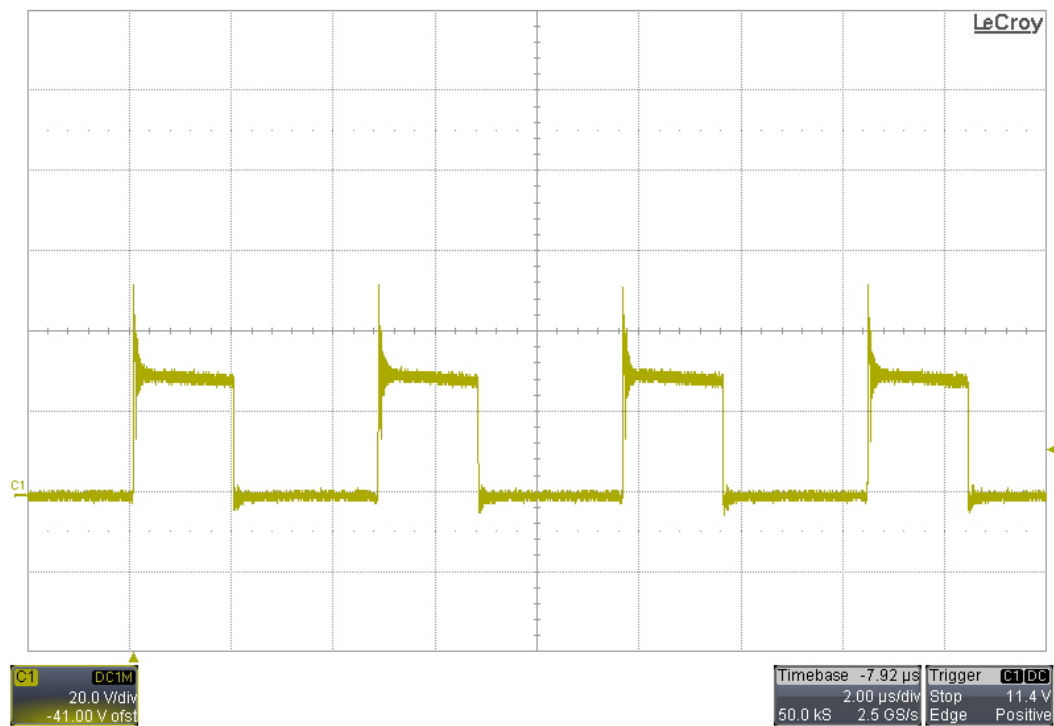
### 9.1 Primary FETs $V_{ds}$ (Q5 and Q6) – 48Vin, 21A Load



### 9.2 Primary FETs $V_{ds}$ (Q5 and Q6) – 60Vin, 21A Load



**9.3 Sync FETs Vds (Q1 and Q2) – 48Vin, 21A Load****9.4 Sync FETs Vds (Q1 and Q2) – 60Vin, 21A Load**

**9.5 Sync FETs Vds (Q4 and Q7) – 48Vin, 21A Load****9.6 Sync FETs Vds (Q4 and Q7) – 60Vin, 21A Load**

## IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer's systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER'S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer's safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have **not** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.