48V Input 3.3V/30A with Output Pre-bias

(ACTIVE) PMP5997

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Description

This reference design generates a 3.3V/100W output from a standard 48V telecom input and allows for a pre-biased output. The UCC2897A controls operation of the active clamp power stage. The drive signal for the synchronous rectifiers is sent to the secondary side through an ISO7220 digital isolator. This drive signal is blanked out during startup to allow for a pre-biased output. This design achieves efficiencies over 92% and is built on a standard ¼ brick footprint.

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Top view

Fully assembled board (shown above) developed for testing and performance validation only, not available for sale.

Bill of Materials (BOM)

Find the complete list of components in this reference design.

Download BOM

Parametrics

	PMP5997
Vin (Max) (V)	72
Vin (Min) (V)	36
Vout (Nom) (V)	3.3
Iout (Max) (A)	30
Output Power	99
Isolated/Non-Isolated	Isolated
Input Type	DC
Topology	Forward- Active Clamp Forward- Synchronous

TI Devices (5)

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Part Number	Name	Product Family	Sample & Buy	Design Kits & Evaluation Modules
ISO7220M	Dual Channel, 2/0, 150Mbps Digital Isolator	Isolator	Sample & Buy	View Design Kits & Evaluation Modules
TL331	Single Differential Comparator	Amplifiers and Linear	Sample & Buy	Not Available

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CAD/CAE symbols

Part #	Package | Pins	CAD File (.bxl)	STEP Model (.stp)
ISO7220M	SOIC (D) | 8	Download	Download
TL331	SOT (DBV) | 5	Download	Download
TPS28225	SOIC (D) | 8	Download	Download
	VSON (DRB) | 8	Download	-
UCC2897A	TSSOP (PW) | 20	Download	Download
	VQFN (RGP) | 20	Download	-

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Technical Documents

User Guides (1)

Title	Abstract	Type	Size (KB)	Date	Views
PMP5997 Test Results		PDF	2860	16 Aug 2011	34

Design Files (2)

Title	Abstract	Type	Size (KB)	Date	Views
PMP5997 BOM		PDF	64	04 Aug 2011	47
PMP5997 Schematic		PDF	131	04 Aug 2011	65

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