AN3383
Application note

STA350BW 2.0-channel demonstration board

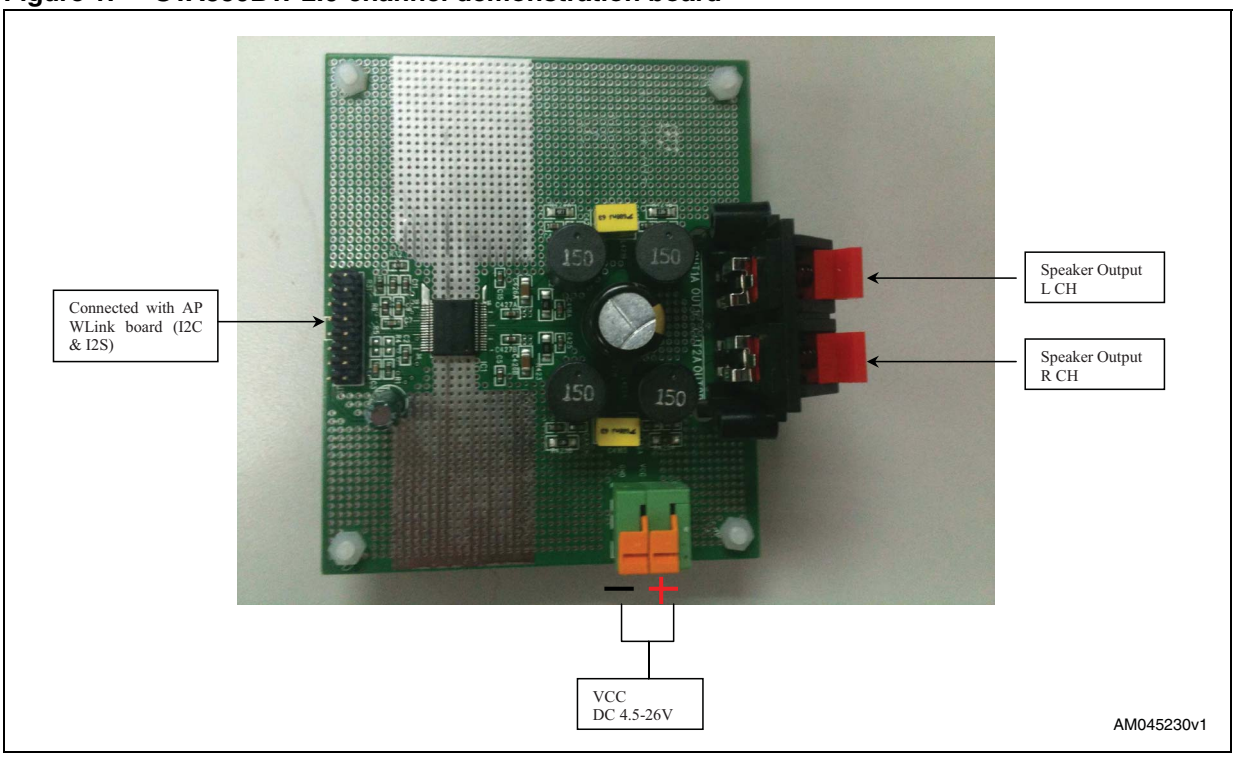
Introduction

The purpose of this application note is to describe:

- how to connect the STA350BW 2.0-channel demonstration board
- how to evaluate the demonstration board performance with all the electrical curves
- how to avoid critical issues in the PCB schematic and layout of the the STA350BW

The STA350BW demonstration board is specifically configured for 2.0 BTL channels, releasing up to 2 x 50 W into 6 ohm of power output at 25 V of supply voltage using reduced components. It is a complete solution for the digital audio power amplifier.

Figure 1. STA350BW 2.0-channel demonstration board



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1 Functional description of the demonstration board

The following terms used in this application note are defined as follows:

- THD+N vs. Freq: Total harmonic distortion plus noise versus frequency curve
- THD+N vs. Pout: Total Harmonic Distortion (THD) plus noise versus output power
- S/N ratio: Signal-to-noise ratio
- FFT: Fast Fourier Transform Algorithm (method)
- CT: Channel separation L to R, or R to L channel crosstalk

The equipment used includes the following:

- Audio Precision (System 2700) by AP Co., USA)
- DC power supply (4.5 V to 26 V)
- Digital oscilloscope (TDS3034B by Tektronix)
- PC (with APWorkbench GUI control software installed)

1.1 Connections

Power supply signal and interface connection

1. Connect the positive voltage of 24V DC power supply to the +Vcc pin and negative to GND.
2. Connect the APWorkbench board to the J1 connector of the STA350BW demonstration board.
3. Connect the S/PDIF signal cable to the RCA jack on the APWLink board, connecting to the signal source such as Audio precision or DVD player.

Note: The voltage range of the DC power supply for V_{CC} is 4.5 V to 26 V.

1.2 Output configuration

The STA350BW demo board is specifically configured in 2 BTL channels. For the software setup, please refer to the APWUserManualR1.0.pdf.

1.3 Schematic and block diagrams, PCB layout, bill of material

Figure 2. Schematic diagram

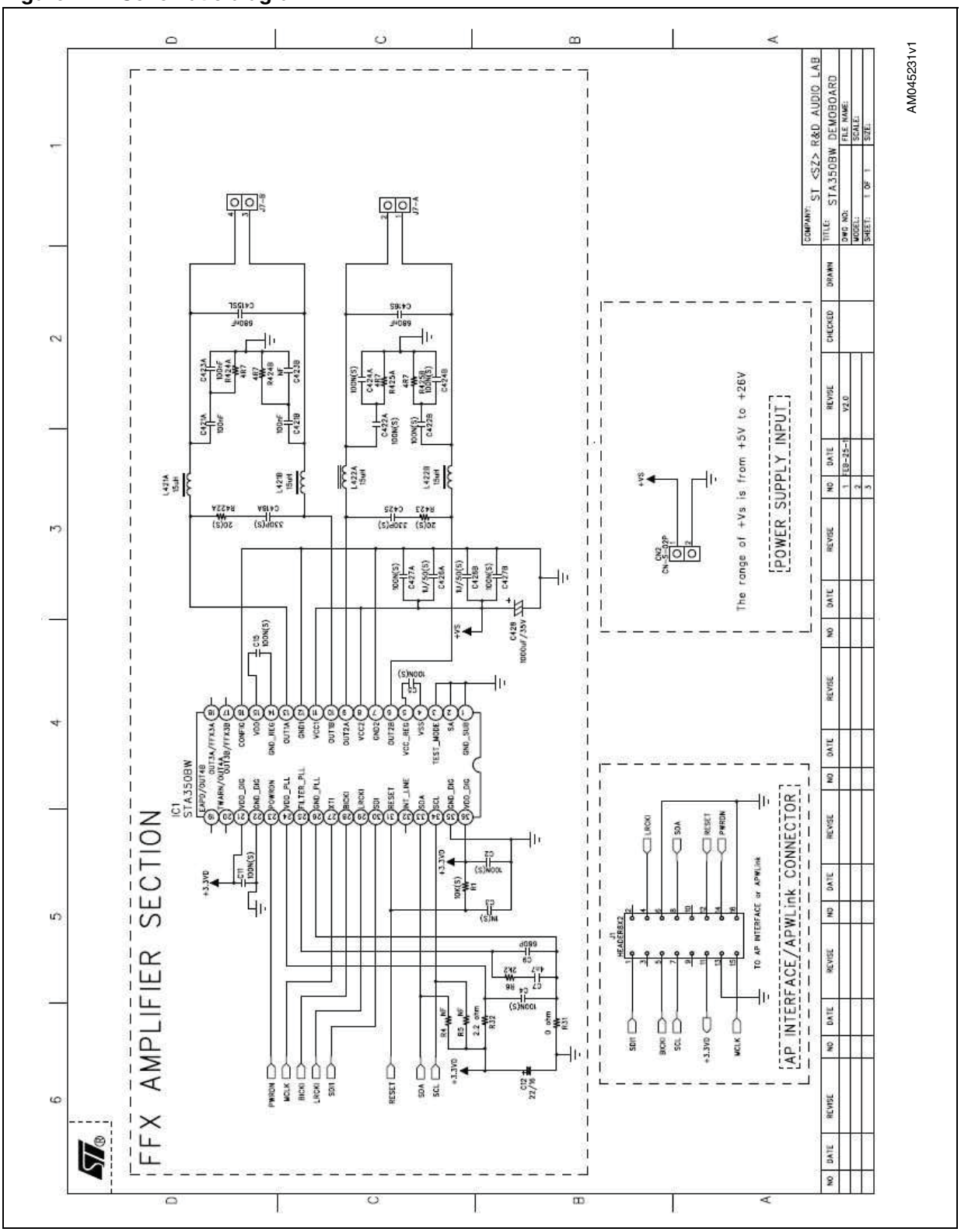


Figure 3. Block diagram of test connections with equipment

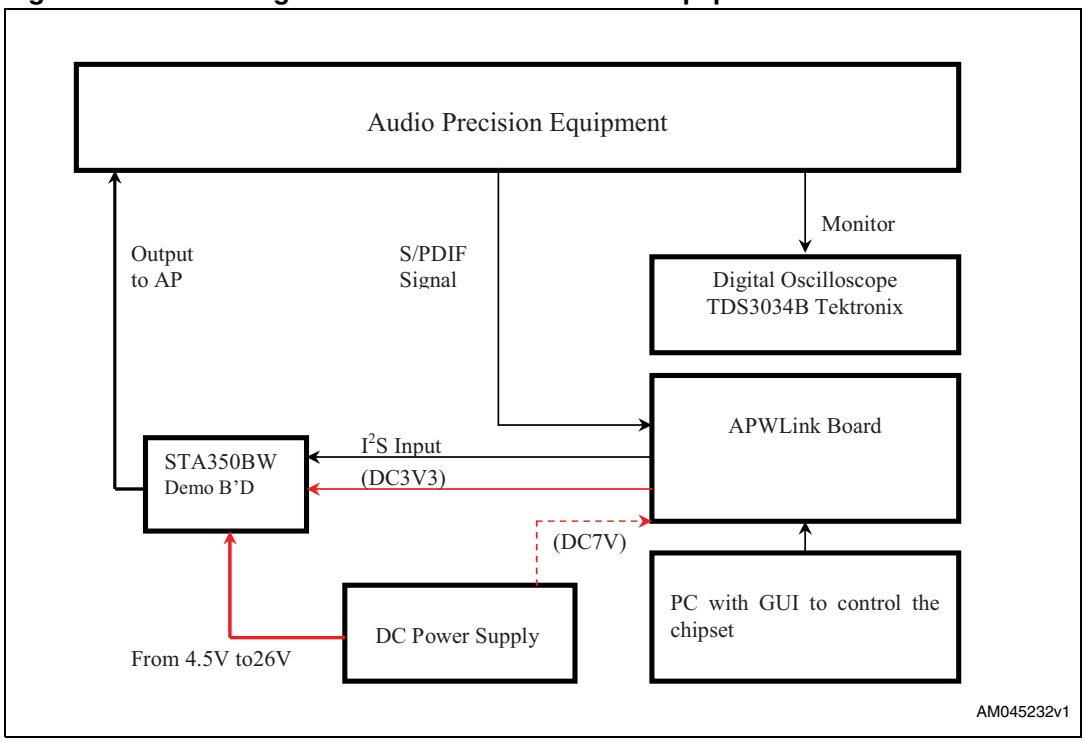


Figure 4. Top view of PCB layout

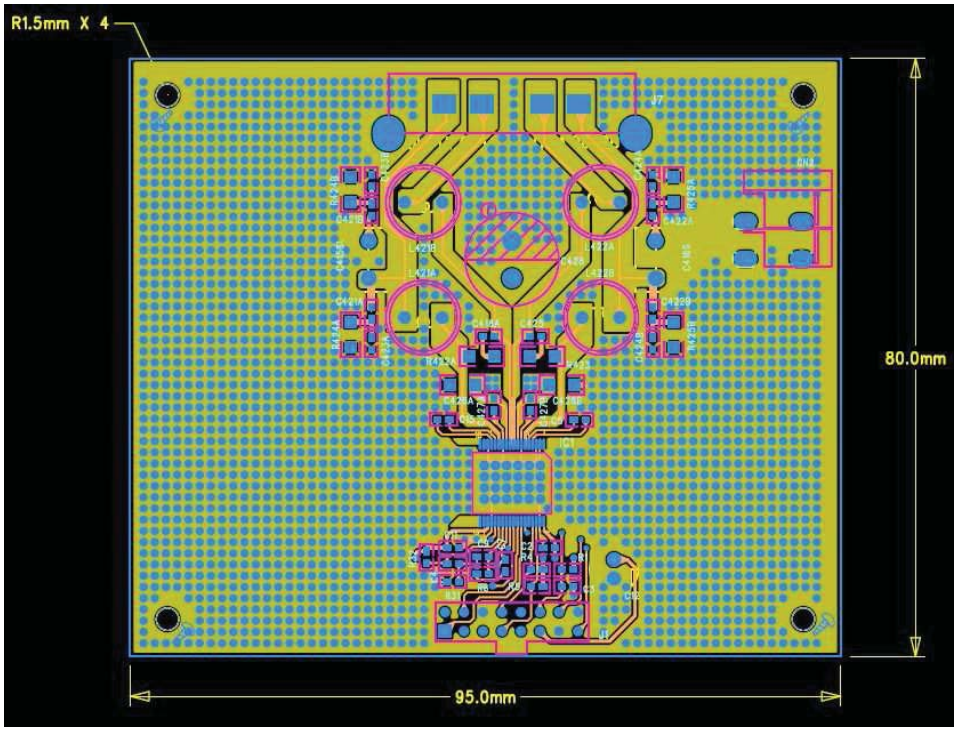


Figure 5. Bottom view of PCB layout

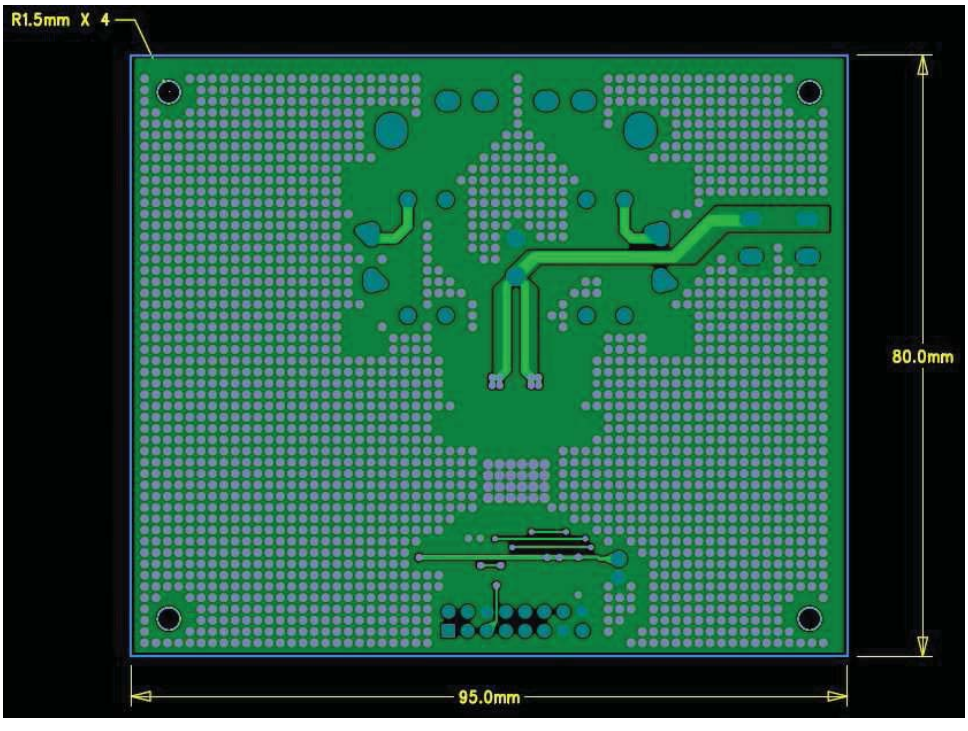


Table 1. Bill of material

No.	Type	Footprint	Description	Qty	Reference	Manufacturer
1	Jack	Through-hole	4P Speaker Jack	1	J7	Any source
2	MCAP	Through-hole	680NF-M(63V) Capacitor	2	C415SL, C416S	Any source
3	Terminal	Through-hole	2P Pitch: 5 mm Connector Terminal	1	CN2	Phoenix Contact
4	CNN	Through-hole	16P (8 x 2 row) 2.5 mm male CNN	1	J1	Any source
5	CCAP	CAP0603	50 volt NPO 330 pF +/- 10%	2	C418A, C425	Murata
6	CCAP	CAP0603	50 volt NPO 680 pF +/- 10%	1	C9	Murata
7	CCAP	CAP0603	50 volt 1 nF +/- 10%	1	C3	Murata
8	CCAP	CAP0603	50 volt 4.7 nF +/- 10%	1	C7	Murata
9	CCAP	CAP0603	50 volt 100 nF +/- 10%	15	C2, C4, C5, C11, C15, C421A, C421B, C422A, C422B, C423A, C423B, C424A, C424B, C427A, C427B	Murata
10	CCAP	CAP1206	50 volt 1 µF +/-10%	2	C426A, C426B	Murata
11	RES	R1206	4R7, +/-5% 1/4W	4	R424A, R424B, R425A, R425B	Murata
12	RES	R1206	20 +/-5% 1/4W	2	R422A, R423	Murata
13	RES	R0603	0 ohm 1/16W	1	R31	Murata
14	RES	R0603	2R2 +/-5% 1/16W	1	R32	Murata
15	RES	R0603	10K +/-5% 1/16W	1	R1	Murata
16	RES	R0603	2.2K +/-5% 1/16W	1	R6	Murata
17	RES	R0603	NS	2	R4, R5	
18	ECAP	Through-hole	22 µF/ 16 V	1	C12	Rubycon/ Panasonic
19	ECAP	Through-hole	1000 µF / 35 V 105 Centigrade	1	C428	Rubycon/ Panasonic
20	Plastic rod		Hexagonal rod 15 mm length, male type	4	Four Corner	
21	Plastic rod		Hexagonal rod 8 mm length, female type	4	Four Corner	
22	IC	PSSO36	STA350BW	1	IC1	ST
23	Coil	Through-hole	15 µH Choke Coil (1014P-01-150L)	4	L421A, L421B, L422A, L422B	KwangSung
24	PCB		STA350BW 2.0 CH VER1.0	1		Fastprint

2 Test results

All the results and graphs are from measures using equipment from Audio Precision.

Figure 6. Efficiency (2 channels, BTL configuration), V_{CC} = 26 V, R_L = 6 ohm

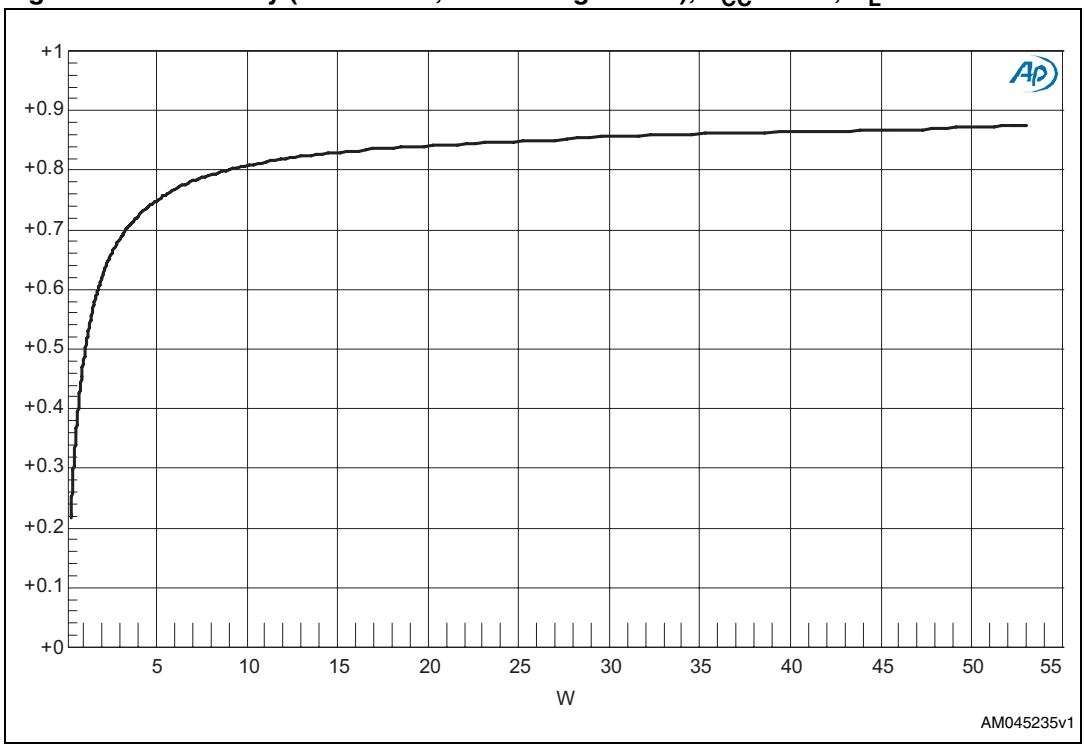


Figure 7. Efficiency (2 channels, BTL configuration), V_{CC} = 26 V, R_L = 8 ohm

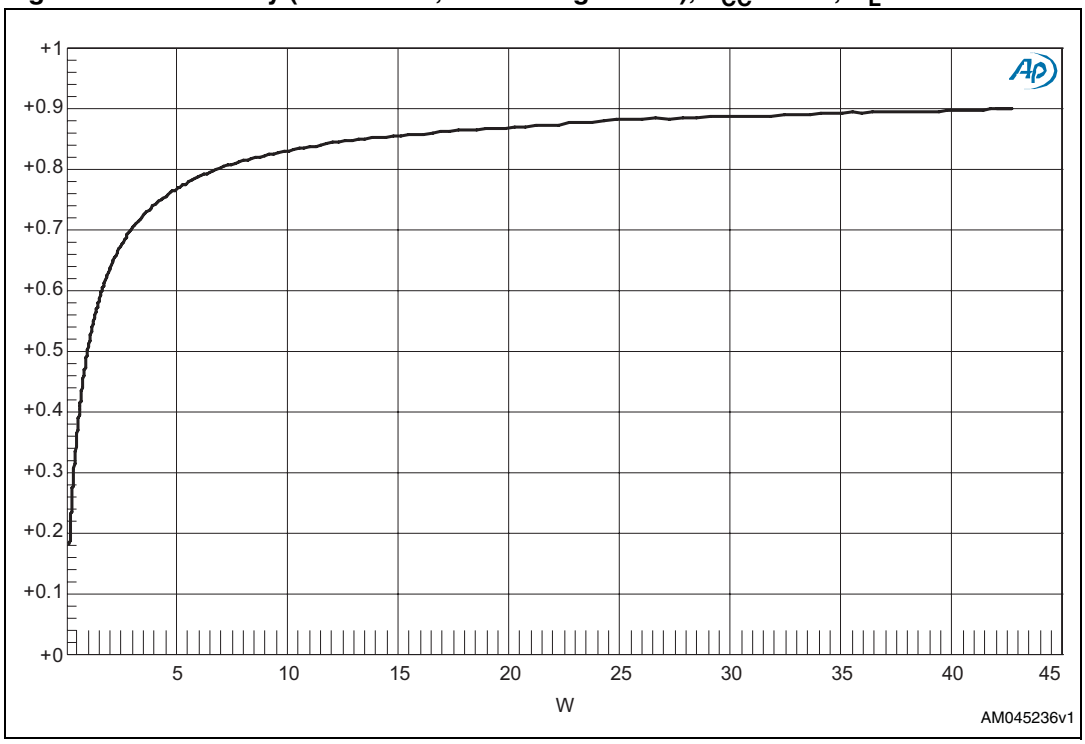


Figure 8. Output power vs. supply voltage, R_L = 6 ohm

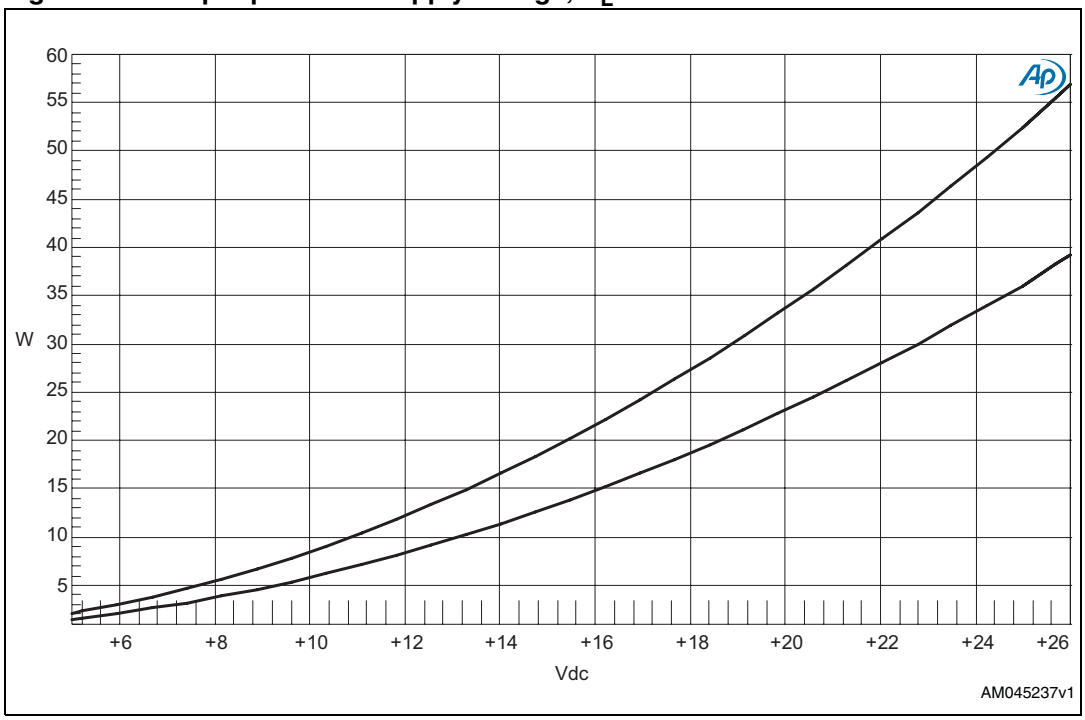


Figure 9. Output power vs. supply voltage, R_L = 8 ohm

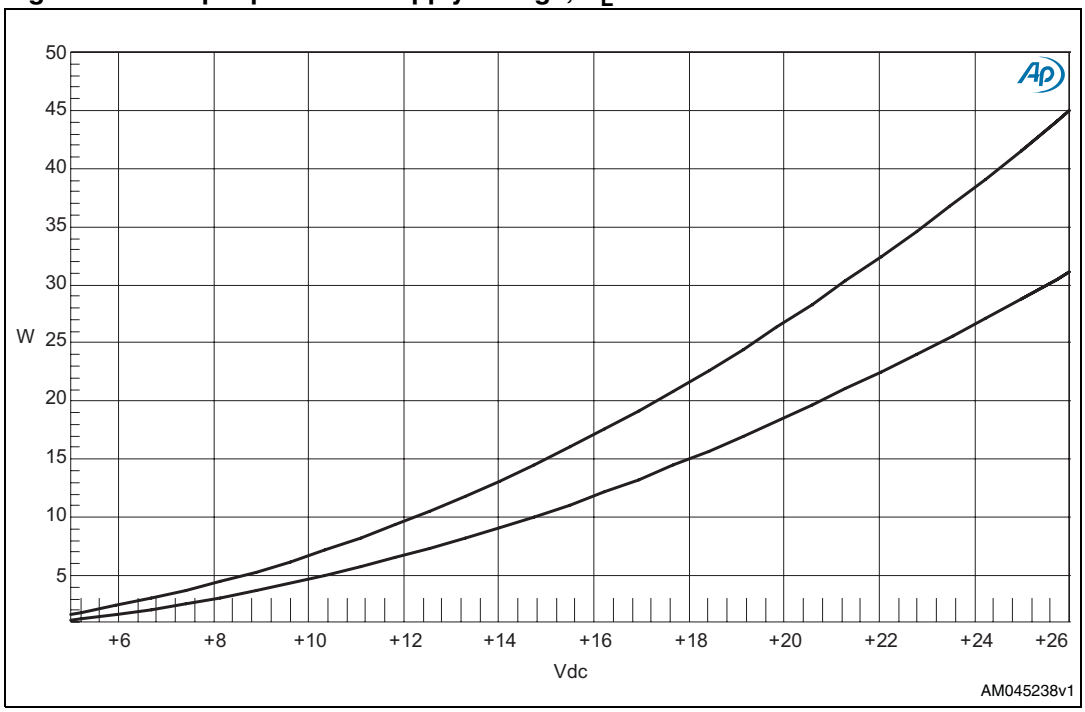


Figure 10. Frequency response, V_{CC} = 24 V, R_L = 6 ohm, 0 dB (Pout = 1 W)

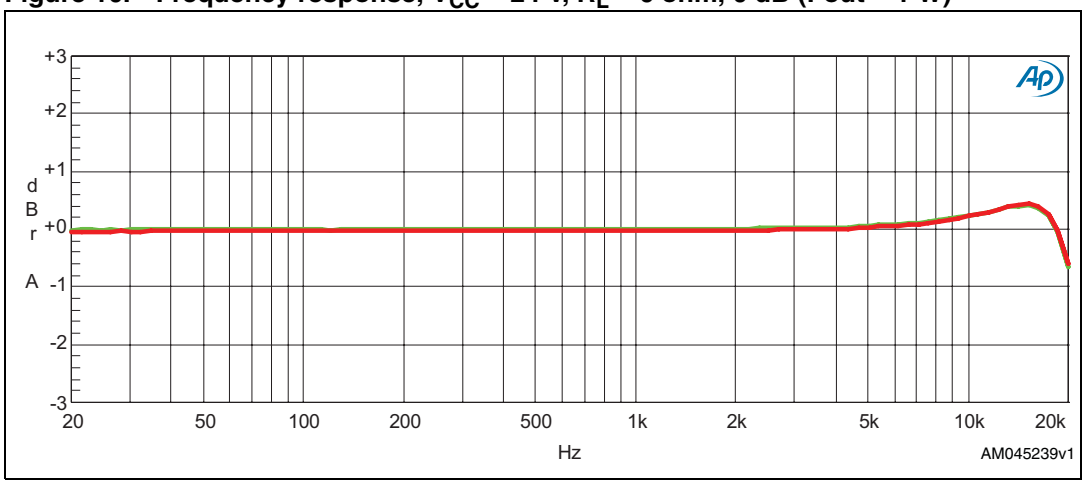


Figure 11. Crosstalk, V_{CC} = 24 V, R_L = 6 ohm, 0 dB (Pout = 1 W)

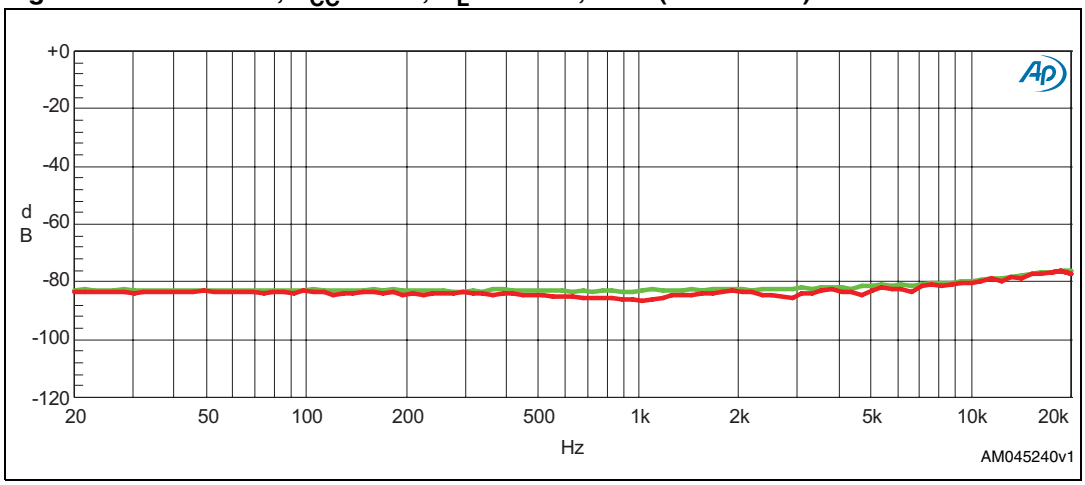


Figure 12. SNR, V_{CC} = 24 V, R_L = 6 ohm, 0 dB (Pout = 1 W)

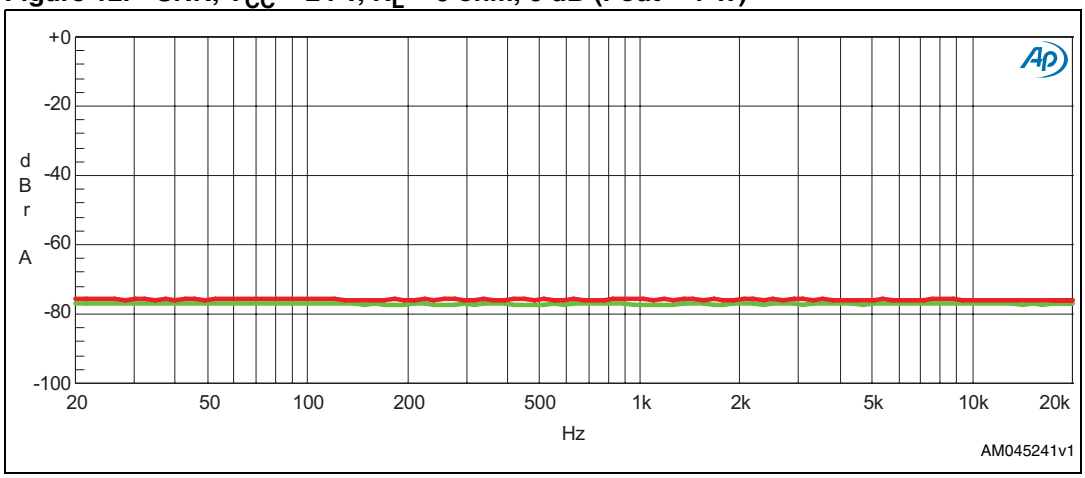


Figure 13. THD vs. frequency, V_{CC} = 24 V, R_L = 6 ohm, Pout = 1 W

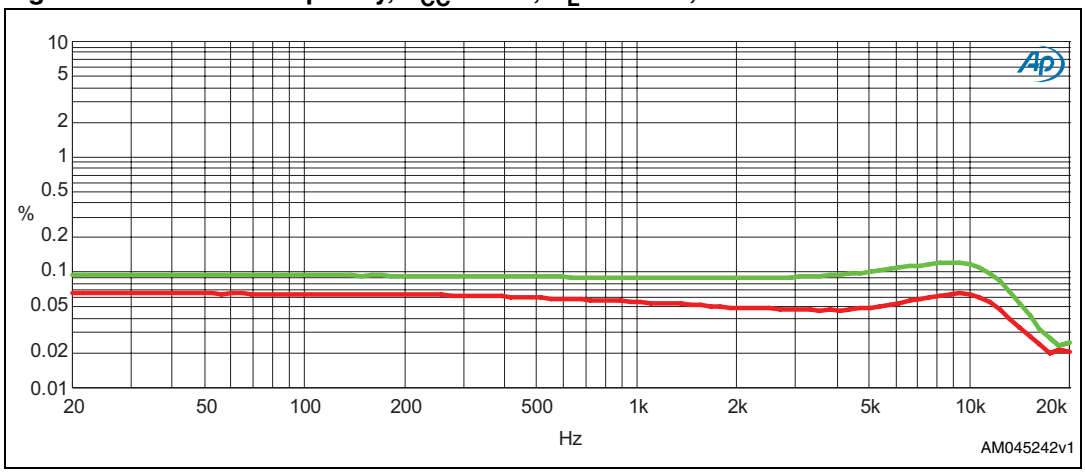


Figure 14. FFT (0 dBFS), V_{CC} = 24 V, R_L = 6 ohm, 0 dBFS (Pout = 1 W)

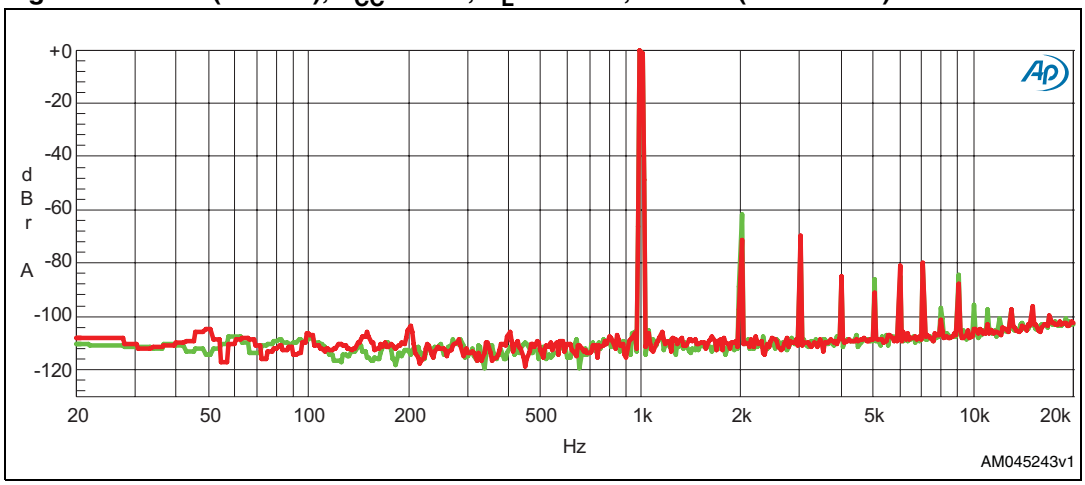


Figure 15. FFT (-60 dBFS), V_{CC} = 24 V, R_L = 6 ohm, 0 dBFS (Pout = 1 W)

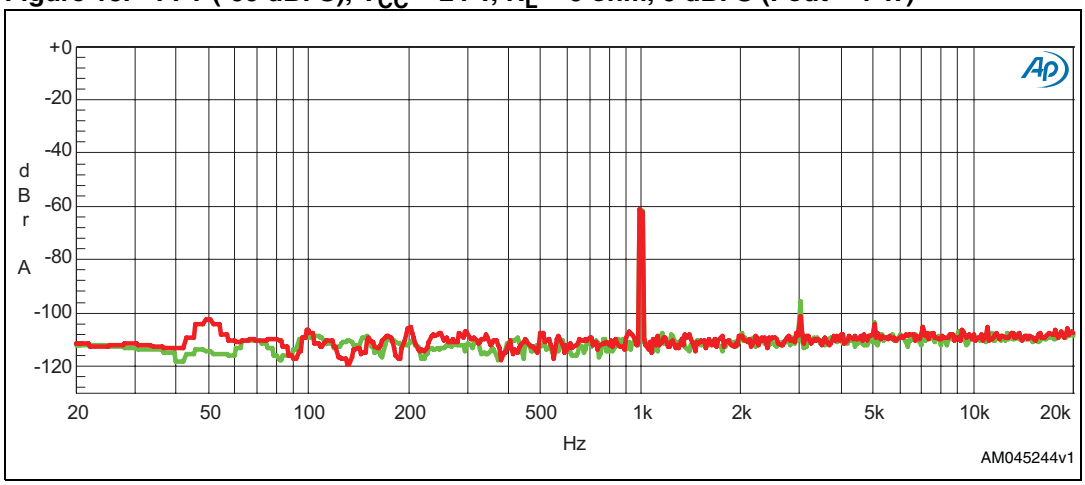
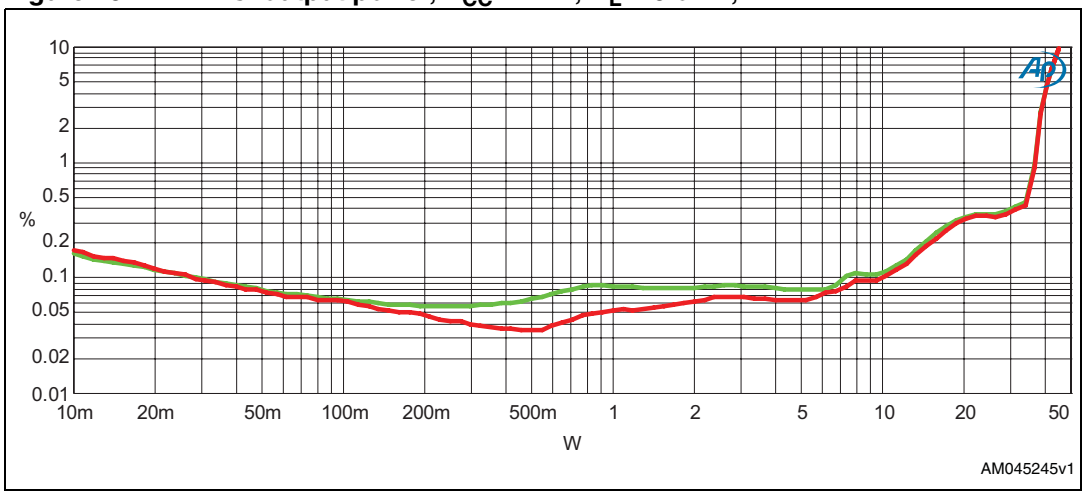


Figure 16. THD vs. output power, V_{CC} = 24 V, R_L = 6 ohm, f = 1 kHz



3 Thermal test results

Figure 17. Output power = 2 x 5 W, V_{CC} = 26 V, load = 6 ohm, frequency = 1 kHz

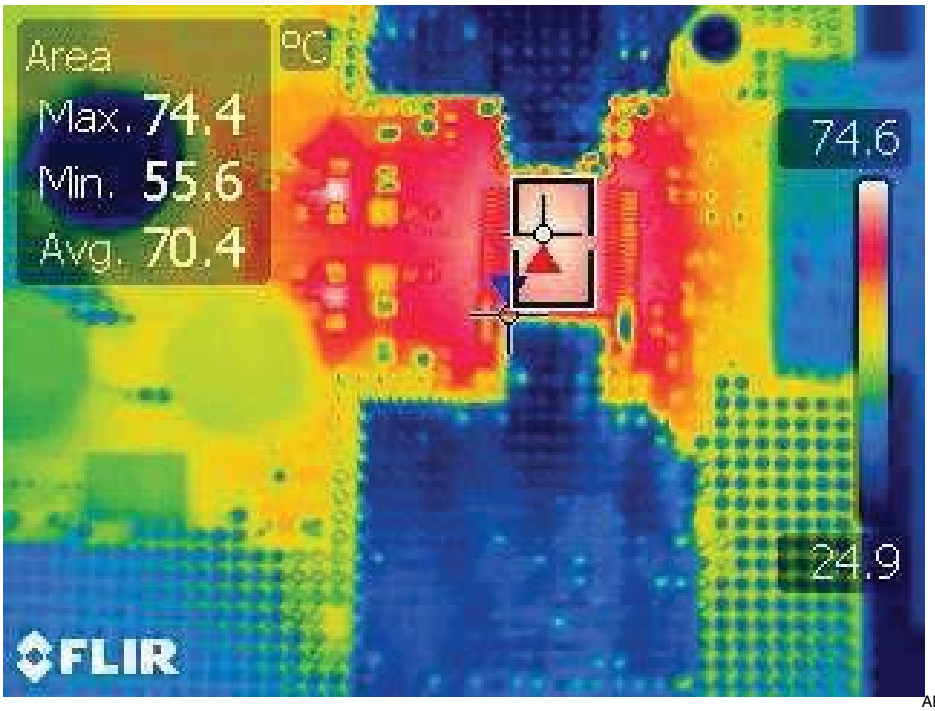


Figure 18. Output power = 2 x 10 W, V_{CC} = 26 V, load = 6 ohm, frequency = 1 kHz

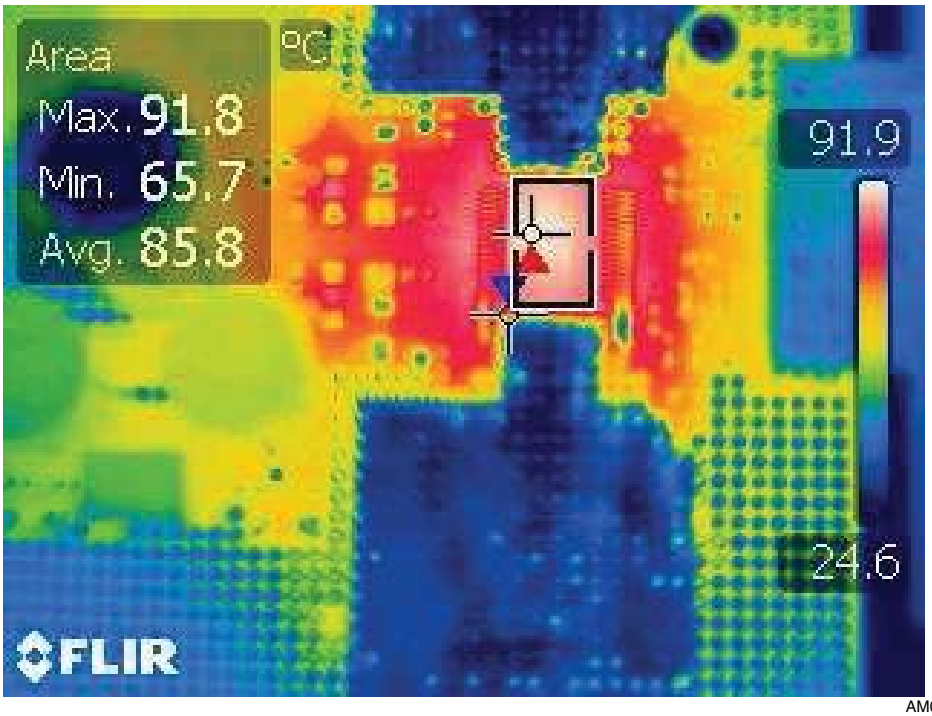


Figure 19. Output power = 2 x 15 W, V_{CC} = 26 V, load = 6 ohm, frequency = 1 kHz

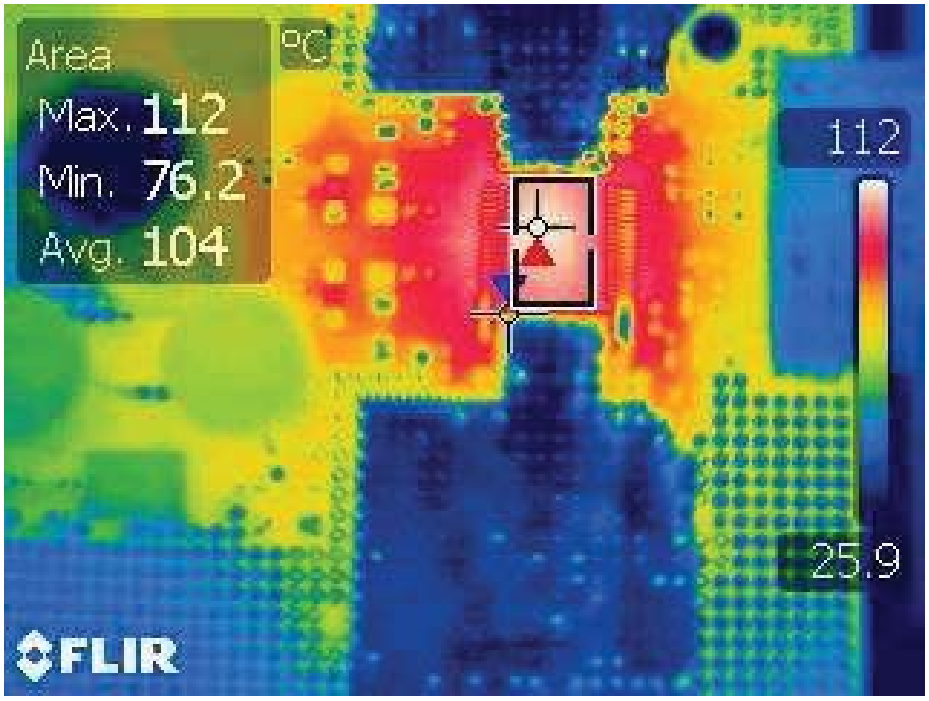
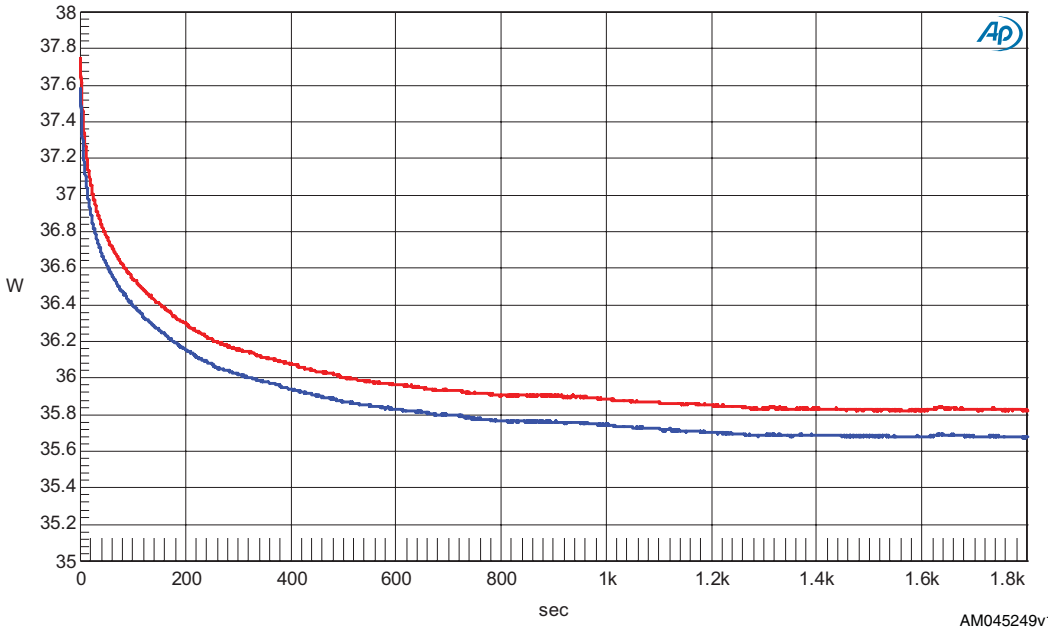


Figure 20. Output power = 2 x 38 W, V_{CC} = 26 V, load = 8 ohm, frequency = 1 kHz



The device works properly during the entire test time (30 minutes).

4 Design guidelines for schematic and PCB layout

4.1 Schematic

4.1.1 Main driver for selection of components

The characteristics of the main driver are as follows:

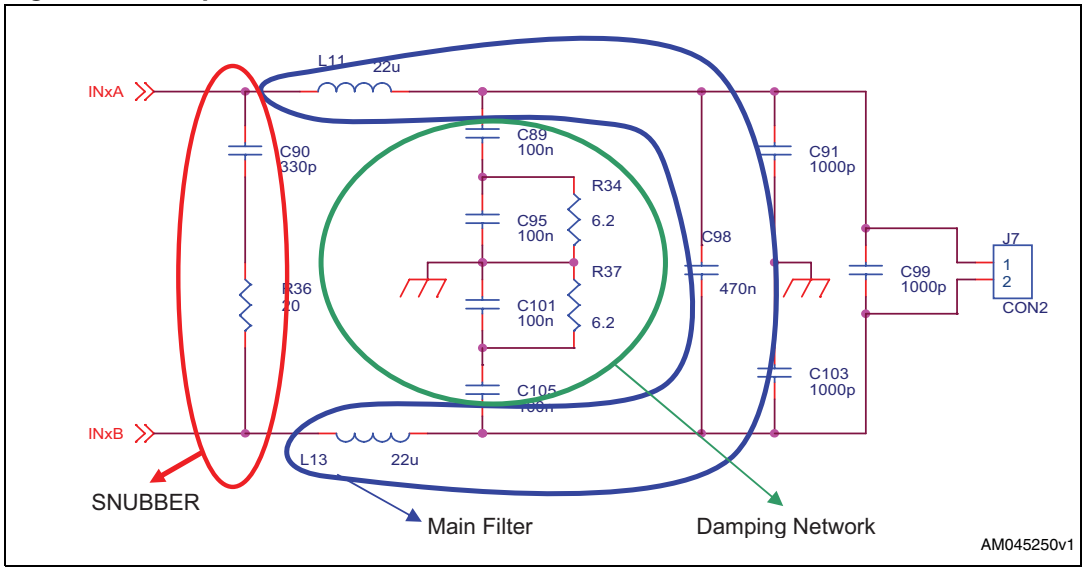
- Absolute maximum rating: STA350BW V_{CC} = 30 V
- Bypass capacitor 100 nF in parallel to 1 µF for each power V_{CC} branch. Preferable dielectric is X7R
- Vdd and Ground for PLL filter separated from the other power supply
- Coil saturation current compatible with the peak current of application

4.1.2 Decoupling capacitors

For the decoupling capacitor(s), one decoupling system can be used per channel. The decoupling capacitor must be as close as possible to the IC pins in order to avoid parasitic inductance with the copper wire on the PC board.

4.1.3 Output filter

Figure 21. Output filter



1. The key function of a snubber network is to absorb energy from the reactance in the power circuit. The purpose of the snubber RC network is to avoid unnecessary high pulse energy such as a spike in the power circuit which is dangerous to the system.

The snubber network allows the energy (big spike) to be transferred to and from the snubber network in order for the system to be worked on safely.

2. The purpose of the main filter is to limit the frequency higher than the audible range of 20 kHz, which is mandatory in order to have a clean amplifier response. The main filter is designed using the Butterworth formula to define the cutoff frequency.
3. The purpose of the damping network is to avoid the high-frequency oscillation issue on the output circuit. The damping network allows the THD to be improved and also allows avoiding the inductive copper on the PCB route when the system is working on high frequency with PWM or PCM.

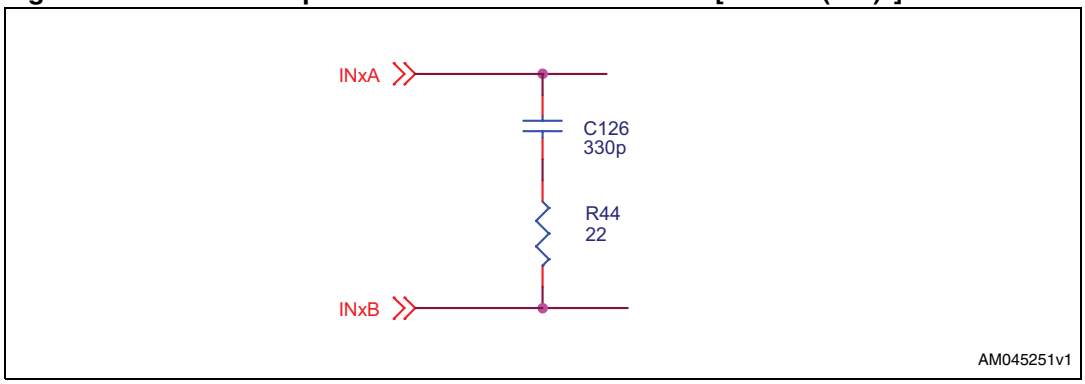
Snubber filter

The snubber circuit must be optimized for the specific application. Starting values are 330 pF in series to 22 ohm. The power on this network is dependent on the power supply, frequency and capacitor value according to the following formula:

$P = C*f*(2*V)^2$

This power is dissipated over the series resistance as shown in *Figure 22*

Figure 22. Power dissipated over the series resistance [$P = C*f*(2*V)^2$]

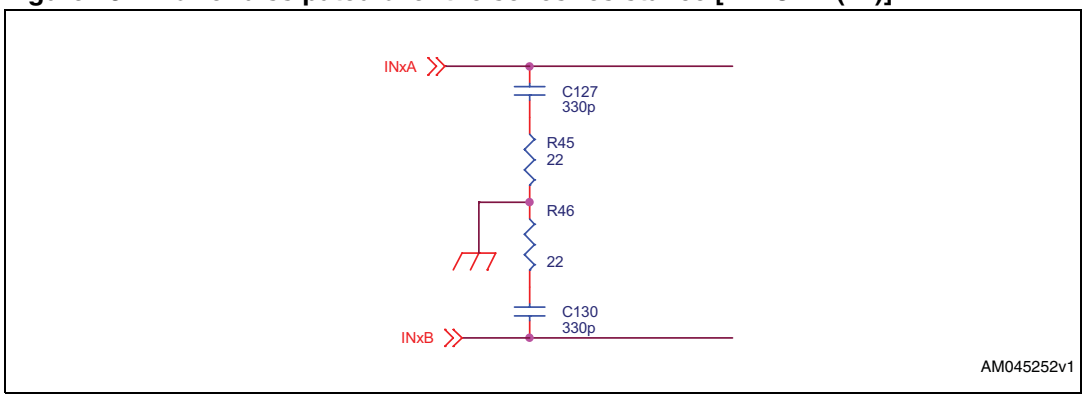


In the following case the formula to evaluate power is:

$P = C*f*2*(V^2)$

This power is dissipated over the series resistance as shown in *Figure 23*:

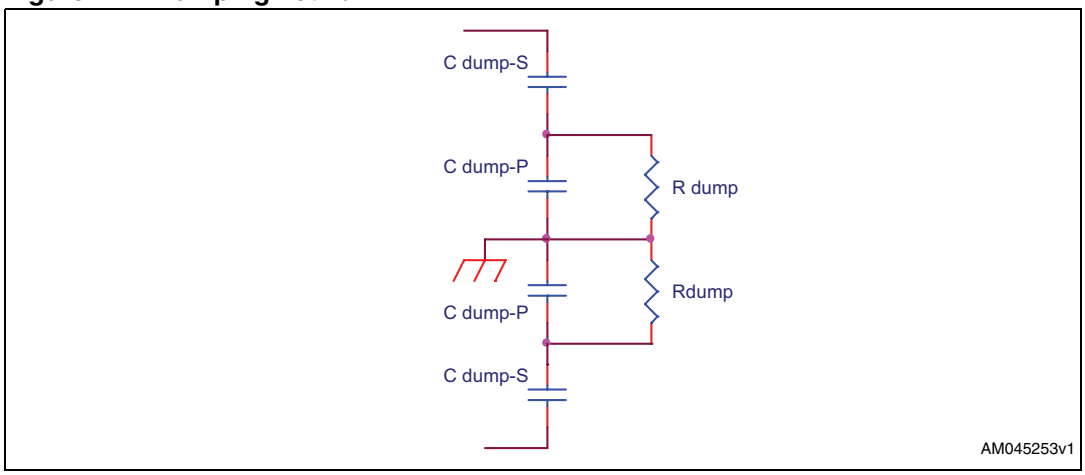
Figure 23. Power dissipated over the series resistance [$P = C*f*2(V^2)$]



Damping network

The C-R-C is a damping network. It is mainly intended for high inductive loads.

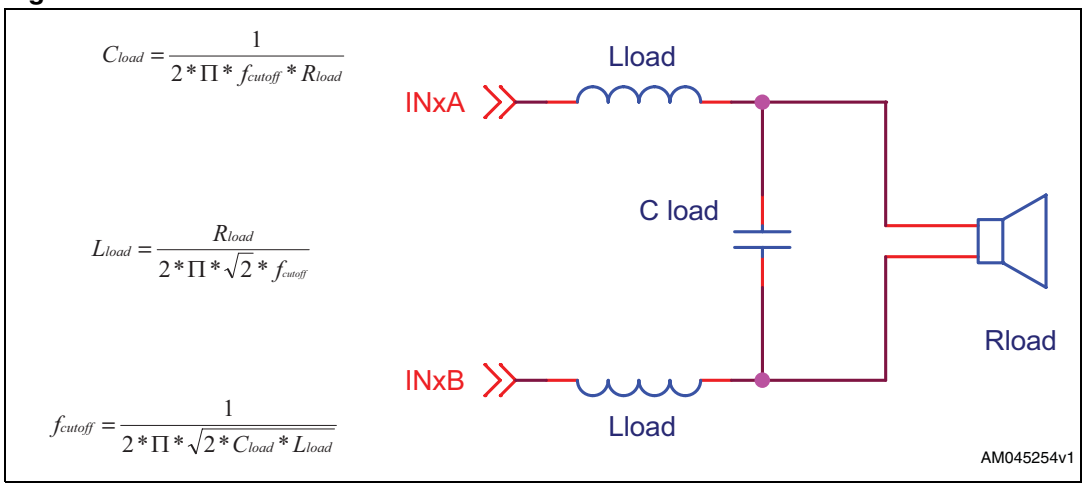
Figure 24. Damping network



Main filter

The main filter is an L and C based Butterworth filter. The cutoff frequency must be chosen between the upper limit of the audio band (≈20 kHz) and the carrier frequency (384 kHz).

Figure 25. Main filter



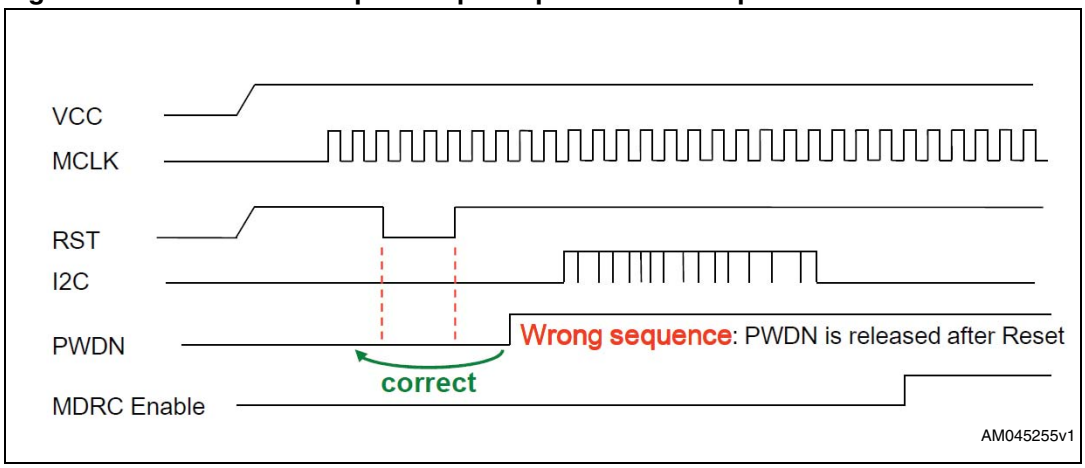
Recommended values

Table 2. Recommended values

R_{load}	16 Ω	12 Ω	8 Ω	6 Ω	4 Ω
L_{load}	47 µH	33 µH	22 µH	15 µH	10 µH
C_{load}	220 nF	330 nF	470 nF	680 nF	1 µF
C dump-S	100 nF	100 nF	100 nF	100 nF	220 nF
C dump-P	100 nF	100 nF	100 nF	100 nF	220 nF
R dump	10	8.2	6.2	4.7	2.7

Recommended power-up and power-down sequence

Figure 26. Recommended power-up and power-down sequence



4.2 PCB layout

The following figures illustrate layout recommendations.

Figure 27. Snubber network soldered as close as possible to the related IC pin

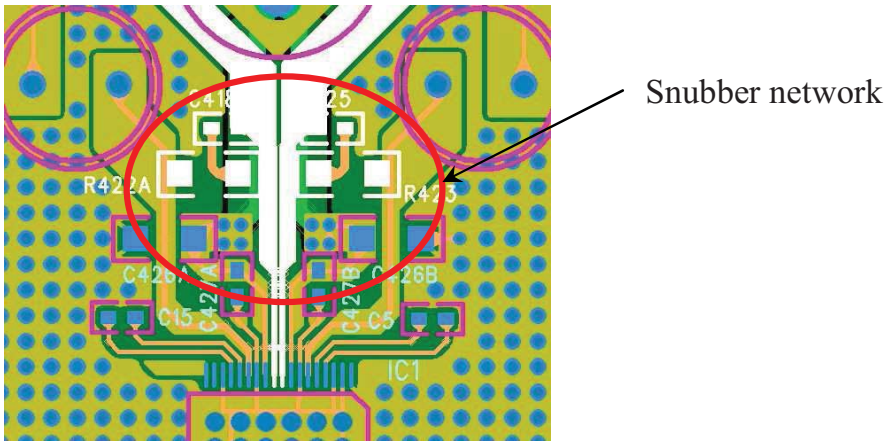


Figure 28. Electrolytic capacitor used first to separate the V_{CC} branches

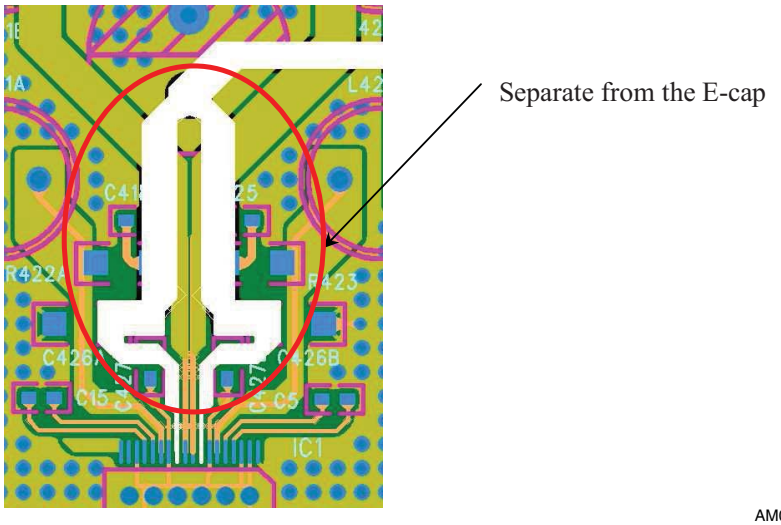
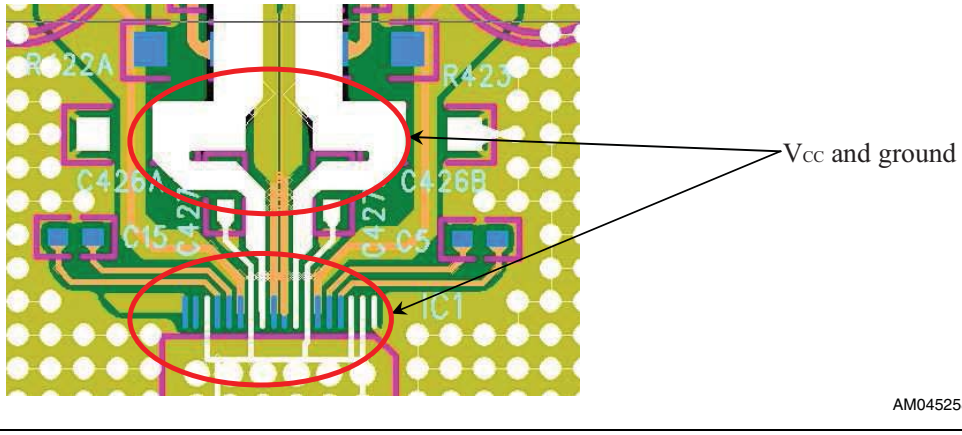


Figure 29. Path between V_{CC} and ground pin minimized in order to avoid inductive paths



For better thermal dissipation, it is recommended that 2-ounce copper be used in the PCB.

It is mandatory to have a large ground plane on the top and bottom layer and solder the slug on the PCB.

Figure 30. Large ground planes on the top and bottom sides of the PCB

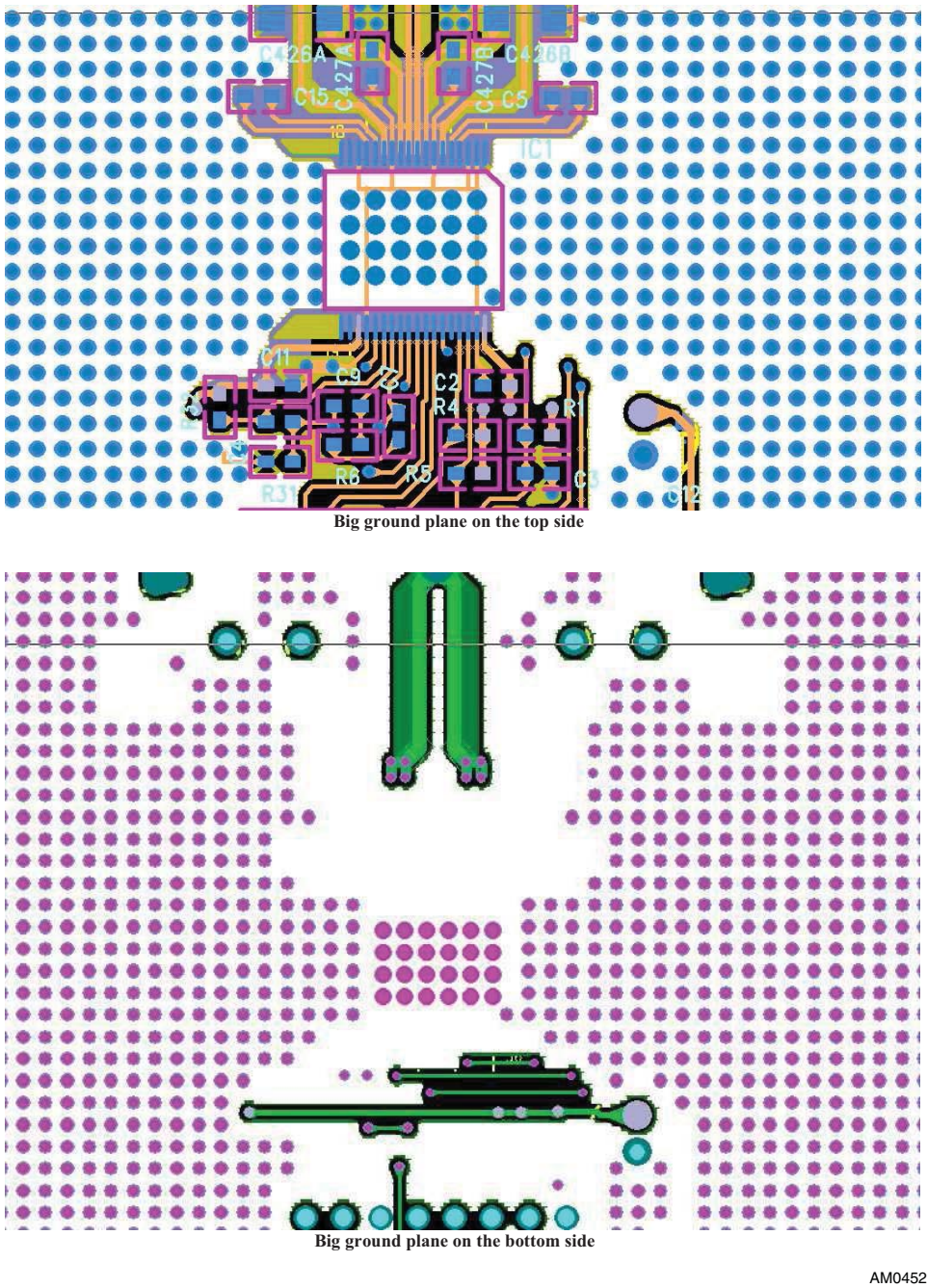


Figure 31. PLL filter soldered as close as possible to the FILT pin

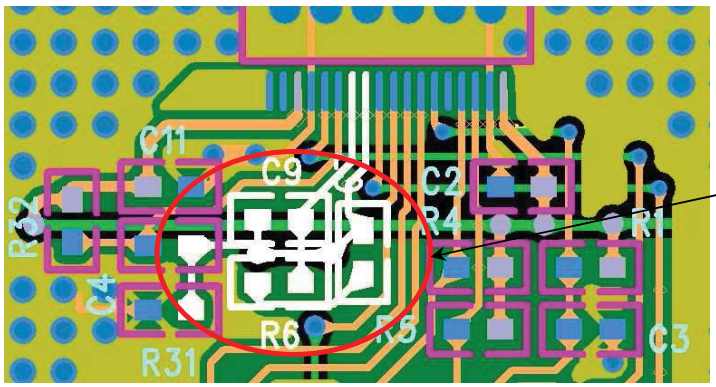


Figure 32. Symmetrical paths created for output stage (for differential applications)

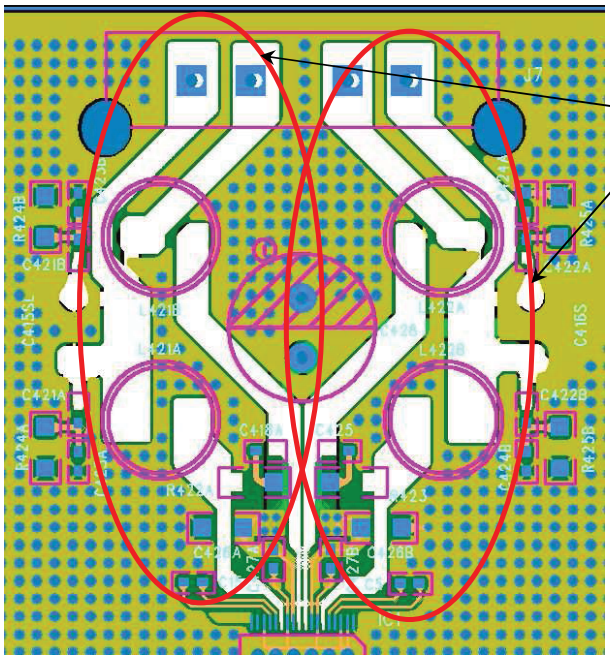


Figure 33. Coils separated in order to avoid crosstalk

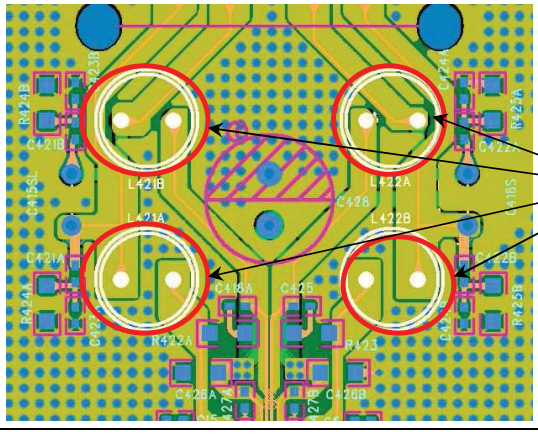
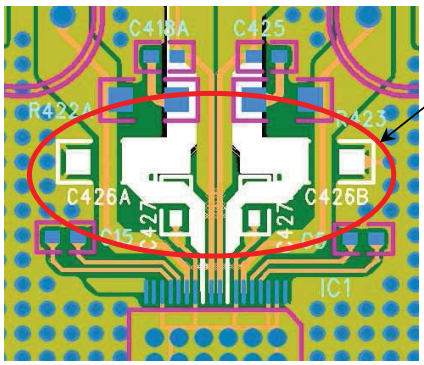


Figure 34. V_{CC} filter for high frequency



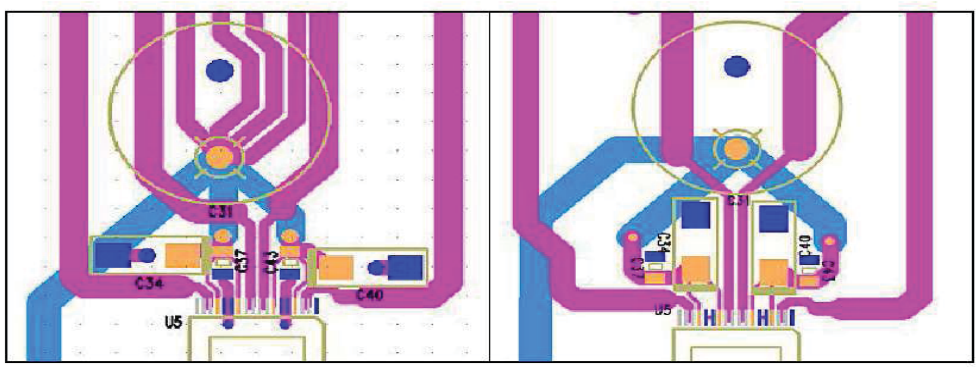
Place Vcc filter capacitors as close as possible to the related pins, the ceramic capacitors on top of the PCB near the IC due to SMD mounting limitations.

AM045263v1

Placing the V_{CC} filter capacitors close to the pins avoids an inductive coil generated by the copper wire because the system is working in PWM with fast switching (the frequency is about 340 kHz) so the longer copper wire is very easy to become an inductor. To improve this we suggest using ceramic capacitors to balance the reactance.

It is mandatory to put the ceramic capacitors as close as possible to the related pins. The distance between the capacitor to the related pins is suggested to be within 5 mm.

Figure 35. Decoupling capacitors



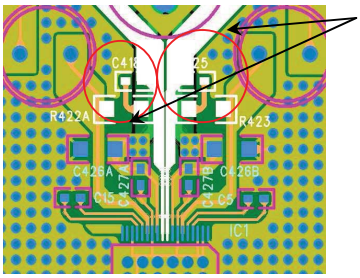
Good Amplifier Bypassing - Capacitors are properly placed

Bad Amplifier Bypassing – Capacitors are out of order and ground connection is indirect

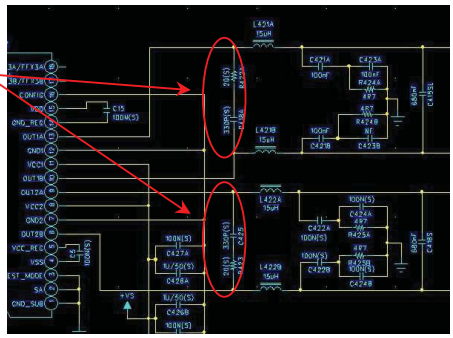
AM045264v1

Solder the decoupling capacitors as close as possible to the related IC pin in order to reduce the inductive coil with copper wire (parasitic inductor). As shown in *Figure 35*, the first example is a correct layout while the second example is incorrect.

Figure 36. Snubber filter for spike high frequency in PWM



Place snubber circuit for spikes in PWM as close as possible to the IC pins and close to the minus and plus of each channel.



AM045265v1

Figure 37. Correct common-mode and differential snubber placement

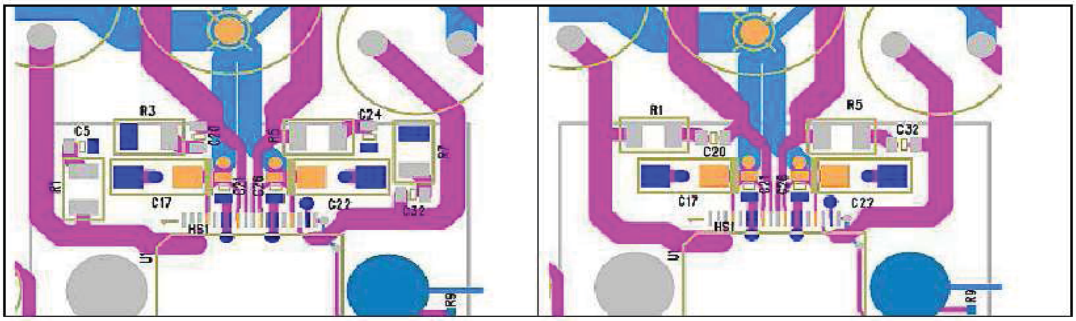


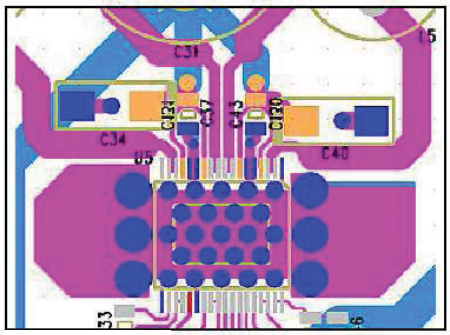
Figure 4: Good Common-Mode Snubber Placement

Figure 5: Good Differential Snubber Placement

AM045266v1

A strong spike could occur if the snubber network is far from the pins and could possibly damage the IC. It is recommended that the distance between snubber network and the pins be within 3 mm, which takes into consideration the diameter of the copper wire.

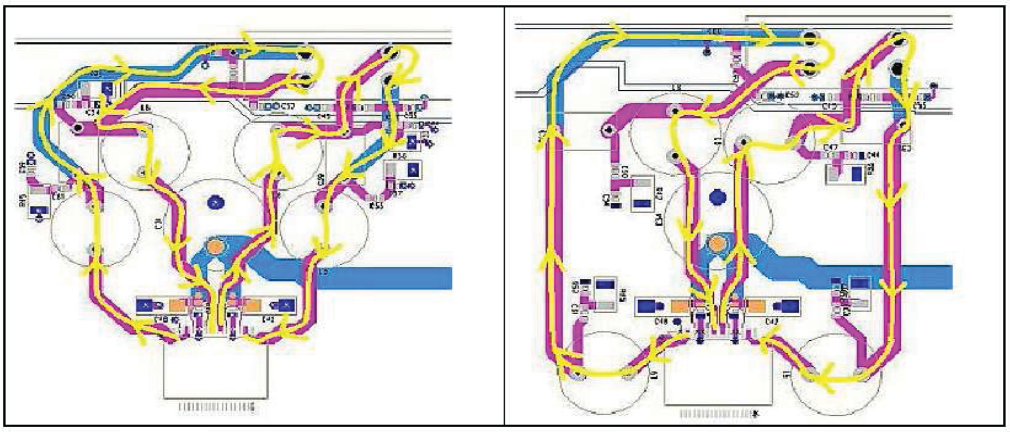
Figure 38. Correct output routing



Good Output Routing –
Traces grow wider as space allows

AM045267v1

Figure 39. Comparison of output routing



Good Output Routing -
Area between outputs is small

Bad Output Routing -
Area between outputs is large

AM045268v1

Figure 40. Thermal layout with large ground (1/3 for top and bottom layers)

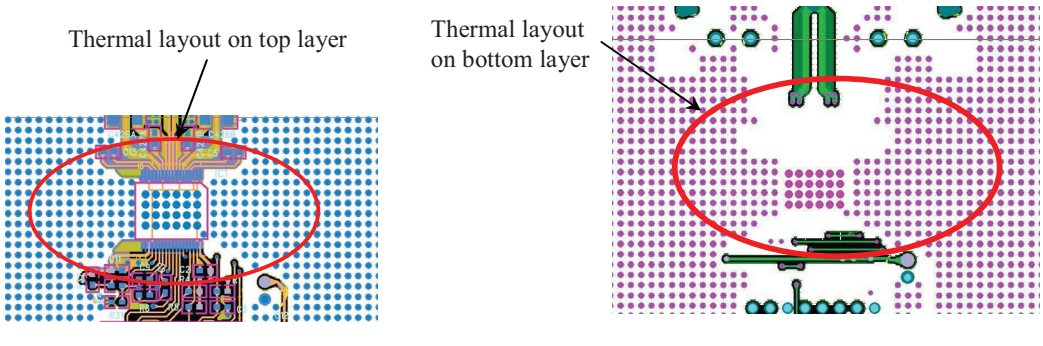


Figure 41. Thermal layout with large ground (2/3 for thermal and soldering holes)

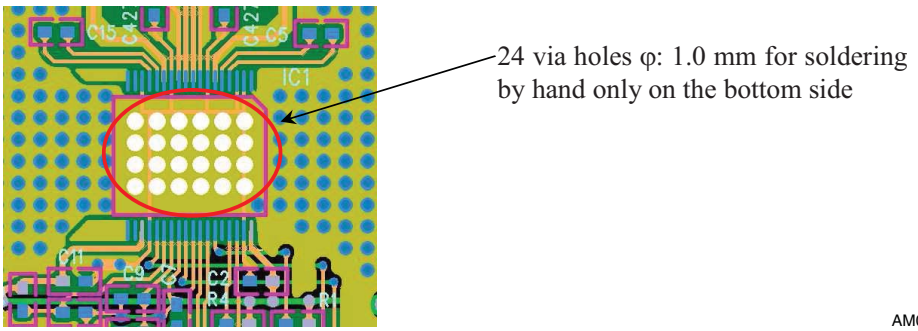


Figure 41 shows an example of the thermal resistance junction to ambient on the bottom side of the STA335B, obtainable with a ground copper area of 7 x 8 cm and with 24 via holes.

Please note that the thermal pad must be connected to ground in order to properly set the IC references. It is necessary that the heat flow freely to the sides of the IC, not only to the top of board but also to the bottom of board, which allows better dissipation of the high temperature using the soldered via holes of the PCB.

Figure 42. Comparison of thermal layout (top layer)

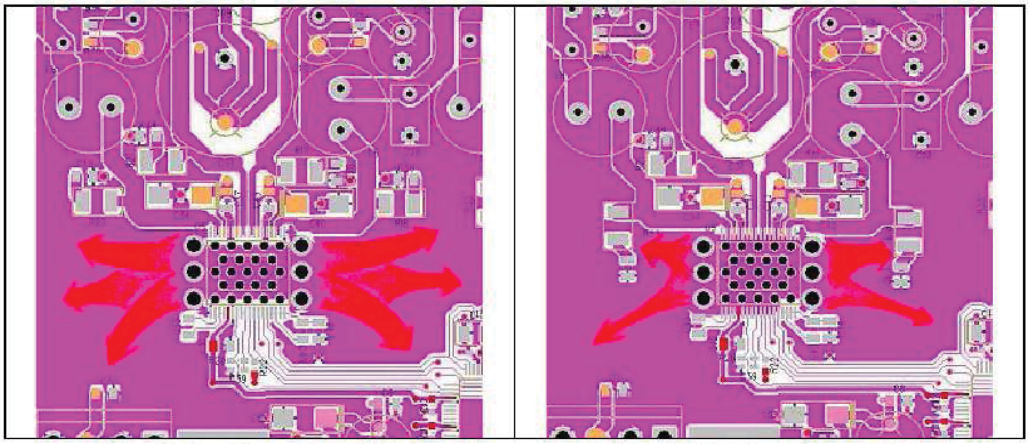
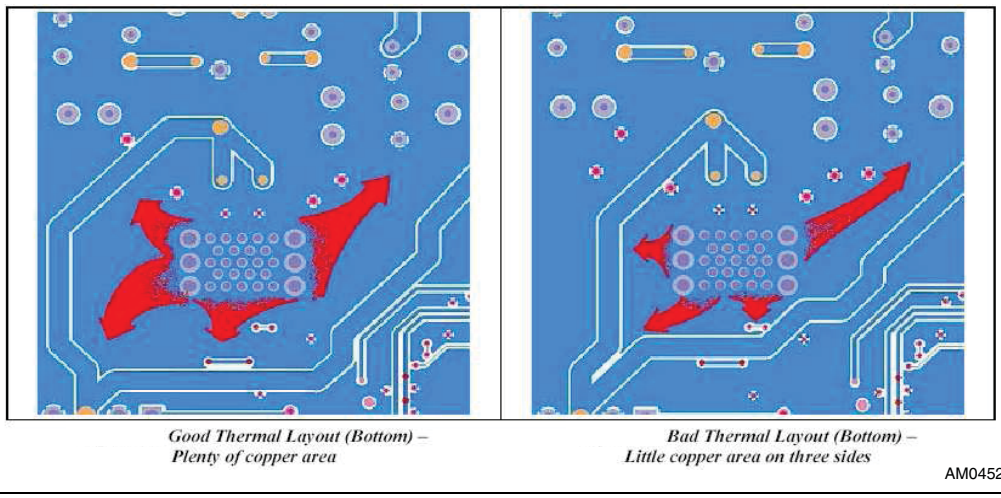


Figure 43. Comparison of thermal layout (bottom layer)



5 Revision history

Table 3. Document revision history

Date	Revision	Changes
08-Apr-2011	1	Initial release.

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