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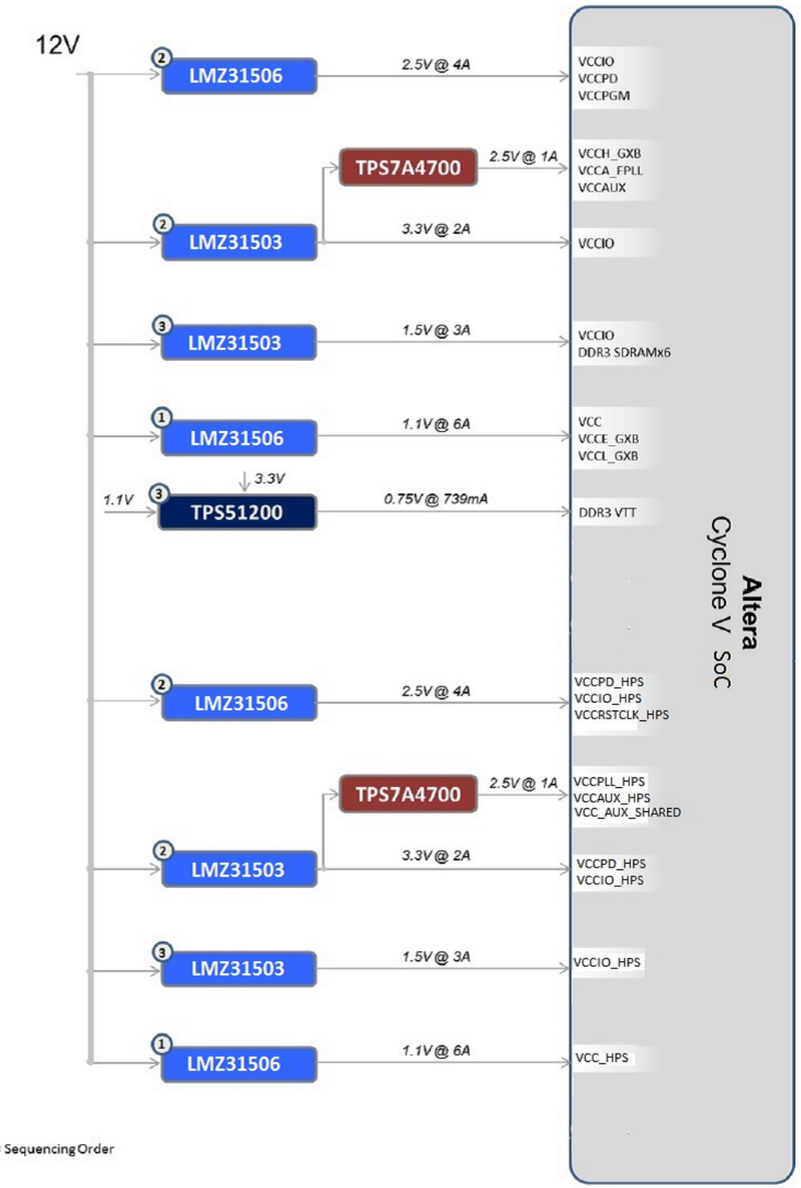

Revision History	
Revision	Notes

Number: PMP9353	Rev: E1	Designed for: Public Release	Mod. Date: 4/22/2014
SVN Rev: Not in version control		Project Title: Altera Cyclone V SoC	
Drawn By:		Sheet Title:	
Engineer: Sami Sirhan		Assembly Variant: [No Variations]	Sheet: 1 of 6
		File: Cover Sheet_ANSI-B.SchDoc	Size: B
		Contact: http://www.ti.com/support	

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FPGA Power

Rvadj = 1.74k,
Rrt/clk = 261k

Sets:
VOUT = 1.1V
fSW = 430kHz

+4.5V to 14V
VIN INPUT
J1
ED120/2DS
C3 68µF 16V
C4 47µF 16V
R2 49.9 1%
R4 1.74k 1%
U1
LMZ31506RUQ
R6 261k
RT/CLK1
PG_1p1V
R7 68.1k
C10 0.1µF
R8 12.1k
D1 BZT52C5V1T-7 5.1V
C6 47µF 6.3V
C7 47µF 6.3V
C8 47µF 6.3V
C9 47µF 6.3V
C5 220µF 6.3V
FPGA Core Supply
+1.1V/6A
J2
NT2 Net-Tie

PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.

Rvadj = 453,
Rrt/clk = 158k

Sets:
VOUT = 3.3V
fSW = 630kHz

C1 68µF 16V
C2 47µF 16V
R1 49.9 1%
R3 453 1%
U2
LMZ31503RUQ
R5 158k 1%
PG_3p3V
PG_2p5V_HPS
NT1 Net-Tie
SW_NODE net acts as master clock
SW_NODE
C12 47µF 6.3V
C13 47µF 6.3V
C14 47µF 6.3V
C15 47µF 6.3V
C11 220µF 6.3V
VCCIO Supply
+3.3V/2.5A
J3

PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.

Rvadj = 453,
Rrt/clk = 165k

Sets:
VOUT = 2.5V
fSW = 530kHz

C18 68µF 16V
C19 47µF 16V
R10 49.9 1%
R12 453 1%
U3
LMZ31506RUQ
R14 165k 1%
RT/CLK2
PG_1p1V_HPS
PG_2p5V
C21 47µF 6.3V
C22 47µF 6.3V
C23 47µF 6.3V
C24 47µF 6.3V
C20 220µF 6.3V
VCCPD, VCCPGM, or VCCIO Supply
+2.5V/3.5A
J4
NT3 Net-Tie

PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.

Rvadj = 1.62k,
Rrt/clk = 324k

Sets:
VOUT = 1.5V
fSW = 480kHz

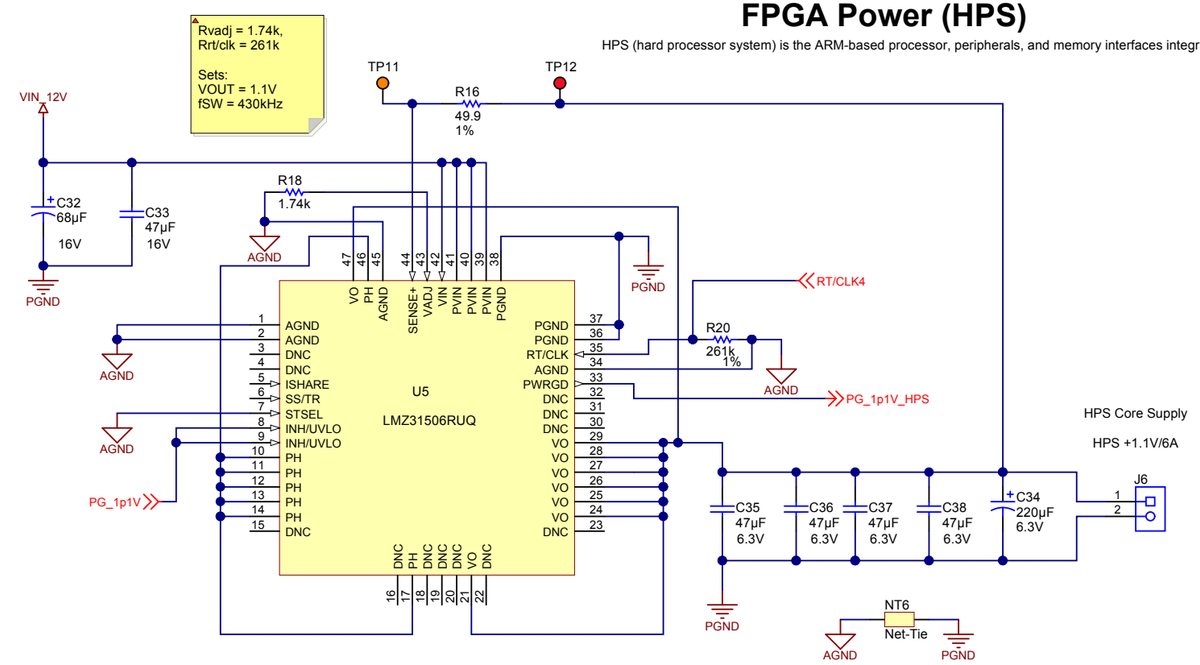
C16 68µF 16V
C17 47µF 16V
R9 49.9 1%
R11 1.62k 1%
U4
LMZ31503RUQ
R13 324k 1%
RT/CLK3
PG_1p5V
PG_3p3V_HPS
NT4 Net-Tie
C26 47µF 6.3V
C27 47µF 6.3V
C28 47µF 6.3V
C29 47µF 6.3V
C25 220µF 6.3V
VCCIO Supply
+1.5V/3A
J5

PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.

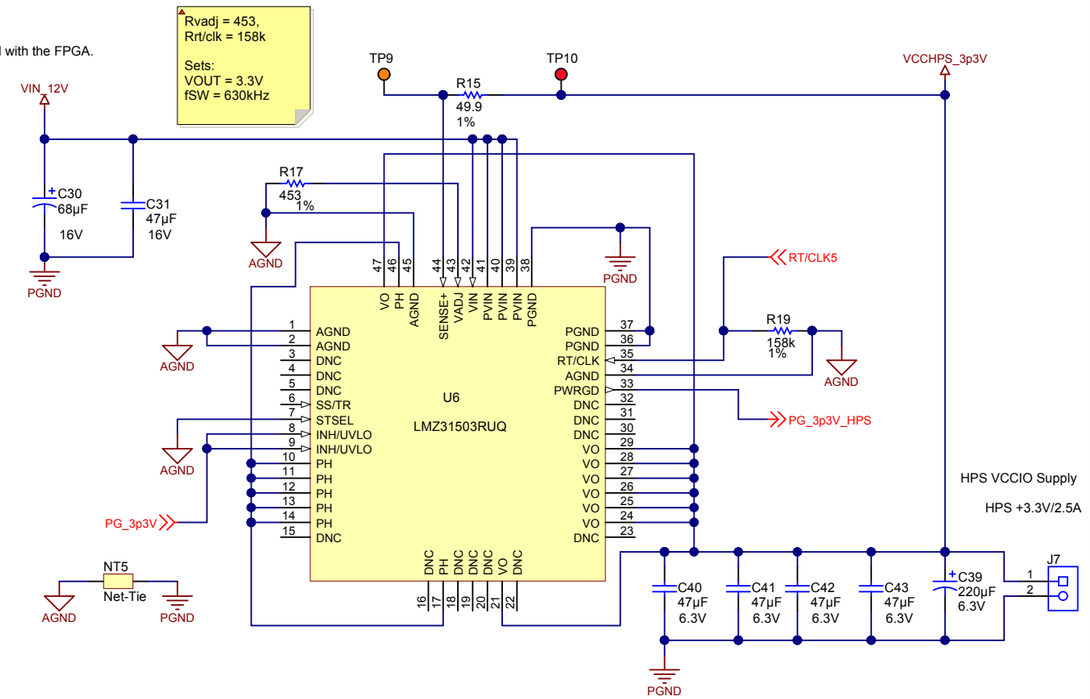
Designed for: Public Release		Mod. Date: 4/22/2014	
Project Title: Altera Cyclone V SoC			
Number: PMP9353	Rev: E1	Sheet Title: Page 1	
SVN Rev: Not in version control		Assembly Variant: [No Variations]	Sheet: 2 of 6
Drawn By: Sami Sirhan		File: Main Schematic.SchDoc	Size: B
Engineer: Sami Sirhan		Contact: http://www.ti.com/support	

FPGA Power (HPS)

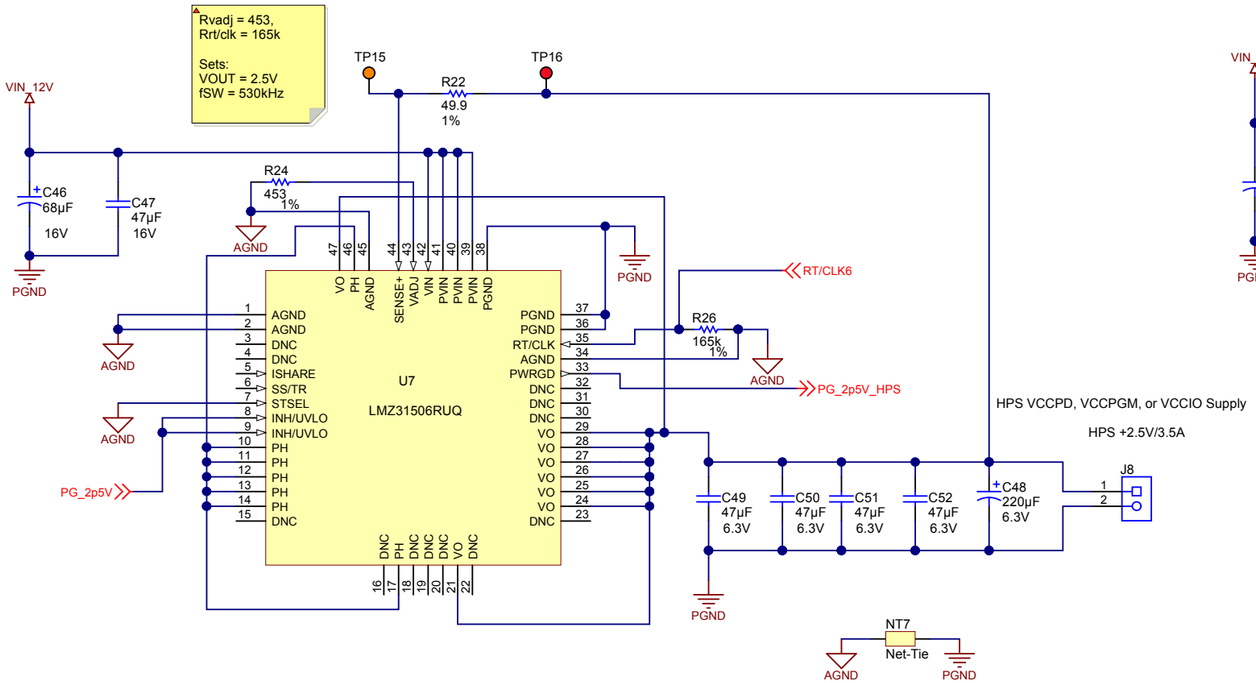
HPS (hard processor system) is the ARM-based processor, peripherals, and memory interfaces integrated with the FPGA.



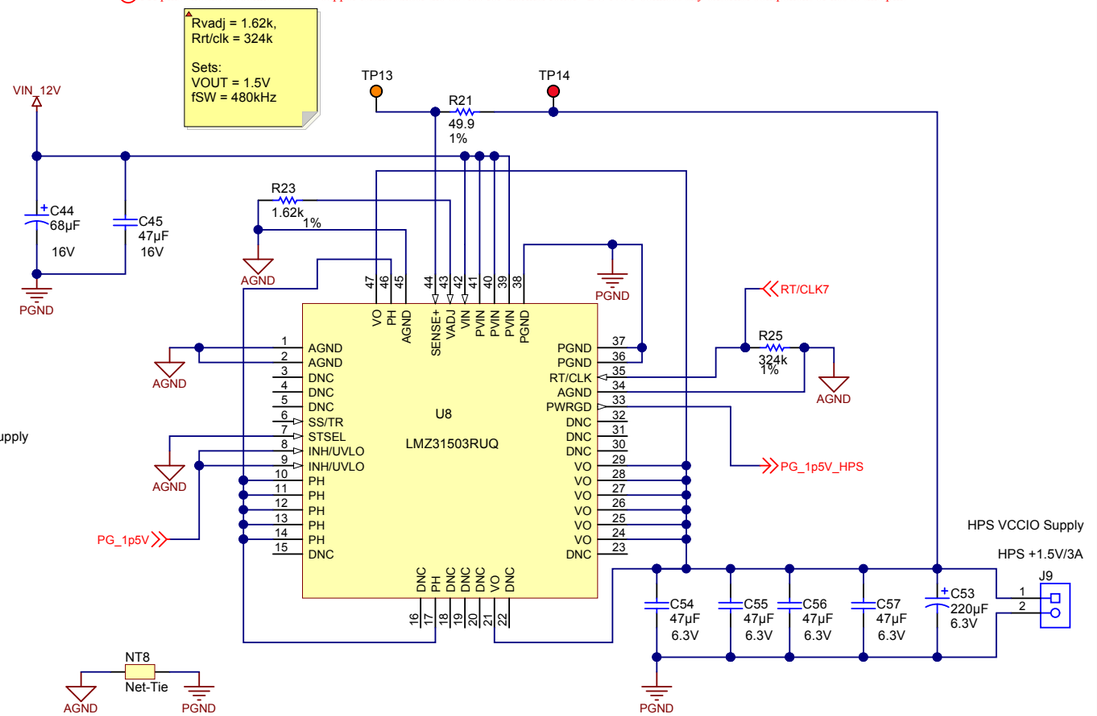
PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.



PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.



PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.



PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.

Number: PMP9353	Rev: E1	Designed for: Public Release	Mod. Date: 4/22/2014
SVN Rev: Not in version control		Project Title: Altera Cyclone V SoC	
Drawn By:		Sheet Title:	
Engineer: Sami Sirhan		Assembly Variant: [No Variations]	Sheet: 3 of 6
		File: Page2.SchDoc	Size: B
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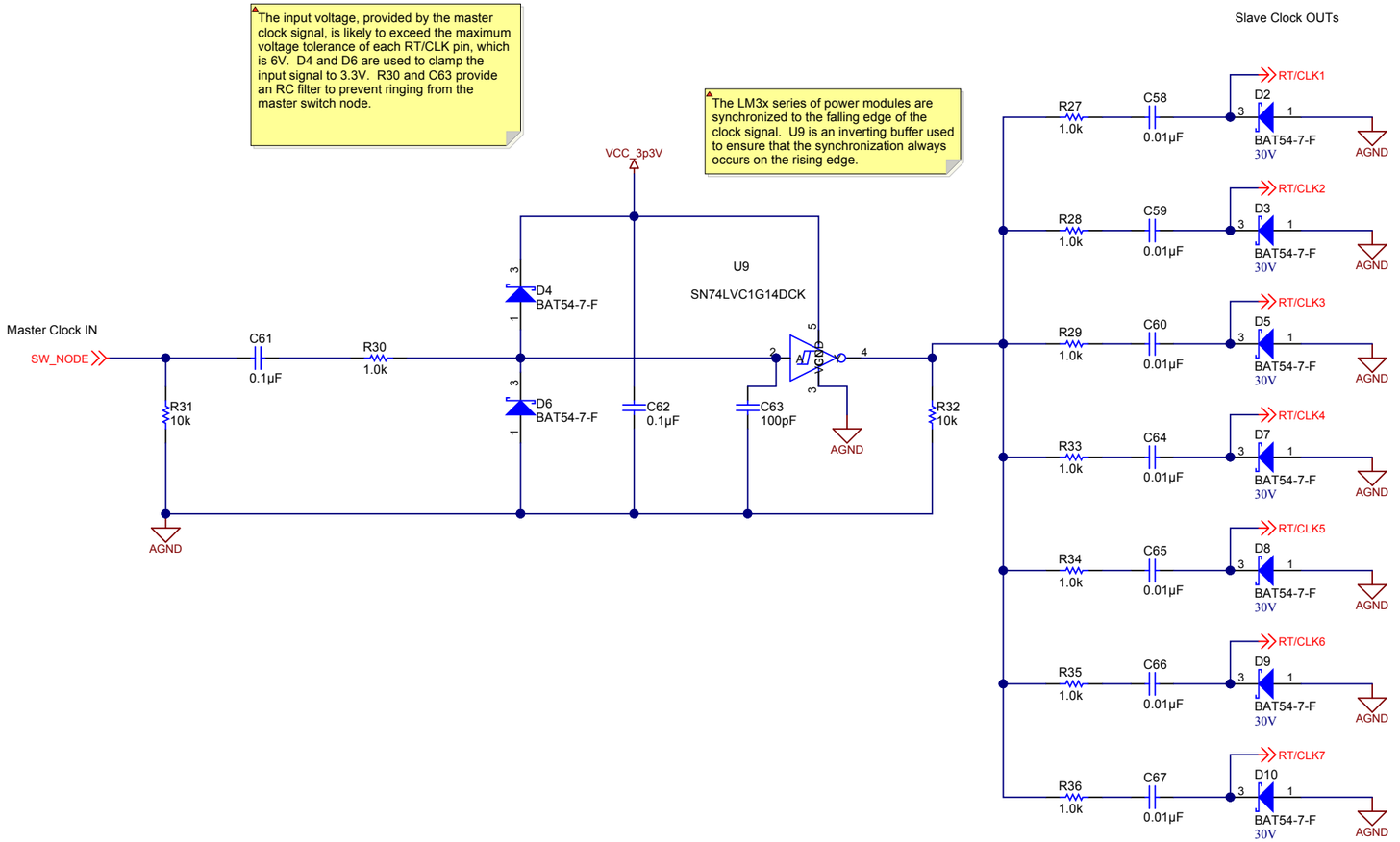
Clock Synchronization Circuit

The input voltage, provided by the master clock signal, is likely to exceed the maximum voltage tolerance of each RT/CLK pin, which is 6V. D4 and D6 are used to clamp the input signal to 3.3V. R30 and C63 provide an RC filter to prevent ringing from the master switch node.

The LM3x series of power modules are synchronized to the falling edge of the clock signal. U9 is an inverting buffer used to ensure that the synchronization always occurs on the rising edge.



Number: PMP9353	Rev: E1	Designed for: Public Release	Mod. Date: 2/18/2014
SVN Rev: Not in version control		Project Title: Altera Cyclone V SoC	
Drawn By:		Sheet Title:	
Engineer: Sami Sirhan		Assembly Variant: [No Variations]	Sheet: 4 of 6
		File: Page3.SchDoc	Size: B
		Contact: http://www.ti.com/support	

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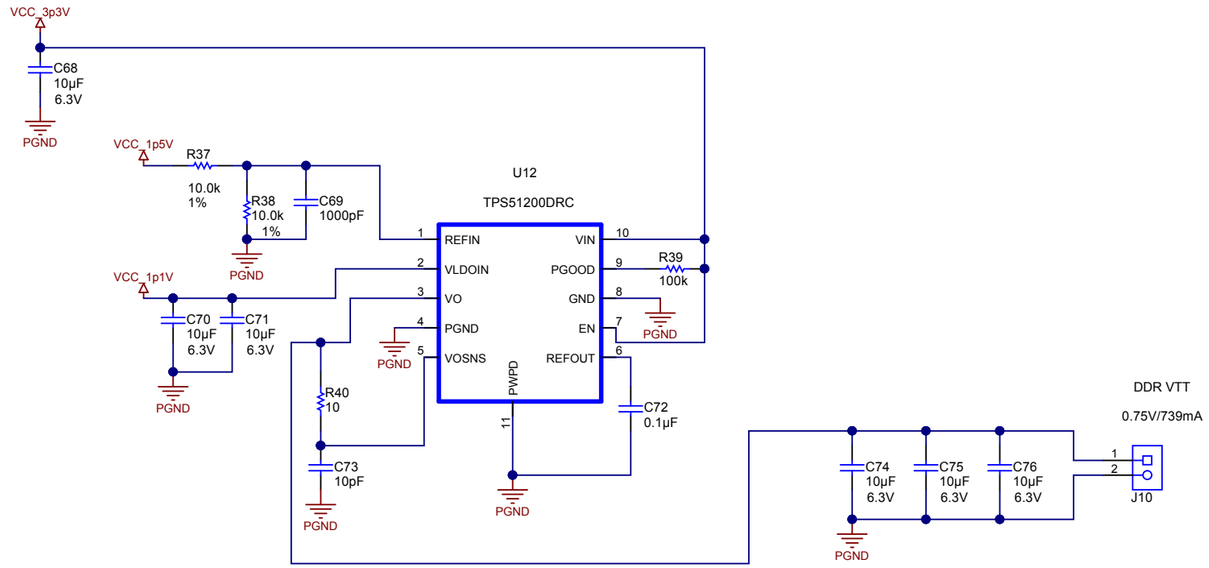
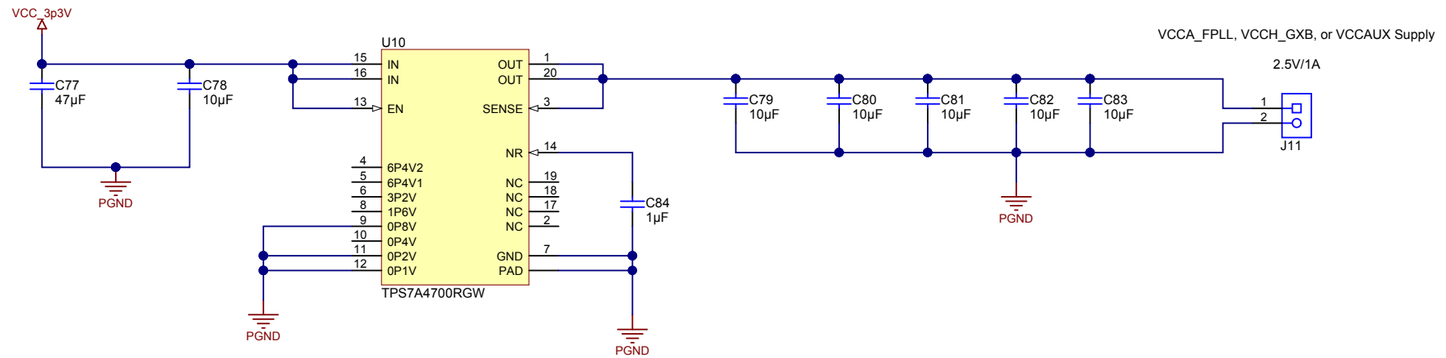
DDR Termination and LDOs





Designed for: Public Release			Mod. Date: 2/19/2014
Project Title: Altera Cyclone V SoC			
Number: PMP9353	Rev: E1	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: [No Variations]	Sheet: 5 of 6
Drawn By:		File: Page 4.SchDoc	Size: B
Engineer: Sami Sirhan		Contact: http://www.ti.com/support	

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