REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	02-11-13	M.W.
	B	FLASH MEMORY/ RESET UPDATE	05-22-13	M.W.
	C	PWR USB MODE, U14 UPDATE	08-14-13	M.W.

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98 (DIELECTRIC CONSTANT +4.3 +/-0.6)

   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'

5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .007"/.005". THIS LINE AT COPPER LAYER MUST MEET AT THIS REQUIREMENT

7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
   .05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
   2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - RED COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.
   MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.

10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.

14. MAY ADD TEARDROPS TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

16. BASIC GRID INCREMENT AT 1:1 IS .0001.

17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)

19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM.

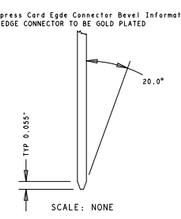
21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURING REQUIREMENT. ADDITION OF .25" RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER AND FAB HOUSE. PANELIZATION MUST BE APPROVED BY FREESCALE.

22. THE PCI CARD EDGE CONNECTOR FINGERS SHALL BE PLATED WITH A MINIMUM OF 30 MICRO INCHES OF HARD GOLD OVER 100-200 MICRO INCHES OF NICKEL BOTH SIDES OF THE BOARD

23. OVERALL PCB DIELECTRIC THICKNESS ARE TARGETED (A & C) 20 MILS+/- 10% AND (B) 18 MILS+/- 10% AS SHOWN IN DETAIL 'A'.
    ADJUSTMENT OF SUBSTRATE B IS ALLOWED TO MEET OVERALL HEIGHT REQUIREMENT

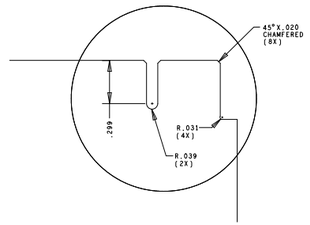
24. THIS LINE(X=2886,Y=638) IS INTENTED TO BE CONNECTED TO RF_ANTENNA NET
    THIS LINE(X=2898,Y=405) IS INTENTED TO BE CONNECTED BETWEEN RF_ANTENNA AND GND

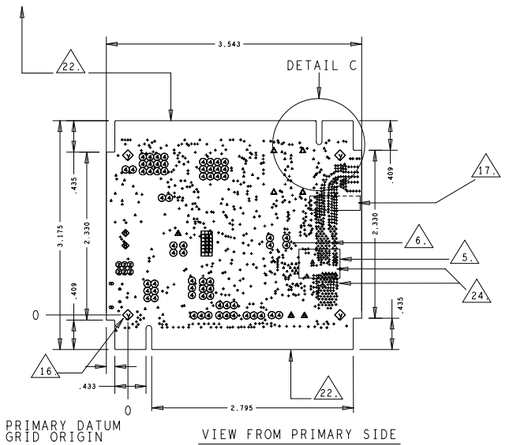
PCI Express Card Egde Connecter Bevel Information.
EDGE CONNECTOR TO BE GOLD PLATED



SCALE: NONE

DETAIL C
SCALE: NONE



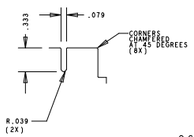


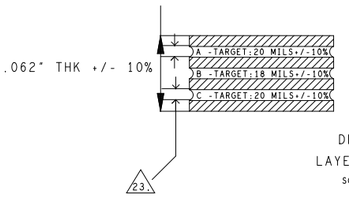
PRIMARY DATUM GRID ORIGIN

VIEW FROM PRIMARY SIDE

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	7.0	+0.0/-8.0	PLATED	76
8 •	8.0	+0.0/-8.0	PLATED	869
◦	12.0	+2.0/-2.0	PLATED	2
ⓟ	28.0	+2.0/-2.0	PLATED	6
ⓙ	31.0	+2.0/-2.0	PLATED	10
ⓐ	40.0	+3.0/-3.0	PLATED	65
▲	63.0	+3.0/-3.0	PLATED	3
◈	35.0	+2.0/-2.0	NON-PLATED	2
△	53.0	+3.0/-0.0	NON-PLATED	4
◇	125.0	+4.0/-4.0	NON-PLATED	4
▪	34.0x30.0	+2.0/-2.0	PLATED	2
▫	59.0x33.0	+2.0/-2.0	PLATED	2

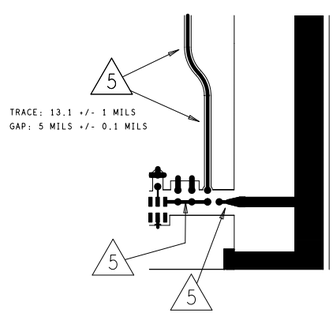
DETAIL C





		FINISHED Cu WEIGHT
LAYER 1	TOP	1 oz.
LAYER 2	L2_GND	1 oz.
LAYER 3	L3_PWR	1 oz.
LAYER 4	BOTTOM	1 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE



DETAIL B
IMPEDANCE REQUIREMENTS

Layers	Single Ended		Differential		
	Trace Width (MILS)	Impedance (Ohms)	Trace Width (MILS)	Trace Pitch center-center (MILS)	Impedance (Ohms)
L1_PS	13.1+/-1mil	50	7	25.5	50

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X FIUO (FREESCALE INTERNAL USE ONLY)
___ FCP (FREESCALE CONFIDENTIAL PROPRIETARY)

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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±0-30'
.XXX ±.005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS	DATE
DRAWN A. QUIROZ	08-14-13
CHECKED F. LATONA	08-14-13
DESIGN ENGINEER A. QUIROZ	08-14-13

PART NO. 170-27846

FREESCALE SEMICONDUCTOR
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
TWR-KW21D256

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-27846	FAB-27846	C

SCALE 1/1 DO NOT SCALE DRAWING SHEET 1 OF 1