TABLE OF CONTENTS

Revisions

Rev	Description	Date	Approved
X1	Initial Release	06/10/13	Ron Kim
X2	Release for schematic review	06/26/2013	Ron Kim
A	Release to production	07/01/2013	Ron Kim
AX1	Respin release to CAD	10/07/2013	Ron Kim
B	Respin release to production	10/14/2013	Ron Kim
BX1	Removing socket	11/12/2013	Ron Kim
C	Socketless version	12/17/2013	Ron Kim
C1	Updating LPUART0 Symbol ref.	04/04/14	Ron Kim

TWR-K22F120M

freescale semiconductor

Microcontroller Solutions Group

6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: FIUO: X PUBI:

Designer: Rafael del Rey	Drawing Title: TWR-K22F120M	
Drawn by: Rafael del Rey	Page Title: TABLE OF CONTENTS	
Approved: Ron Kim	Size: C	Document Number: SCH-27957 PDF: SPF-27957 — Rev: C1
	Date: Monday, April 07, 2014	Sheet 1 of 8

1. Unless Otherwise Specified:
   All resistors are in ohms
   All capacitors are in uF
   All voltages are DC

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

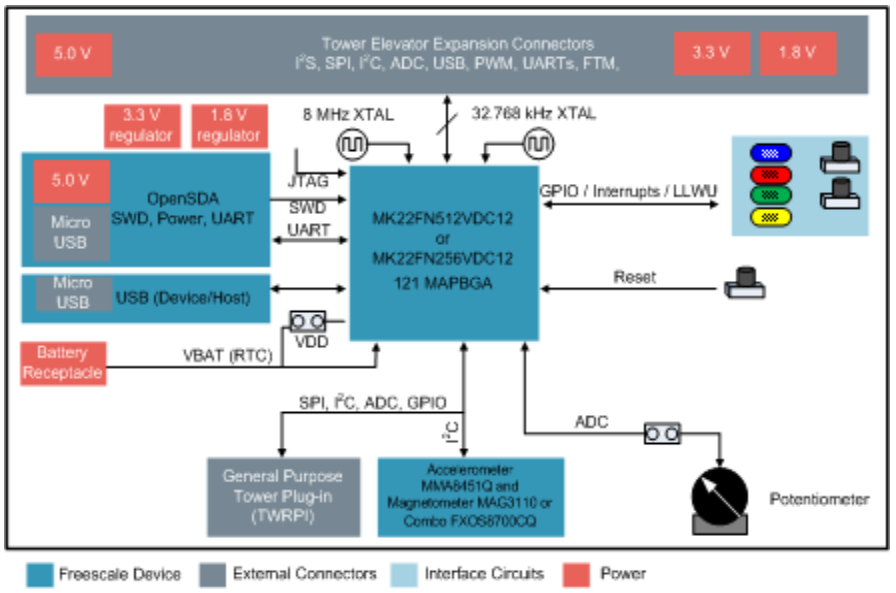
4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Power & Ground Nets

NET	VOLTAGE	DESCRIPTION
P5V_TRG_SDA	5V	Output of USB power switch controlled by the VTRG_EN signal from the OpenSDA and the ELE_PS_SENSE signal from the TWR elevator connectors. Goes to regulator input select header.
USB0_VBUS	5V	USB power from primary elevator Pin A57.
P3V3_VOUT	3.3V	VDD power from the regulator internal to the MCU.
VOUT33_K20	3.3V	Output of OpenSDA's K20 internal regulator to power OpenSDA's circuitry
P5V_ELEV	5V	Power to the elevator boards.
P3V3_REG	3.3V	Output of 3.3V regulator or from the Elevator connectors. May also be supplied externally by connecting to the board voltage select header at pins 1 and 4.
P1V8	1.8V	Output of the 1.8V regulator.
V_BRD	1.8 -3.3V	Output of 1.8v or 3.3V regulators as selected by the board voltage select header. May also be supplied externally by connecting to the board voltage select header at pins 3 and 4.
VREG_IN	5V	Power into the on board voltage regulators.
P5V0_VREGIN_K22	5V	Power into the K21 MCU voltage regulator. It is typically derived from the K21 USB connector or the elevator USB0_VBUS pin.
VBAT	1.8-3.3V	Voltage to the battery input of the MCU. The value depends on whether the board is powered and at what value and the setting of the shunt that selects the source of the battery voltage.
MCU_PWR	1.8-3.3V	MCU digital power. Filtered from V_BRD
MCU_VDD	1.8-3.3V	MCU digital power input after current measurement jumper
VDDA	1.8-3.3V	VDDA power for MCU and analog circuits. Filtered from MCU_PWR.
P3V3_REG	3.3V	Output of regulator U503 or from the Elevator connector
VREFH	3.3V	Upper reference voltage for ADC on the MCU. Filtered from VDDA.
VREFL	0V	Lower reference voltage for ADC on the MCU. Filtered from VSSA.
VSSA	0V	VSSA power for MCU and analog circuits. Filtered from GND.
GND	0V	Digital and Analog Ground.

Block Diagram



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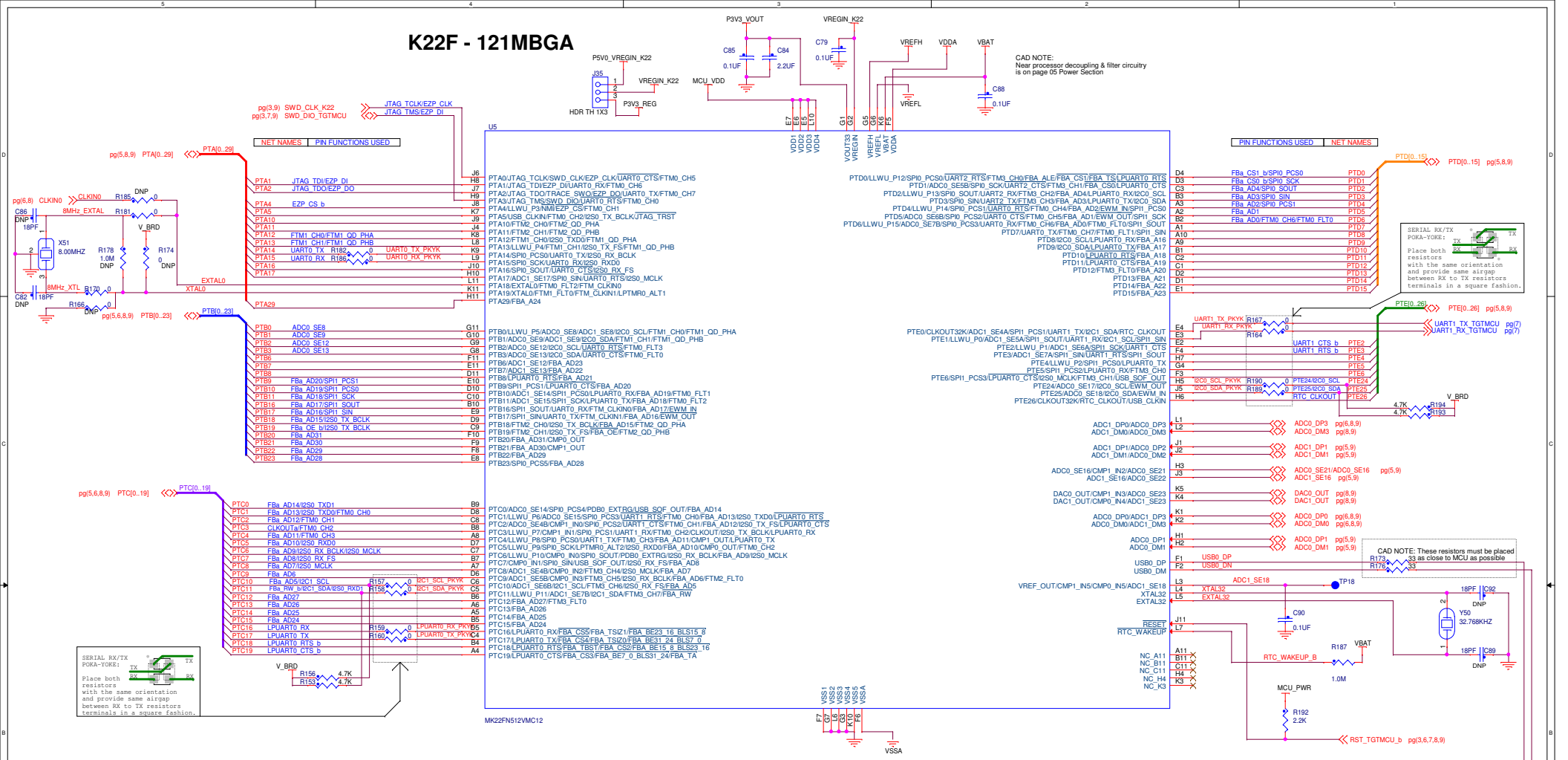
Drawing Title: **TWR-K22F120M**

Page Title: **NOTES & BLOCK DIAGRAM**

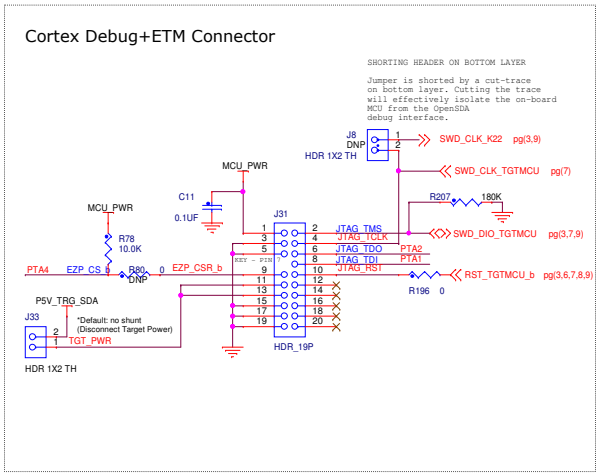
Size	Document Number	Rev
C	SCH-27957 PDF: SPF-27957	C1

Date: Monday, April 07, 2014 Sheet 2 of 8

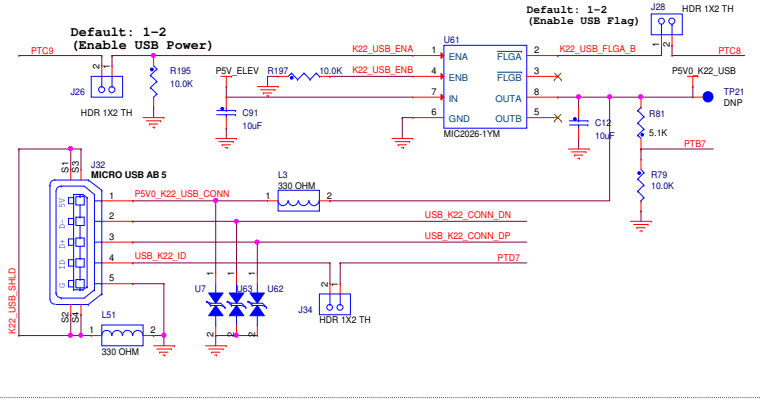
K22F - 121MBGA

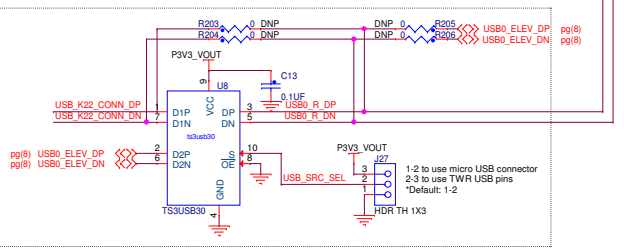


Cortex Debug+ETM Connector



K21 USB Interface (Host, Device, OTG)





For socket interconnection

ADC1_SE18	ADC1_SE18 pg(9)
EXTAL0	EXTAL0 pg(9)
XTAL0	XTAL0 pg(9)
USB0_DP	USB0_DP pg(9)
USB0_DN	USB0_DN pg(9)
XTAL32	XTAL32 pg(9)
EXTAL32	EXTAL32 pg(9)
RTC_WAKEUP_B	RTC_WAKEUP_B pg(9)
PTA4	PTA4 pg(9)
UART1_TX_PKYK	UART1_TX_PKYK pg(9)
UART1_RX_PKYK	UART1_RX_PKYK pg(9)
I2C0_SDA_PKYK	I2C0_SDA_PKYK pg(9)
I2C0_SCL_PKYK	I2C0_SCL_PKYK pg(9)
LPUART0_RX_PKYK	LPUART0_RX_PKYK pg(9)
LPUART0_TX_PKYK	LPUART0_TX_PKYK pg(9)
I2C1_SCL_PKYK	I2C1_SCL_PKYK pg(9)
I2C1_SDA_PKYK	I2C1_SDA_PKYK pg(9)
UART0_TX_PKYK	UART0_TX_PKYK pg(9)
UART0_RX_PKYK	UART0_RX_PKYK pg(9)

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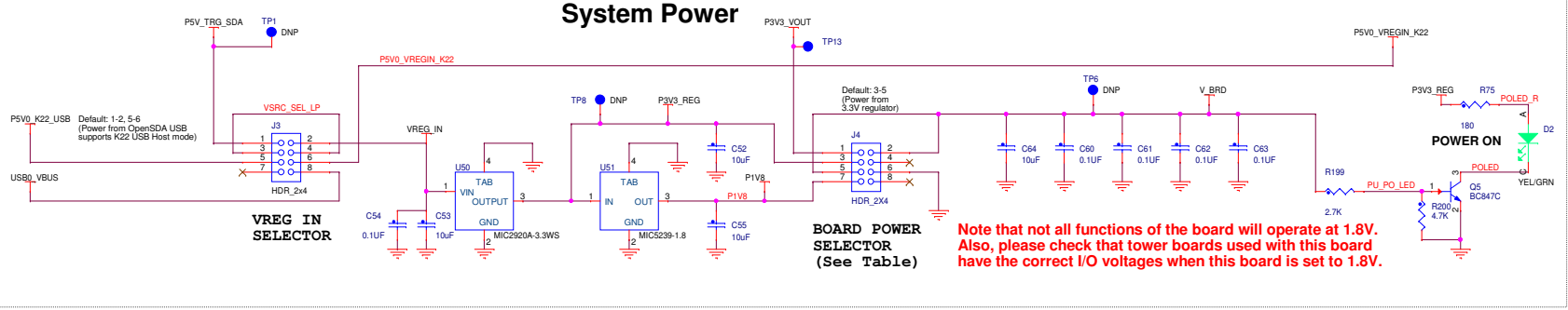
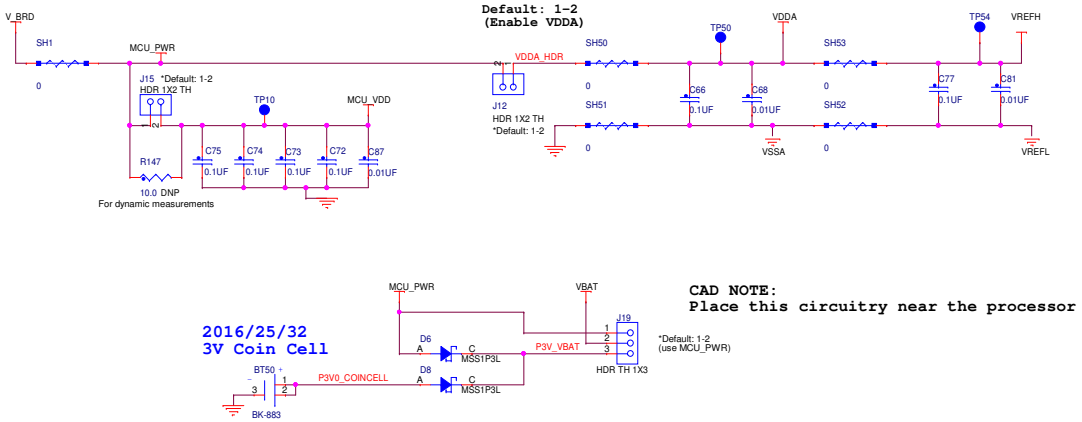
ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	TWR-K22F120M		
Page Title:	PK22FN512VMC12 (121 MBGA)		
Size: C	Document Number: SCH-27957 PDF: SPF-27957		Rev: C1
Date: Wednesday, April 16, 2014	Sheet 3 of 8		

BOARD POWER SELECTOR:	
1-2:	VOUT_3V3 (from MCU)
3-5:	3.3 V from regulator (default)
5-7:	1.8 V from regulator

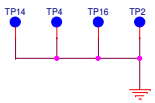
System Power



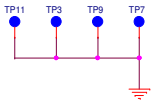
PWR_MCU



GND LOOP TEST PADS



GND LOOP TEST LOOPS



CAD NOTE:
Place ground test loops
in the four corners
away from sensitive signals
that might short
with scope probe alligator clips

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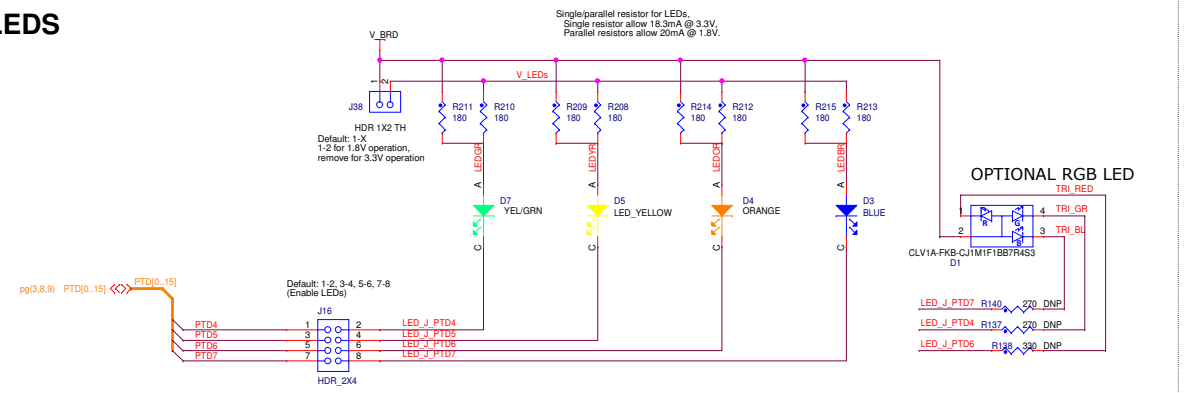
Drawing Title: **TWR-K22F120M**

Page Title: **POWER SECTION**

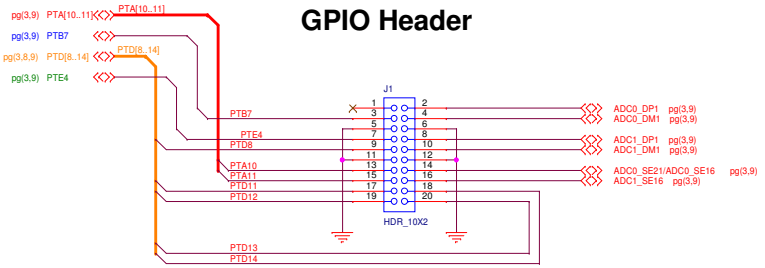
Size	Document Number	Rev
C	SCH-27957 PDF: SPF-27957	C1

Date: Monday, April 07, 2014 Sheet 4 of 8

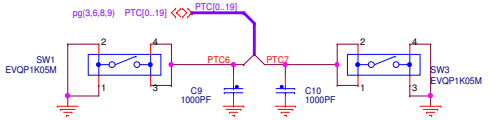
LEDS



GPIO Header



PUSH BUTTONS



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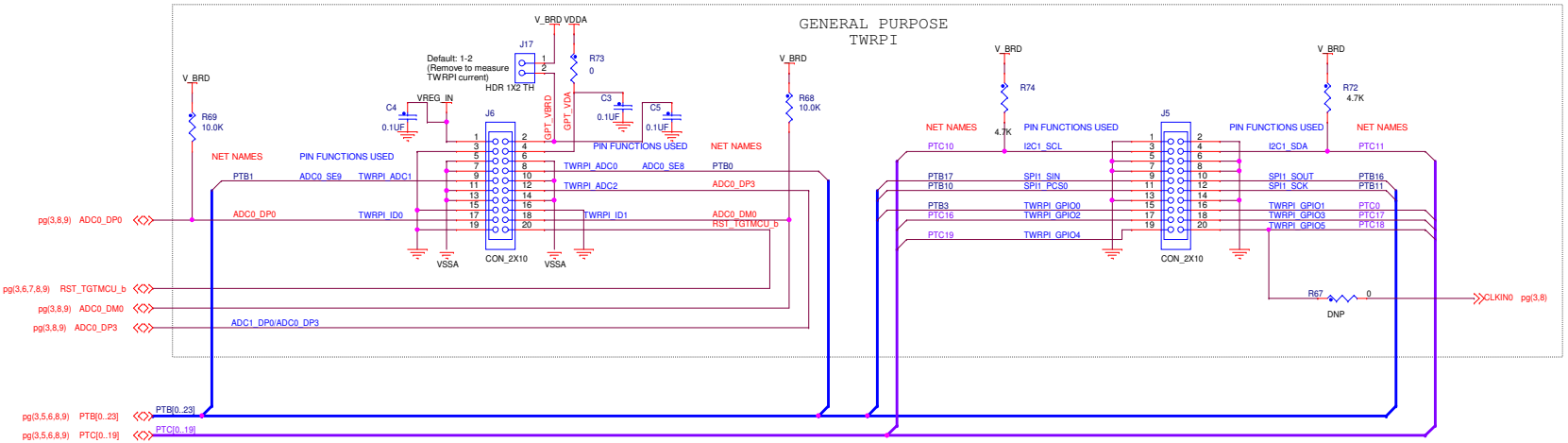
Drawing Title: **TWR-K22F120M**

Page Title: **PERIPHERALS**

Size	Document Number	Rev
C	SCH-27957 PDF: SPF-27957	C1

Date: Monday, April 07, 2014 Sheet 5 of 8

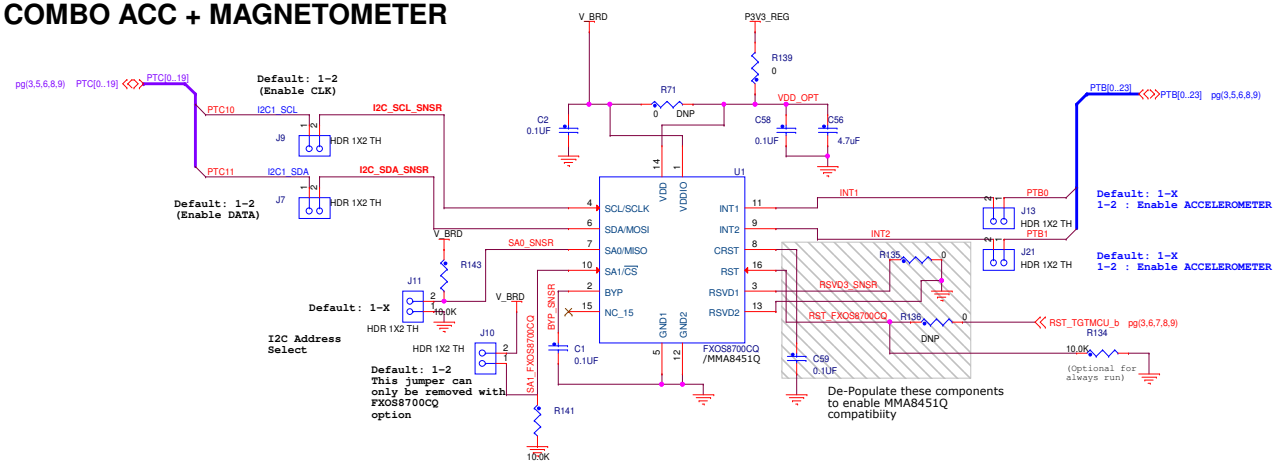


Note: The TWRPI connectors are powered by V_BRD which may be 1.8V or 3.3V.

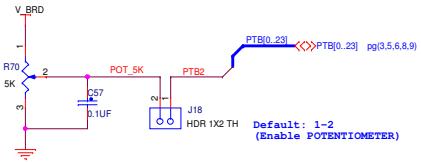
Not all TWRPI boards will work at 1.8V.

Check that TWRPI boards will work at 1.8V before using them with this board when V_BRD is jumpered for 1.8V.

MMA8451Q ACCELEROMETER / FXOS87000CQ COMBO ACC + MAGNETOMETER



POTENTIOMETER



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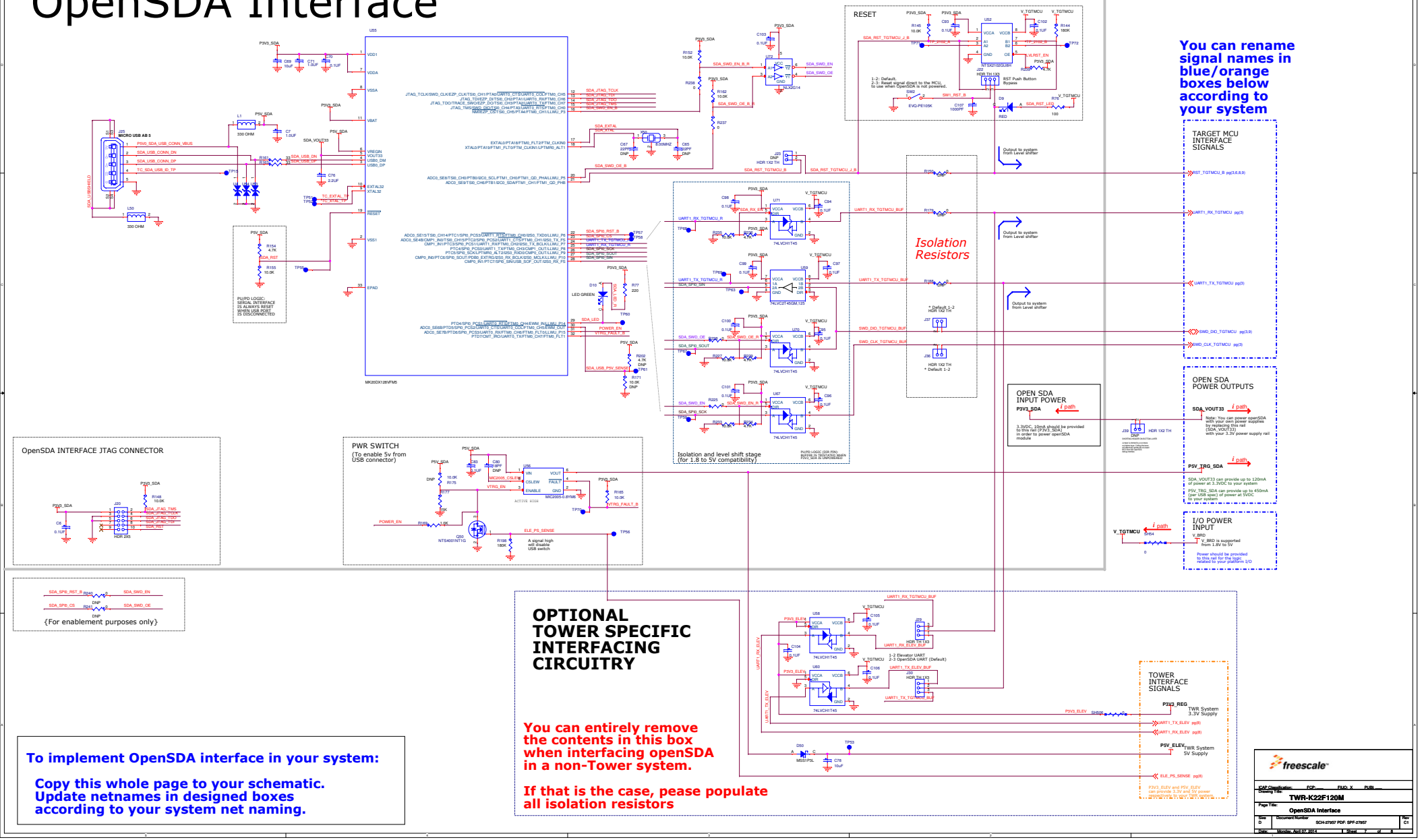
Drawing Title: **TWR-K22F120M**

Page Title: **TWRPI MODULES**

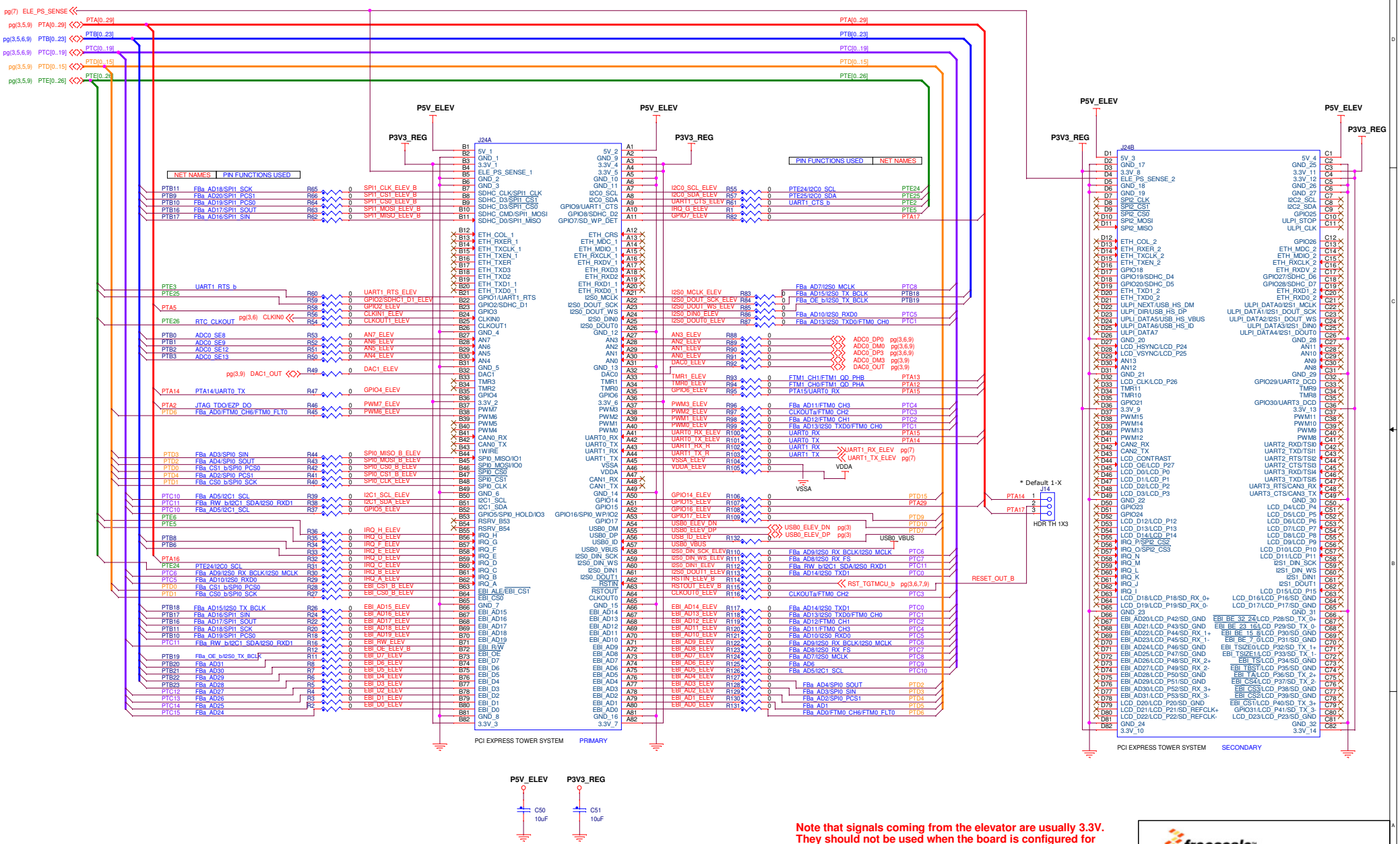
Size	Document Number	Rev
C	SCH-27957 PDF: SPF-27957	C1

Date: Monday, April 07, 2014 Sheet 6 of 8

OpenSDA Interface



ELEVATOR CONNECTOR



Note that signals coming from the elevator are usually 3.3V. They should not be used when the board is configured for 1.8V operation.

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ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___

Drawing Title: **TWR-K22F120M**

Page Title: **ELEVATORS**

Size	Document Number	Rev
C	SCH-27957 PDF: SPF-27957	C1

Date: Monday, April 07, 2014 | Sheet 8 of 8