Design Notes

1) CMC5001 is configured as a Cardstac master card.
2) CPLD Bank 3 is fixed 3.3V I/O
3) Dev OE pin is used as IO, not as reset
4) RST_OUT_n is reset signal from CPLD
5) CPLD_RST_n is the CPLD reset from Power Supply

FID1 FID2 LOGO1

FID3 FID4

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REVISION TABLE

02-25-12	A	ET	Initial release of the schematic.

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File: C:\dallas_logic\altium_dlc\Projects\CMC5001_REVA\1_TOC.SchDoc			

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801 E. Plano Parkway
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Plano TX 75074 USA

Title: ***Cardstac Cntlr., Dual Row, Altera MAX V***		Dallas Logic Corporation 801 E. Plano Parkway Suite 158 Plano TX 75074 USA
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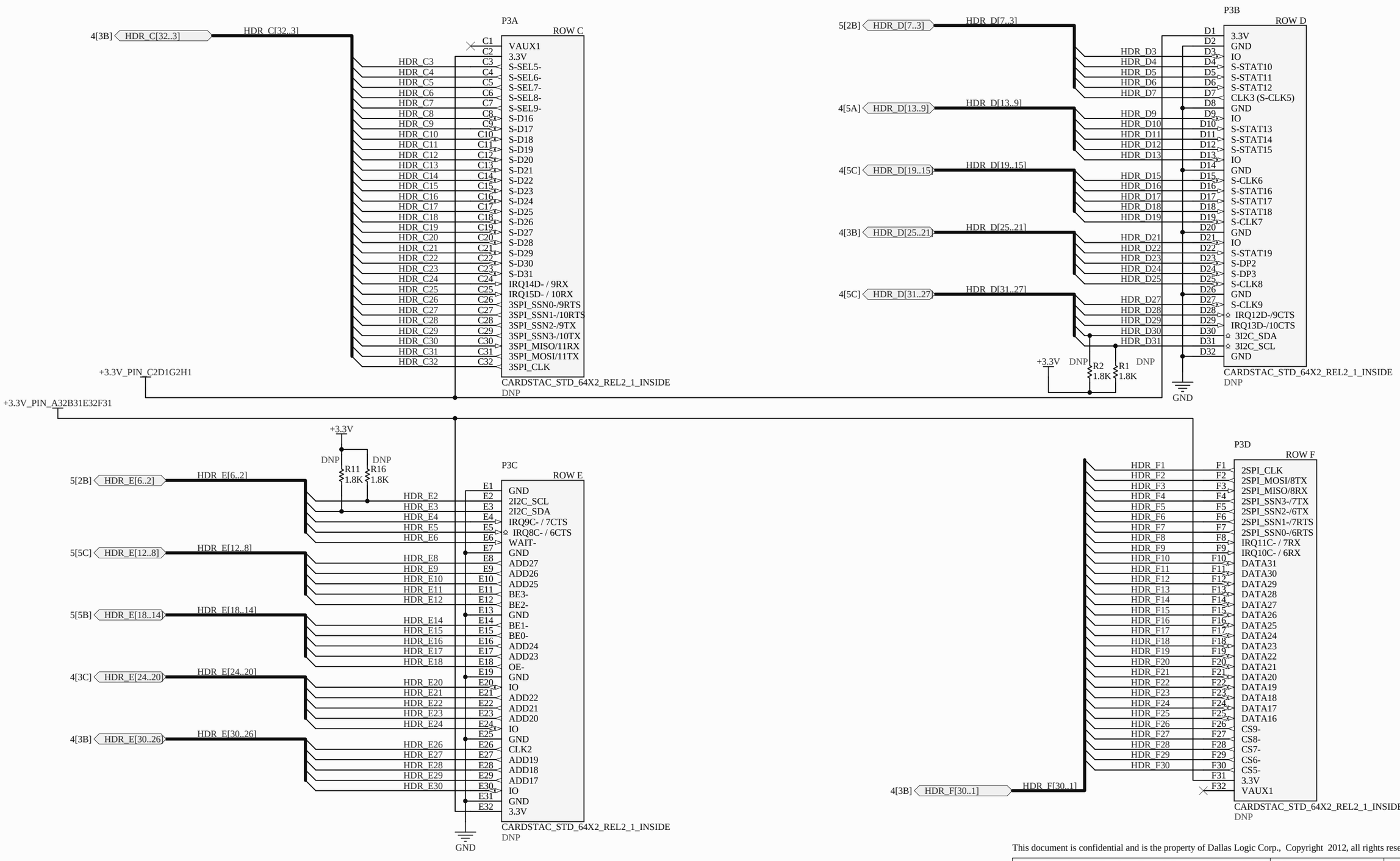

Title	***Cardstac Cntlr., Dual Row, Altera MAX V***		Dallas Logic Corporation 801 E. Plano Parkway Suite 158 Plano TX 75074 USA
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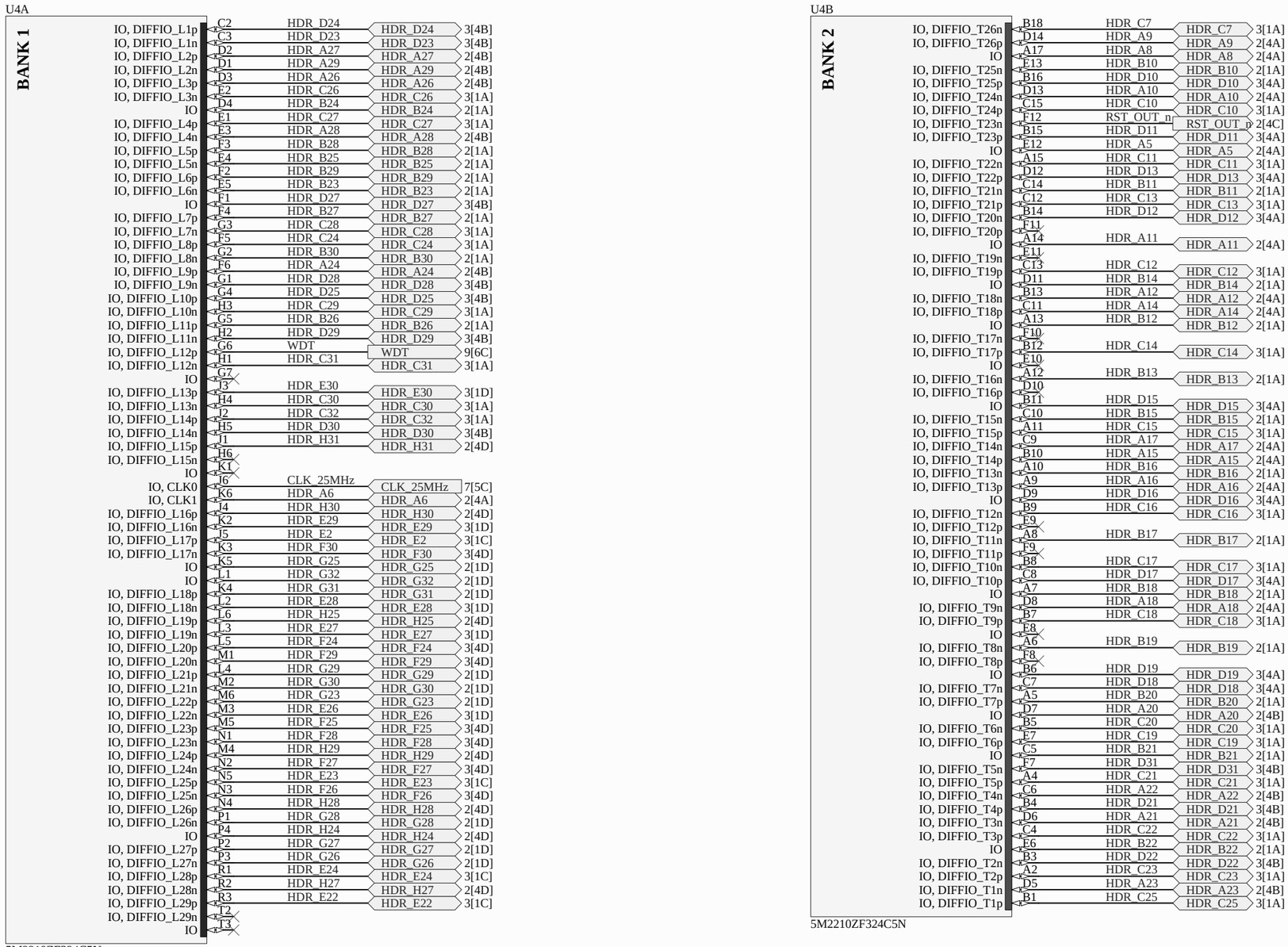

Title	***Cardstac Cntlr., Dual Row, Altera MAX V***		Dallas Logic Corporation 801 E. Plano Parkway Suite 158 Plano TX 75074 USA
Size: B	Number:CMC5001	Revision:A	
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U4C

BANK 3

IO, DIFFIO_R32n	T17	EEPROM3_WP_N	7[1C]
IO, DIFFIO_R32p	R15	EEPROM3_CLK	7[1C]
IO, DIFFIO_R31n	T16	EEPROM3_HOLD_N	7[1D]
IO, DIFFIO_R31p	R16	EEPROM3_SO	7[2C]
IO, DIFFIO_R30n	P15	EEPROM1_HOLD_N	7[1A]
IO, DIFFIO_R30p	R17	EEPROM3_CS_N	7[1C]
IO, DIFFIO_R29n	P14	LED_YEL	8[1C]
IO, DIFFIO_R29p	R18	EEPROM3_SI	7[1C]
IO, DIFFIO_R28n	N15	SW1	8[4A]
IO, DIFFIO_R28p	P16	EEPROM1_WP_N	7[1A]
IO	N14	LED_GRN	8[1C]
IO, DIFFIO_R27n	P17	EEPROM1_SO	7[2A]
IO, DIFFIO_R27p	N13	TEMP_CLK	8[4A]
IO, DIFFIO_R26n	P18	EEPROM1_CS_N	7[1A]
IO, DIFFIO_R26p	M15	EEPROM2_SO	7[2B]
IO, DIFFIO_R25n	N16	EEPROM2_CS_N	7[1B]
IO, DIFFIO_R25p	M14	EEPROM2_HOLD_N	7[1B]
IO, DIFFIO_R24n	N17	EEPROM1_CLK	7[1A]
IO, DIFFIO_R24p	M13	TEMP_CSN	8[4A]
IO, DIFFIO_R23n	N18	SW2	8[4B]
IO, DIFFIO_R23p	M12	LED_RED	8[1C]
IO	M16	EEPROM2_CLK	7[1B]
IO, DIFFIO_R22n	L16	SW3	8[4C]
IO, DIFFIO_R22p	M17	EEPROM2_WP_N	7[1B]
IO, DIFFIO_R21n	L15	EEPROM2_SI	7[1B]
IO, DIFFIO_R21p	M18	EEPROM1_SI	7[1A]
IO, DIFFIO_R20n	L14	TEMP_SIO	8[4A]
IO, DIFFIO_R20p	L17	HDR_G4	2[1D]
IO, DIFFIO_R19n	L13	HDR_E8	3[1C]
IO, DIFFIO_R19p	L18	HDR_F4	3[4D]
IO, DIFFIO_R18n	K16	HDR_F5	3[4D]
IO, DIFFIO_R18p	K17	HDR_F3	3[4D]
IO	K15	HDR_E3	3[1C]
IO, DIFFIO_R17n	K18	HDR_E5	3[1C]
IO, DIFFIO_R17p	K14	HDR_F6	3[4D]
IO, CLK2	K13	HDR_D7	3[4A]
IO, CLK3	J13	HDR_E6	3[1C]
IO, DIFFIO_R16n	J18	HDR_F1	3[4D]
IO, DIFFIO_R16p	J14	HDR_G3	2[1D]
IO, DIFFIO_R15n	J17	HDR_E4	3[1C]
IO, DIFFIO_R15p	J15		
IO, DIFFIO_R14n	H18	HDR_F2	3[4D]
IO, DIFFIO_R14p	J16		
IO, DIFFIO_R13n	H17	HDR_D3	3[4A]
IO, DIFFIO_R13p	H13		
IO, DIFFIO_R12n	G18	HDR_B1	2[1A]
IO, DIFFIO_R12p	H14		
IO, DIFFIO_R11n	G17	HDR_C3	3[1A]
IO, DIFFIO_R11p	H15	HDR_D5	3[4A]
IO	G16	HDR_C4	3[1A]
IO, DIFFIO_R10n	H16	HDR_D4	3[4A]
IO, DIFFIO_R10p	F18	HDR_B2	2[1A]
IO, DIFFIO_R9n	G12		
IO, DIFFIO_R9p	F17	HDR_B3	2[1A]
IO	G13		
IO, DIFFIO_R8n	F16	HDR_D6	3[4A]
IO, DIFFIO_R8p	G14		
IO, DIFFIO_R7n	F18		
IO, DIFFIO_R7p	G15	HDR_B5	2[1A]
IO, DIFFIO_R6n	E17	HDR_C5	3[1A]
IO, DIFFIO_R6p	F13	HDR_A2	2[4A]
IO, DIFFIO_R5n	D18	HDR_B4	2[1A]
IO, DIFFIO_R5p	F14	HDR_D9	3[4A]
IO, DIFFIO_R4n	E16	HDR_C6	3[1A]
IO, DIFFIO_R4p	F15	HDR_B9	2[1A]
IO	D17	HDR_B6	2[1A]
IO, DIFFIO_R3n	E14	HDR_A3	2[4A]
IO, DIFFIO_R3p	D16	HDR_C8	3[1A]
IO, DIFFIO_R2n	C16	HDR_B8	2[1A]
IO, DIFFIO_R2p	E15	HDR_A4	2[4A]
IO, DIFFIO_R1n	C17	HDR_B7	2[1A]
IO, DIFFIO_R1p	D15	HDR_C9	3[1A]

5M2210ZF324C5N

U4D

BANK 4

IO, DIFFIO_B1p	U1	HDR_G24	2[1D]
IO, DIFFIO_B1n	V2	HDR_E21	3[1C]
IO	R5	HDR_F22	3[4D]
IO, DIFFIO_B2p	U3	HDR_H23	2[4D]
IO, DIFFIO_B2n	P6	HDR_F21	3[4D]
IO, DIFFIO_B3p	T4	HDR_G22	2[1D]
IO, DIFFIO_B3n	R6	HDR_G21	2[1D]
IO, DIFFIO_B4p	U4	HDR_E20	3[1C]
IO, DIFFIO_B4n	T6	HDR_F19	3[4D]
IO	V4	HDR_H22	2[4D]
IO, DIFFIO_B5p	N7	HDR_F23	3[4D]
IO, DIFFIO_B5n	T5	HDR_H21	2[4D]
IO, DIFFIO_B6p	P7	HDR_H19	2[4C]
IO, DIFFIO_B6n	U5	HDR_F20	3[4D]
IO, DIFFIO_B7p	R7	HDR_F18	3[4D]
IO, DIFFIO_B7n	V5	HDR_G20	2[1D]
IO	T7	HDR_G18	2[1D]
IO, DIFFIO_B8p	U6	HDR_G19	2[1D]
IO, DIFFIO_B8n	N8	HDR_G16	2[1D]
IO, DIFFIO_B9p	V6	HDR_E18	3[1C]
IO, DIFFIO_B9n	P8	HDR_E17	3[1C]
IO, DIFFIO_B10p	U7	HDR_H18	2[4C]
IO, DIFFIO_B10n	R8	HDR_F17	3[4D]
IO, DIFFIO_B11p	T8	HDR_H16	2[4C]
IO, DIFFIO_B11n	U8	HDR_G17	2[1D]
IO, DIFFIO_B12p	P9	HDR_G13	2[1D]
IO, DIFFIO_B12n	V8	HDR_H17	2[4C]
IO, DIFFIO_B13p	R9	HDR_G15	2[1D]
IO, DIFFIO_B13n	U9	HDR_E16	3[1C]
IO	T9	HDR_H15	2[4C]
IO, DIFFIO_B14p	V9	HDR_F16	3[4D]
IO, DIFFIO_B14n	U10	HDR_E15	3[1C]
IO, DIFFIO_B15p	V10	HDR_F15	3[4D]
IO, DIFFIO_B15n	P10	HDR_H11	2[4C]
IO	U11	HDR_H12	2[4C]
IO, DEV_OE, DIFFIO_B16p	N9	HDR_E14	3[1C]
IO, DEV_CLRn, DIFFIO_B16n	N10	CPLD_RST_n	9[6C]
IO, DIFFIO_B17p	R10	HDR_H13	2[4C]
IO, DIFFIO_B17n	V11	HDR_F14	3[4D]
IO, DIFFIO_B18p	T10	HDR_G14	2[1D]
IO, DIFFIO_B18n	U12	HDR_F12	3[4D]
IO, DIFFIO_B19p	N11	HDR_E9	3[1C]
IO, DIFFIO_B19n	V12	HDR_F13	3[4D]
IO	P11	HDR_G8	2[1D]
IO, DIFFIO_B20p	U13	HDR_E12	3[1C]
IO, DIFFIO_B20n	R11	HDR_G9	2[1D]
IO, DIFFIO_B21p	V13	HDR_G11	2[1D]
IO, DIFFIO_B21n	T11	HDR_G12	2[1D]
IO, DIFFIO_B22p	T14	HDR_E10	3[1C]
IO, DIFFIO_B22n	N12	HDR_G5	2[1D]
IO	U14	HDR_G10	2[1D]
IO, DIFFIO_B23p	P12	HDR_F10	3[4D]
IO, DIFFIO_B23n	V14	HDR_F11	3[4D]
IO, DIFFIO_B24p	R12	HDR_H7	2[4C]
IO, DIFFIO_B24n	T15	HDR_H5	2[4C]
IO, DIFFIO_B25p	T12	HDR_H10	2[4C]
IO, DIFFIO_B25n	U15	HDR_F9	3[4D]
IO	P13	HDR_F7	3[4D]
IO, DIFFIO_B26p	V15	HDR_H9	2[4C]
IO, DIFFIO_B26n	R13	HDR_H6	2[4C]
IO, DIFFIO_B27p	U16	HDR_F8	3[4D]
IO, DIFFIO_B27n	T13	HDR_E11	3[1C]
IO, DIFFIO_B28p	V17	HDR_G7	2[1D]
IO, DIFFIO_B28n	U18	HDR_H4	2[4C]
IO	R14	HDR_G6	2[1D]

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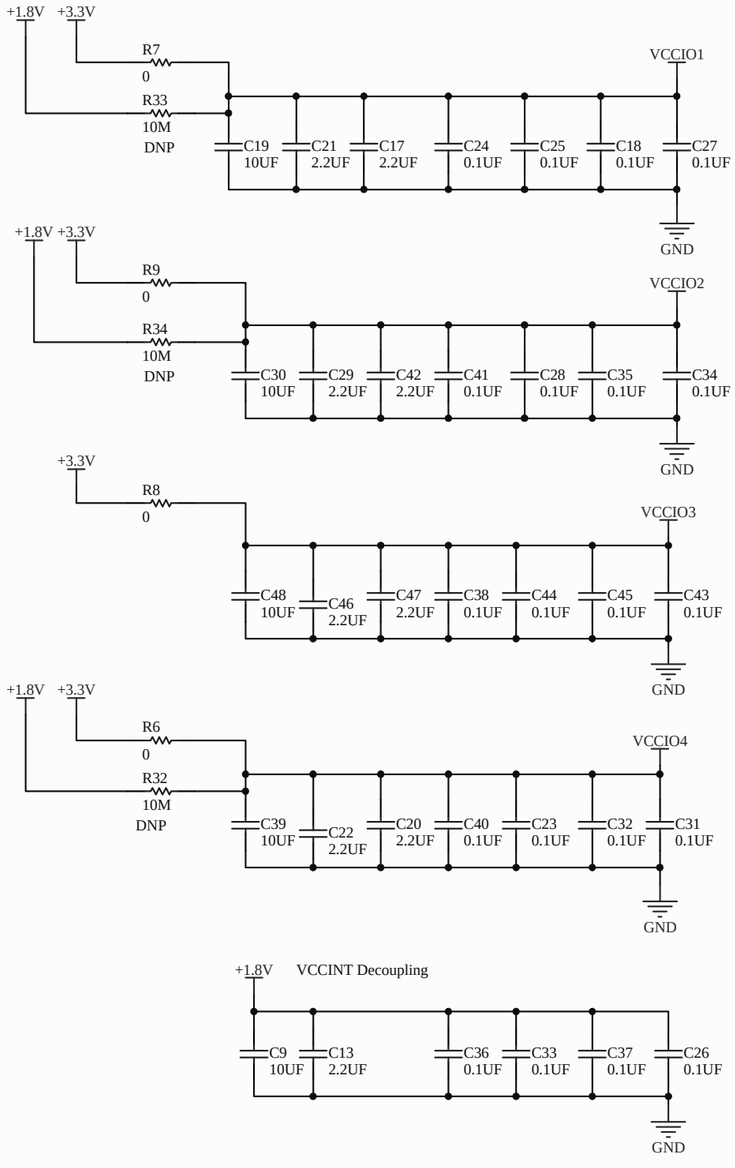
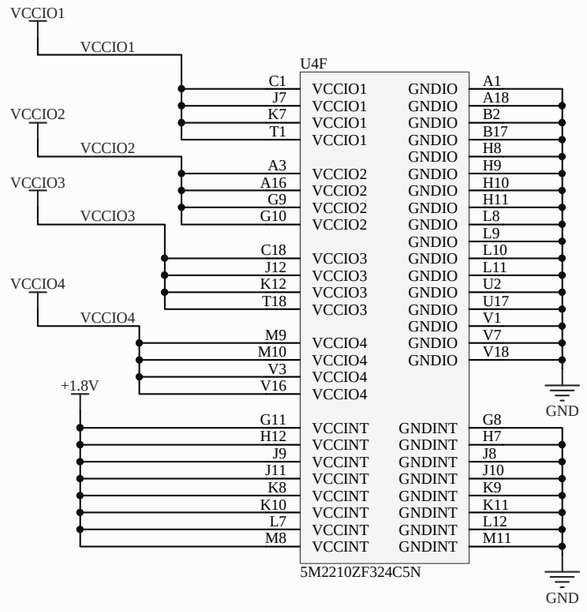
Default power configuration is 3.3V IO.

Remove top-side resistor and install bottom side resistor to support 1.8V IO.





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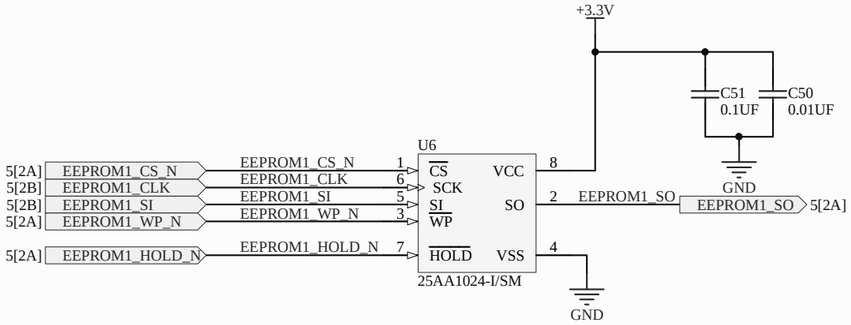

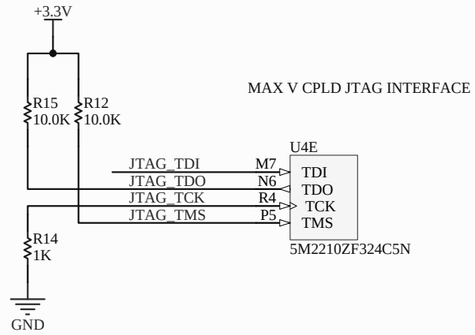

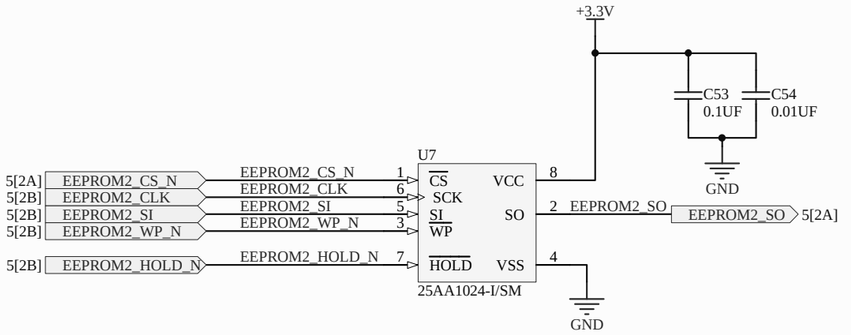

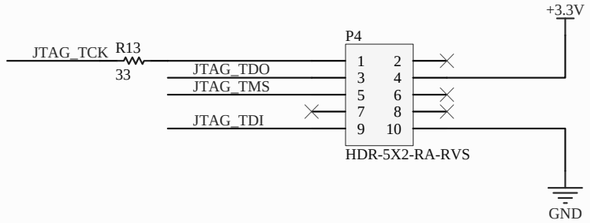

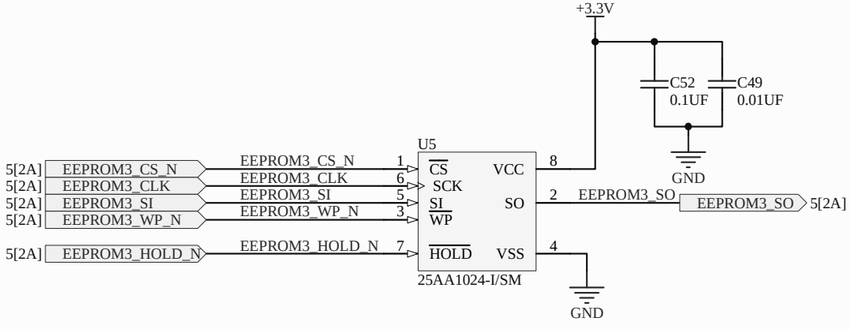

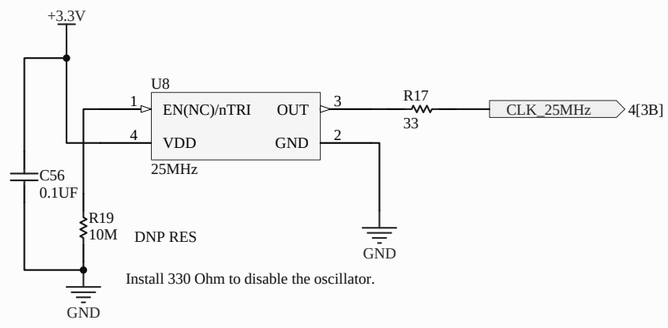

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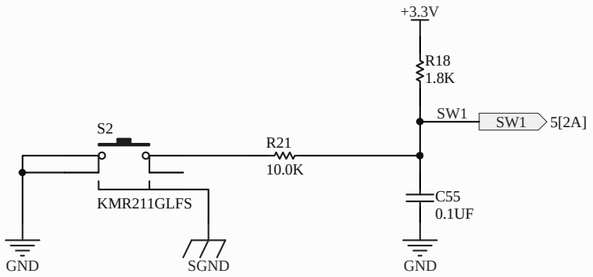

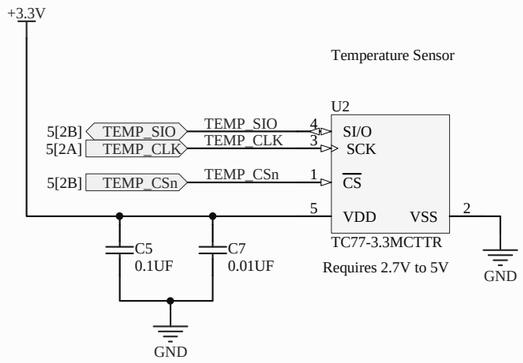

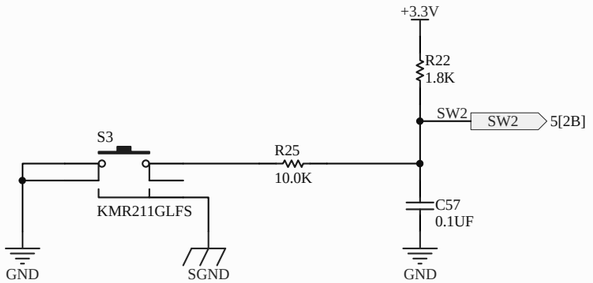

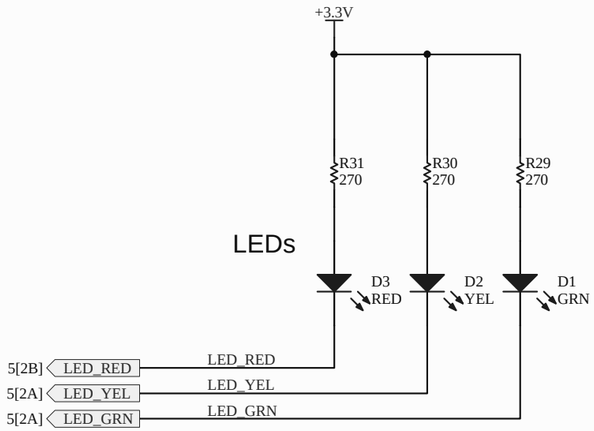

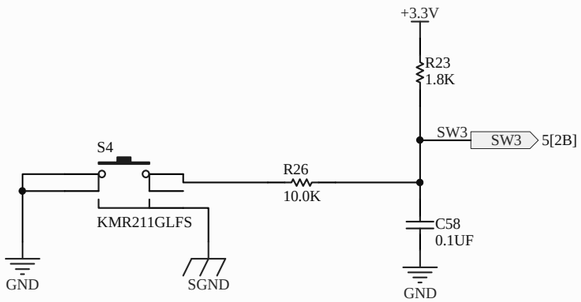

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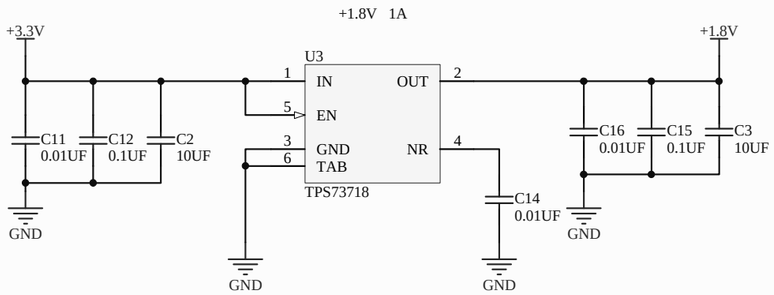
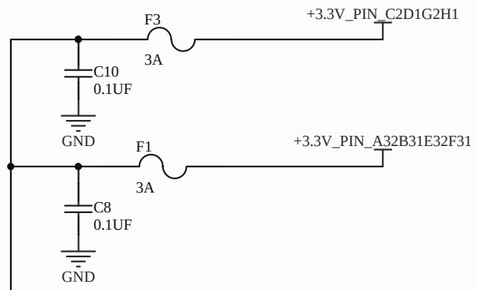
POWER SUPPLY



Remove fuses if other card in stack sources 3.3V power rail and local DCJACK is attached and powered (should not do this).
CMC5001 may also pull current in from 3.3V pin (local power from external source via header pins).

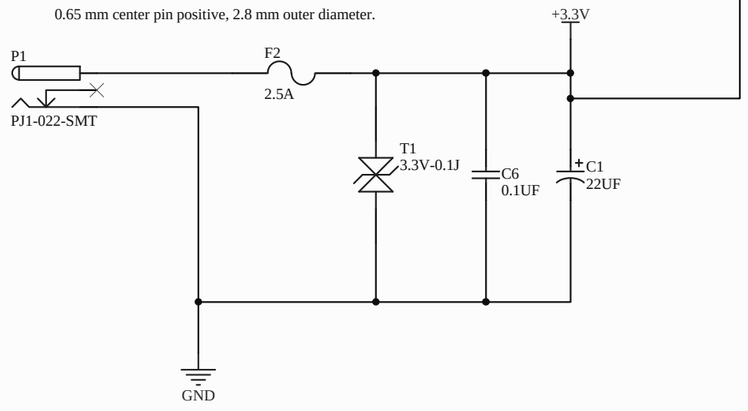


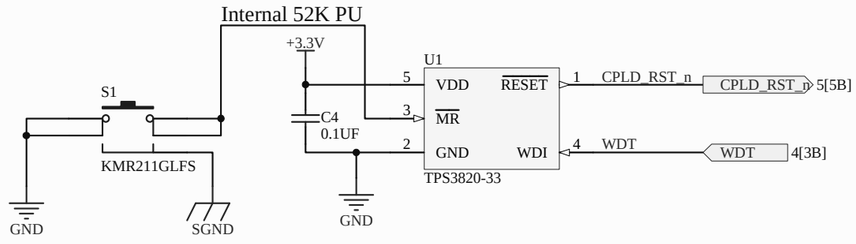
Design limit per set of four pins is 3A. DC Jack fuse will blow before these will.

DC JACK

INPUT: +3.3V, 2.5A Max.

0.65 mm center pin positive, 2.8 mm outer diameter.





SGND (Shield GND or guard ring) connected to ground power pins at two corners of module.

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