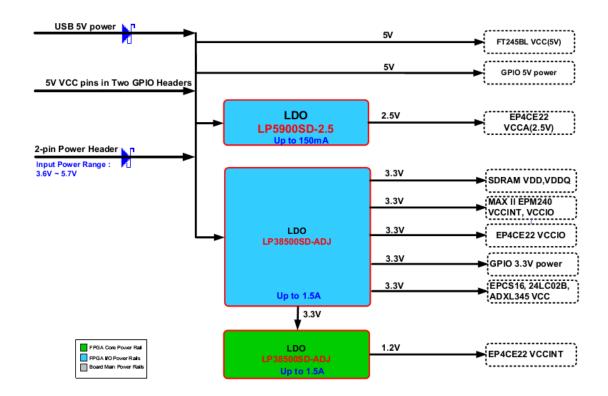
DA D%), \$'fDE0-NanoLTest Report

Contents

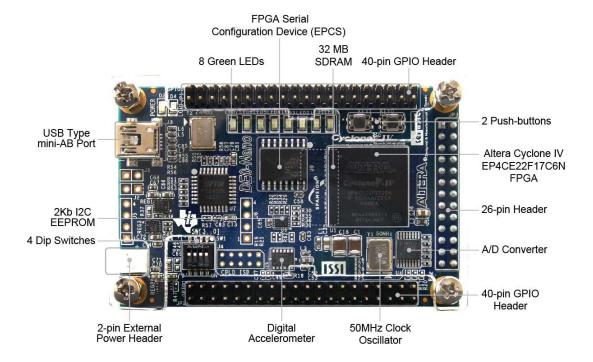
Power Tree Block Diagram
Board Photos
Power-up Sequence
Output Ripple Voltage (Full Load)
Load Regulation

1) Power Tree Block Diagram

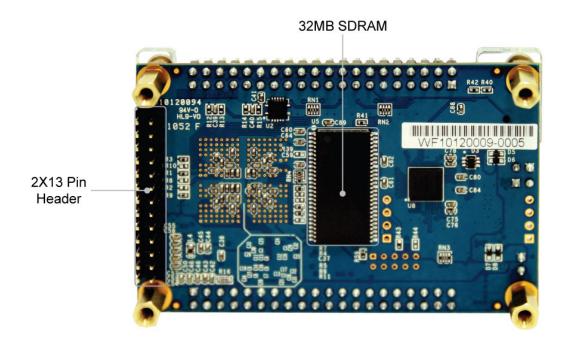


2) Board Photos

Top View

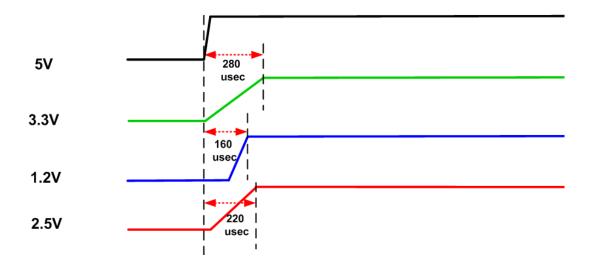


Bottom View



3) Power-up Sequence

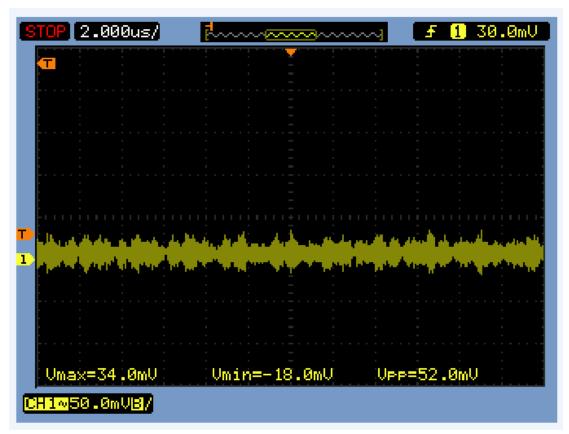
DE0-Nano Power-up Sequence



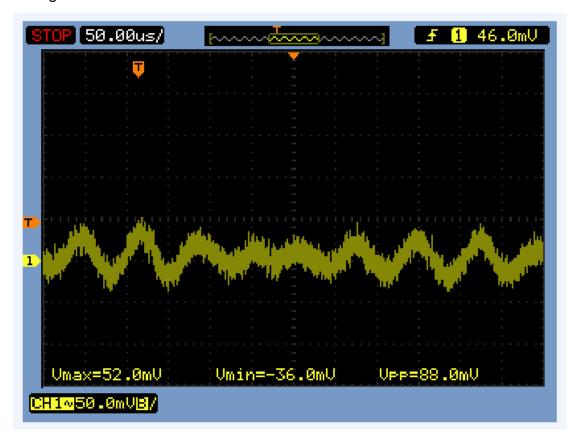
4) Output Voltage Ripple

The images below shows the output voltage ripple when load is fully applied.

LP38500SD-ADJ: VIN = 3.3V, VOUT = 1.2V, IOUT = 0.9A Output Ripple Voltage

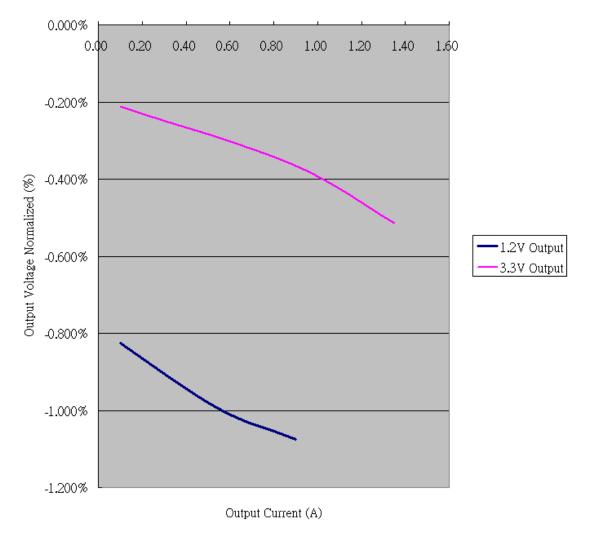


LP38500SD-ADJ: VIN = 5V, VOUT = 3.3V, IOUT = 1.35A Output Ripple Voltage



5) Load Regulation

The images below show the output load regulation. The input voltages are 3.3V and 5V for 1.2V and 3.3V outputs, respectively.



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