Helen Chen

TI Designs: PMP9770 Reference Guide

LCD Bias Power Reference Design with TPS61085

TEXAS INSTRUMENTS

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Circuit Description

This reference design delivers a low cost LCD bias power circuit using the boost converter IC TPS61085. The solution provides all four voltages required by the thin film transistor (TFT) LCD display. The TPS61085 boost converter generates the AVDD voltage. Two external charge pump circuits provide the positive VGH and negative VGL bias voltage for the TFT. One external op-amp LM7321MF acts as a high current buffer, it provides the VCOM voltage for the TFT backplane.

Design Resources

Design Page	All Design files
TPS61085	Product Folder
LM7321	Product Folder

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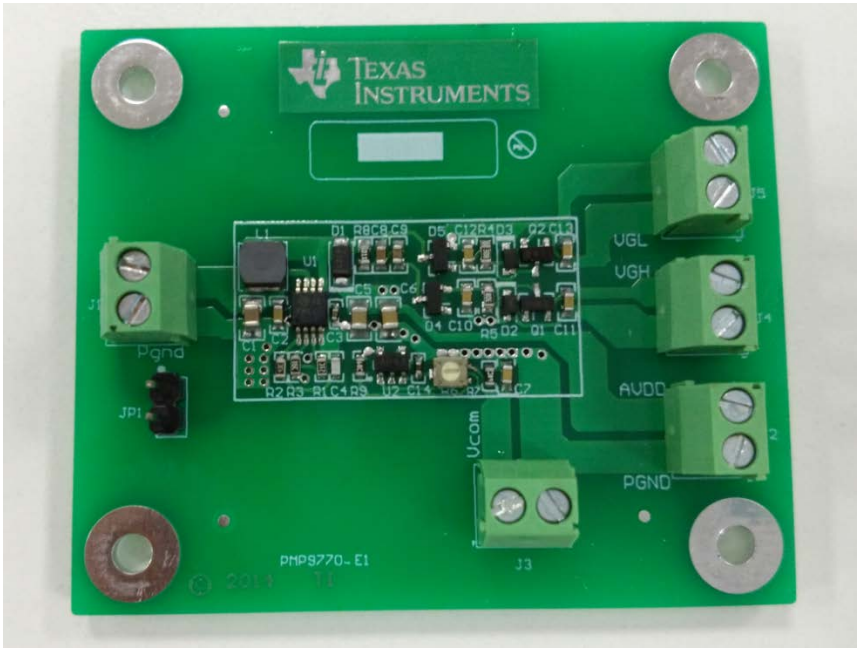

1 Introduction

There already exists some IC which can offer an integrated solution to meet all the voltages required by thin film transistor (TFT) LCD displays. But this kind of IC usually is expensive. So, some customers prefer cheap discrete solution yet hope to keep the small size at the same time.

This reference design illustrates a low cost discrete solution which can meet all the voltage requirements for TFT LCD displays with the TPS61085 and other external components. Additionally, a high current buffer realized by the LM7321MF is also provided for the TFT backplane.

2 LCD Bias Power Reference Design with TPS61085

2.1 Power Specification

The following table gives out the input voltage (Vin) range and all the voltages required by a TFT LCD display. This is the design target for this reference design.

Table 1. Input & Output Parameter

	Voltage	Maximum Current
Vin	2.7-3.9V	--
AVDD	10V	100mA
VGH	17V	10mA
VGL	-7V	10mA
VCOM	5V	20mA

2.2 Reference Design Schematic

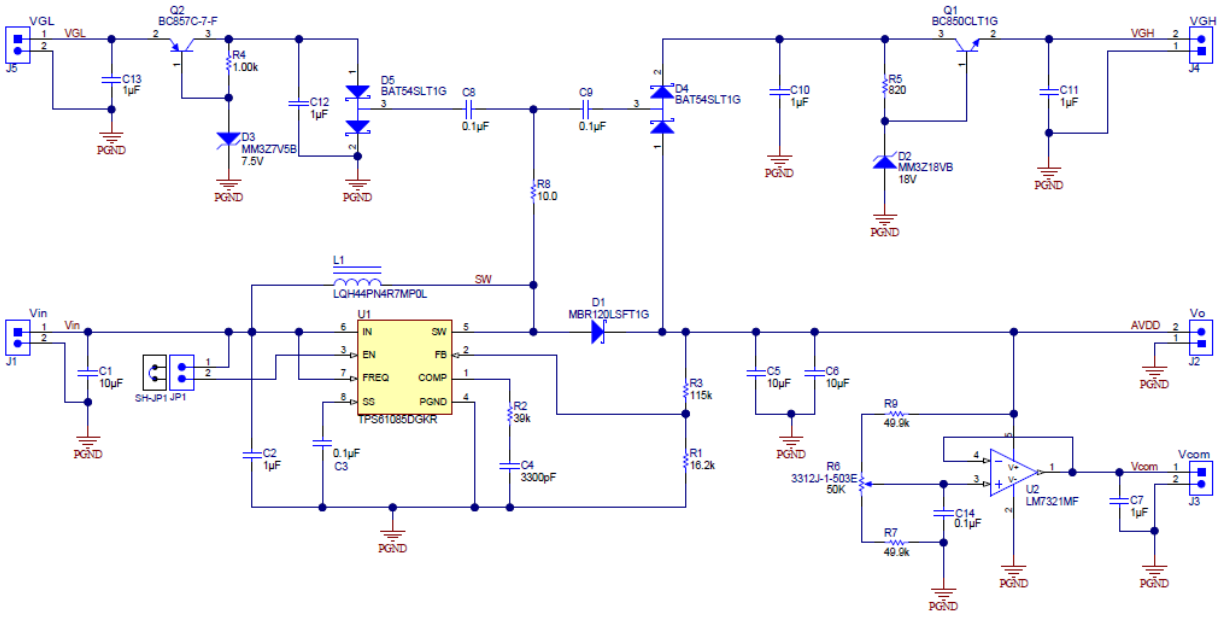

Figure 1. Schematic for LCD bias power with TPS61085

2.3 Frequency Selection

FREQ is the frequency selection pin. The TPS61085 operates at 650kHz when the FREQ pin is connected to the GND pin and at 1.2MHz when the FREQ pin is connected to the IN pin. In this reference design, 1.2MHz frequency is preferred because higher frequency results in smaller inductor size and capacitor size.

2.4 Inductor Selection

The main parameter of a inductor is the saturation current. The saturation current of the selected inductor should be higher than the peak switch current at heavy load (including load transients).

$$P_{o(\max)} = P_{AVDD} + P_{VGH} + P_{VGL} + P_{VCOM} = 1.34W \quad (1)$$

As the total output power is small, we can take the inductor ripple current about 60% of the average inductor current. Suppose efficiency ƞ=0.8, then the peak switch current is:

$$I_{in(peak)} = I_{in(avg)} + I_{in(avg)} \cdot \frac{0.6}{2} = \frac{P_{o(\max)}}{V_{in(\min)} \cdot \eta} \cdot \left(1 + \frac{0.6}{2}\right) = 0.806A \quad (2)$$

Considering 20% margin, the saturation current should be higher than 1A.

The inductor value can be calculated by the following equation:

$$L = \left(\frac{V_{in(\min)}}{V_o}\right)^2 \cdot \left(\frac{V_o - V_{in(\min)}}{I_o \cdot f_s}\right) \cdot \left(\frac{\eta}{0.6}\right) \approx 4.7uH \quad (3)$$

Where:

Vin(min)	Minimum input voltage
Vo	Output voltage AVDD(10V)
Io	Maximum output current equivalent at AVDD(Vo=10V)
fs	Switching frequency(1.2MHz)

Another important factor is the inductor type. At high switching frequencies of 1.2 MHz, inductor core loss, proximity effect and skin effect become very important, the self-resonant frequency of the inductor should be higher than the 1.2MHz operation frequency. Finally, the DC resistance (DCR) should be as low as possible to minimize the power loss.

2.5 Output Voltage Setting of AVDD, VGH, VGL & VCOM

The output voltage AVDD is set by an external resistor divider R1 and R3 (Figure 1). Typically, a minimum current of 50 μA flowing through the feedback divider gives good accuracy. Using 16.2KΩ resistance for R1, R3 can be calculated as:

$$R_3 = R_1 \cdot \left(\frac{V_o}{V_{FB}} - 1\right) \approx 115k\Omega \quad (4)$$

Vo	Output voltage AVDD (10V)

V_{FB} Feedback regulation voltage (1.238V)

The output voltage VGH is calculated as:

$$V_{GH} = V_{Z(D2)} - V_{Q1(be)} \quad (5)$$

$V_{Z(D2)}$ Zener diode D2 voltage

$V_{Q1(be)}$ NPN transistor Q1's base-emitter voltage

To meet VGH = 17V target, a 18V rating, ±2% tolerance zener diode MM3Z18VB is selected as D2. From Vz VS. Iz curve, the zener voltage from Iz=2mA to Iz=5mA is nearly the same. Considering the conversion efficiency, 2.1mA Iz is selected in this design:

$$I_{Z(D2)} = \frac{(2V_o - V_d) - V_{Z(D2)}}{R_5} \approx 2.1mA \quad (6)$$

Vo Output voltage AVDD (10V)

Vd The voltage drop of D4 (BAT54SLT1G), Vd=0.32V @ 25°C

R5 810 Ω

The temperature coefficient (Sz) of the MM3Z18VB is 14.4mV/K, so the minimum zener voltage at -25°C and the maximum zener voltage at 85°C is:

$$V_{D2(\min)} = 18 - 0.0144 \times 50 = 17.28V \quad (7)$$

$$V_{D2(\max)} = 18 + 0.0144 \times 60 = 18.86V \quad (8)$$

NPN transistor Q1's base-emitter voltage (by the test) Vbe = 0.78V at -25°C, and Vbe = 0.499V at 85°C , so:

$$V_{GH(\min)} = 17.28 - 0.78 = 16.5V \quad (9)$$

$$V_{GH(\max)} = 18.86 - 0.499 = 18.36V \quad (10)$$

The output voltage VGL is calculated as:

$$V_{GL} = -V_{Z(D3)} + V_{Q2(eb)} \quad (11)$$

$V_{Z(D3)}$ Zener diode D3 voltage

$V_{Q2(eb)}$ PNP transistor Q2's emitter-base voltage

To meet VGL = -7V target, a 7.5V rating, ±2% tolerance zener diode MM3Z7V5B is selected as D3. The working current Iz of D3 is calculated as:

$$I_{Z(D3)} = \frac{(V_o - V_d) - V_{Z(D3)}}{R_4} \approx 2.2mA \quad (12)$$

$V_{Z(D3)}$ Zener diode D3 (MM3Z7V5B) voltage, $V_{Z(D3)}$ =7.5V @ 25°C

R4 1kΩ

The temperature coefficient (Sz) of the MM3Z7V5B is 4mV/K, so the minimum zener voltage at -25°C and the maximum zener voltage at 85°C is:

$$V_{D3(\min)} = 7.5 - 0.004 \times 50 = 7.3V \quad (13)$$

$$V_{D3(\max)} = 7.5 + 0.004 \times 60 = 7.74V \quad (14)$$

PNP transistor Q2's emitter-base voltage (by the test) Veb=0.783V at -25°C, and Veb=0.495V at 85°C, so:

$$V_{GL(\min)} = -7.74 + 0.495 = -7.245V \quad (15)$$

$$V_{GL(\max)} = -7.3 + 0.783 = -6.517V \quad (16)$$

The output voltage VCOM is set by the resistor R7, R9 and the potentiometer R6. Adjusting R6 gets the required 5V output of the VCOM buffer.

2.6 Output Capacitor Selection

The output cap C5 & C6 for AVDD can be calculated with the following equation:

$$C_{out(AVDD)} = \frac{V_o - V_{in(\min)}}{V_o \cdot f_s} \cdot \frac{I_{out}}{\Delta V_{out}} \quad (17)$$

ΔVout Output voltage ripple

Considering the capacitance derating under certain DC bias, two 10uF ceramic capacitors in parallel is fit for the ΔVo=20mV application.

2.7 Compensation Circuit

The COMP pin is the output of the internal trans-conductance error amplifier. The following equation can be used to calculated R2 and C4 (Figure 1).

$$R_2 = \frac{110 \cdot V_{in(\min)} \cdot V_o \cdot C_{out(AVDD)}}{L \cdot I_{out}} \quad (18)$$

$$C_4 = \frac{V_o \cdot C_{out(AVDD)}}{7.5 \cdot I_{out} \cdot R_2} \quad (19)$$

R2=39k and C4=3.3nF are used in this reference design.

2.8 Buffer Amplifier Selection

LM7321 is used as the buffer amplifier for the VCOM power. The maximum load current should be within the output current capability of the LM7321 (35mA minimum souring current and 50mA minimum sinking current for 10V supplies).

3 PCB Layout

This reference design is implemented in a 3cm×1.55cm and 2-layers PCB. All the components are placed on the top layer. Figure 2 shows the top layer and top silk screen. Figure 3 shows the layout of the bottom layer.

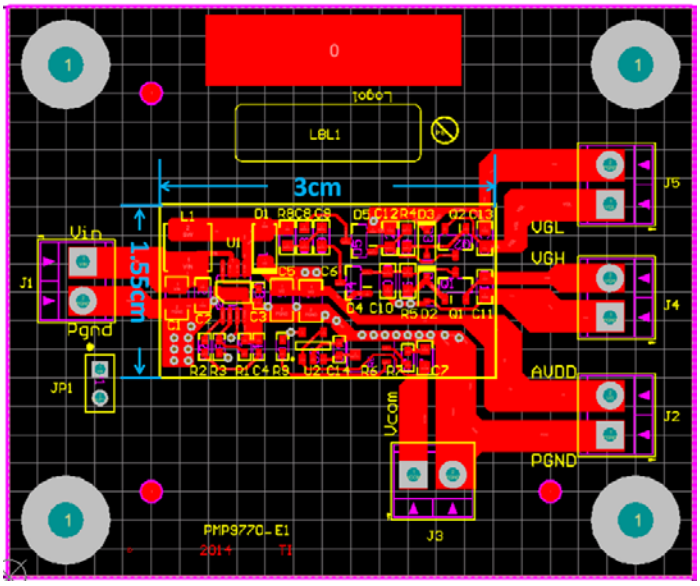

Figure 2 Top layer and Top Silkscreen

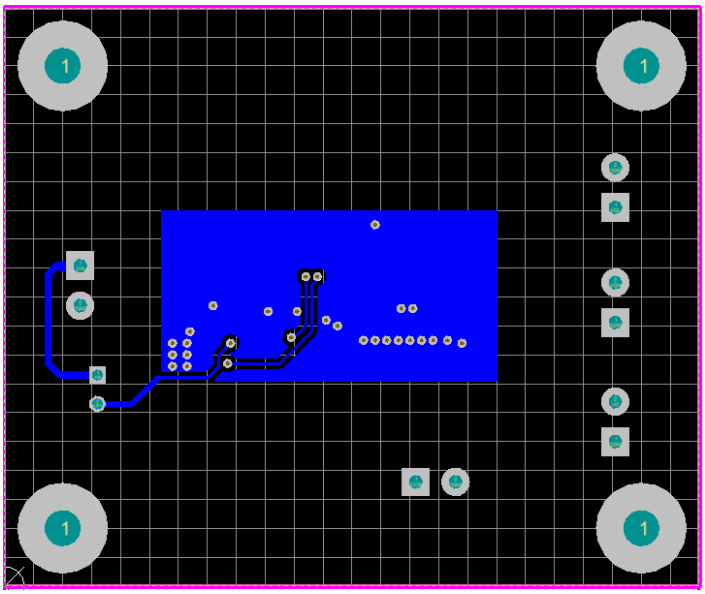

Figure 3 Bottom layer

4 Test Result

Figure 4.1 and Figure 4.2 show the SW pin voltage of the TPS61085 and the current of the inductor L1 at Vin=3.3V.

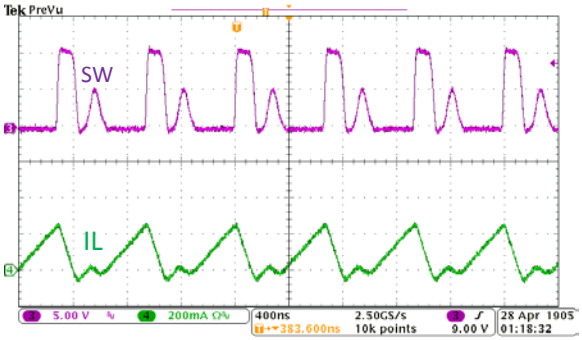

Figure 4.1 PWM switching at light load

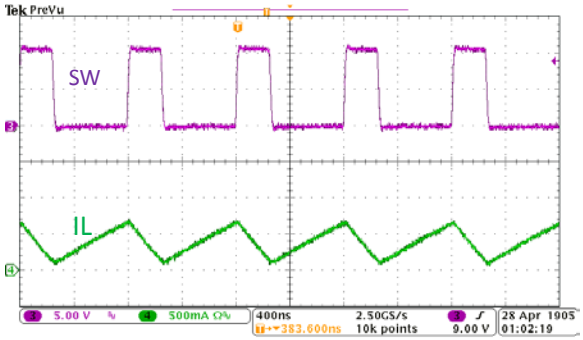

Figure 4.2 PWM switching at heavy load

Figure 5.1 shows AVDD and VCOM voltage ripple at heavy load (I_{AVDD}=100mA & I_{VCOM}=20mA). Figure 5.2 shows VGL and VGH voltage ripple with 10mA load respectively.

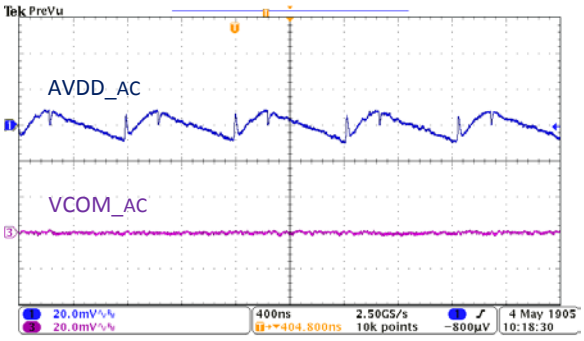

Figure 5.1 AVDD and Vcom voltage ripple

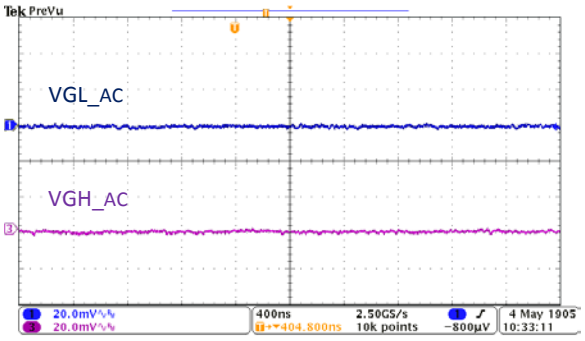

Figure 5.2 VGL and VGH voltage ripple

Figure 6.1 shows the startup waveform of AVDD, VGH voltage, and inductor current. Figure 6.2 shows the startup waveform of VGL, VCOM voltage, and inductor current. The load condition is: I_{AVDD}=100mA , I_{VCOM}=20mA, I_{VGH}=1mA, I_{VGL}=1mA.

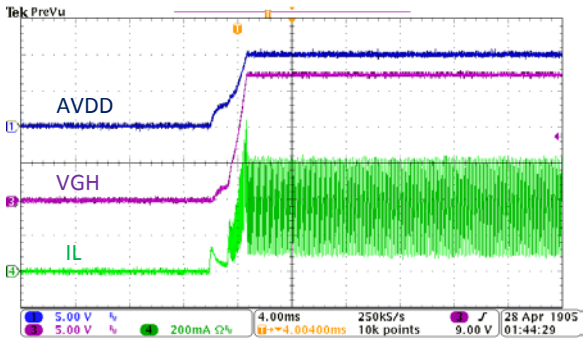

Figure 6.1 AVDD, VCOM and IL startup waveform

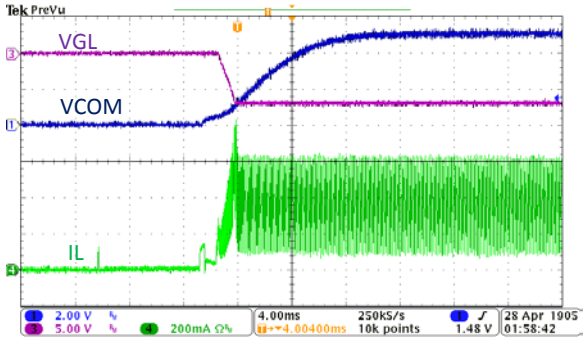

Figure 6.2 VGL, VCOM and IL startup waveform

Figure 7.1 shows the no load to full load (0mA to 100mA) transient response of AVDD. Figure 7.2 shows the no load to full load (0mA to 20mA) transient response of VCOM.

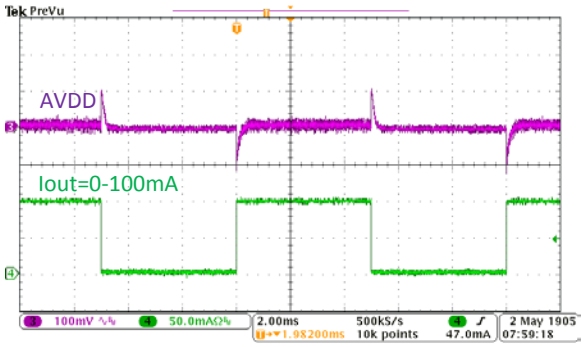

Figure 7.1 AVDD load transient response

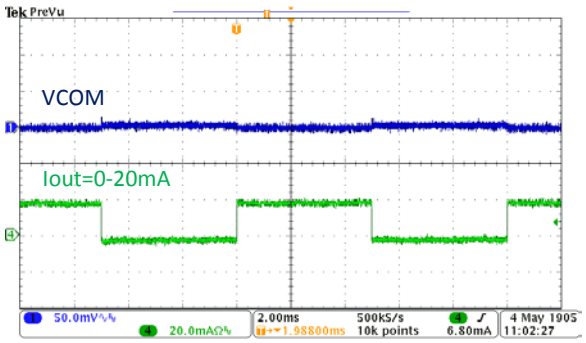

Figure 7.2 Vcom load transient response

Figure 8 shows the buffer amplifier's output voltage VCOM versus sinking & sourcing current ICOM.

Figure 9 shows AVDD voltage versus output current I_{AVDD}.

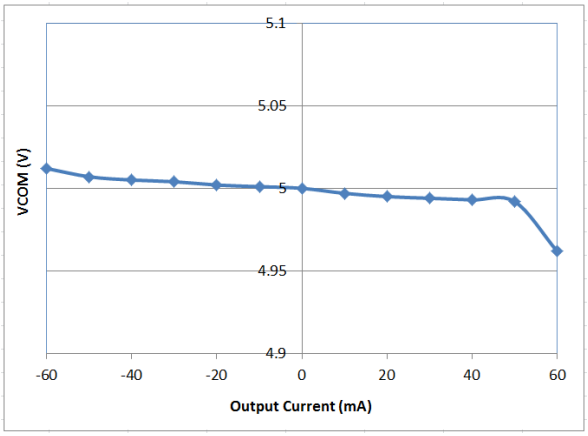

Figure 8 VCOM VS. ICOM

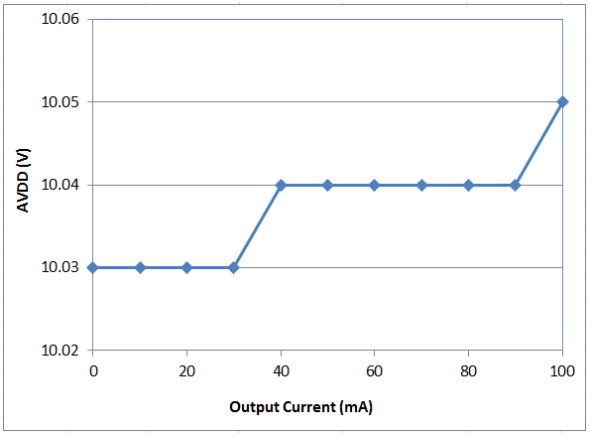

Figure 9 AVDD VS. I_{AVDD}

Figure 10 shows the VGH voltage versus output current I_{VGH}.

Figure 11 shows the VGL voltage versus output current I_{VGL}.

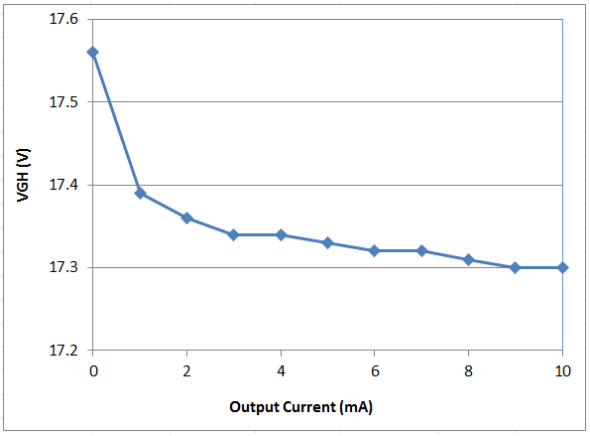

Figure 10 VGH VS. I_{GH}

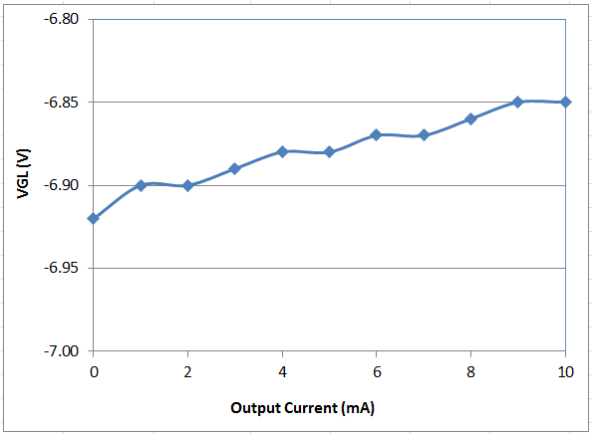

Figure 11 VGL VS. I_{GL}

Figure 12 shows the efficiency versus load current I_{AVDD} (I_{COM}=0, I_{VGH}=I_{VGL}=0) at Vin=3.3V.

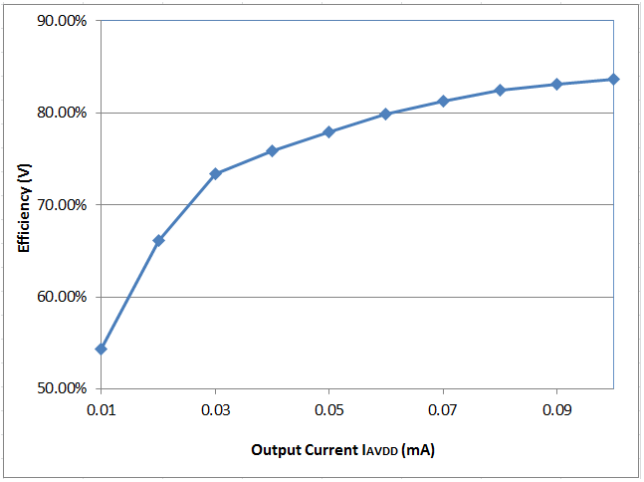

Figure 12 Efficiency VS. Load Curren

5 Further Discussion

In this reference design, the output voltage VGH is lower than twice of the AVDD voltage, the output voltage VGL is higher than -AVDD voltage, so we can get the target VGH and VGL value with the charge pump circuit shown in figure 1. If an application needs a higher VGH voltage, a positive charge pump tripler can be used to generate 3AVDD. For a lower negative VGL voltage requirement, a two-order charge pump inverter can be used to generate -2AVDD.

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