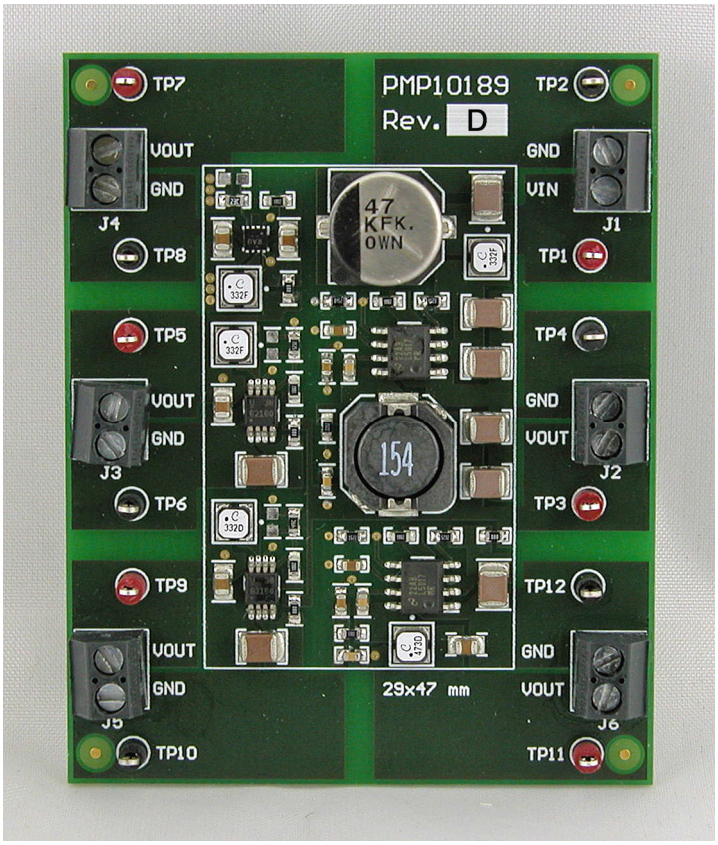
Hercules Safety MCU Power Solution

- Input 48..60V DC
- Outputs
  - LM5017 +12.0V @ 515mA
  - TPS62160 +5.0V @ 430mA
  - TLV62080 +1.2V @ 700mA
  - TPS62160 +3.3V @ 620mA
  - LM5017 +3.3V @ 230mA



1 LM5017 - +12.0V @ 515mA

1.1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 54.0V with no load on the 12.0V output.

Channel C1: **54.0V Input voltage**
10V/div, 5ms/div

Channel C2: **12.0V Output voltage**
2V/div, 5ms/div

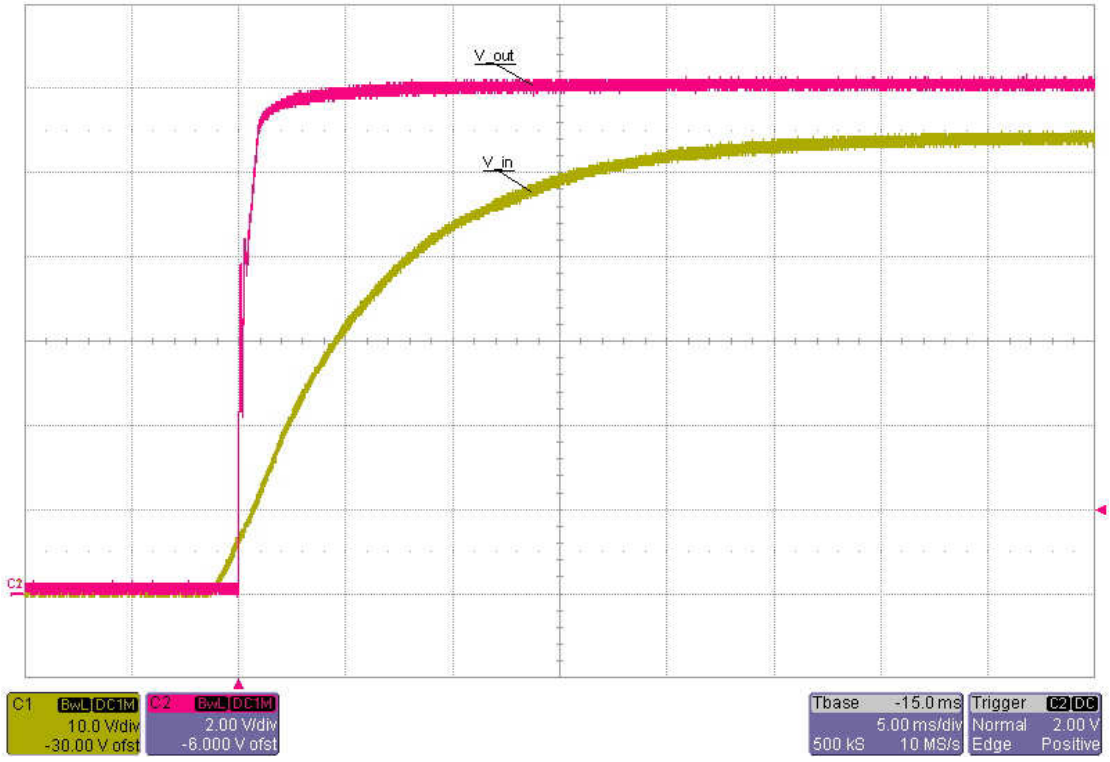


Figure 1

1.2 Shutdown

The shutdown is shown in Figure 2. The input voltage is set at 54.0V with 515mA load on the output.

Channel C1: **54.0V Input voltage**
10V/div, 20ms/div

Channel C2: **12.0V Output voltage**
2V/div, 20ms/div

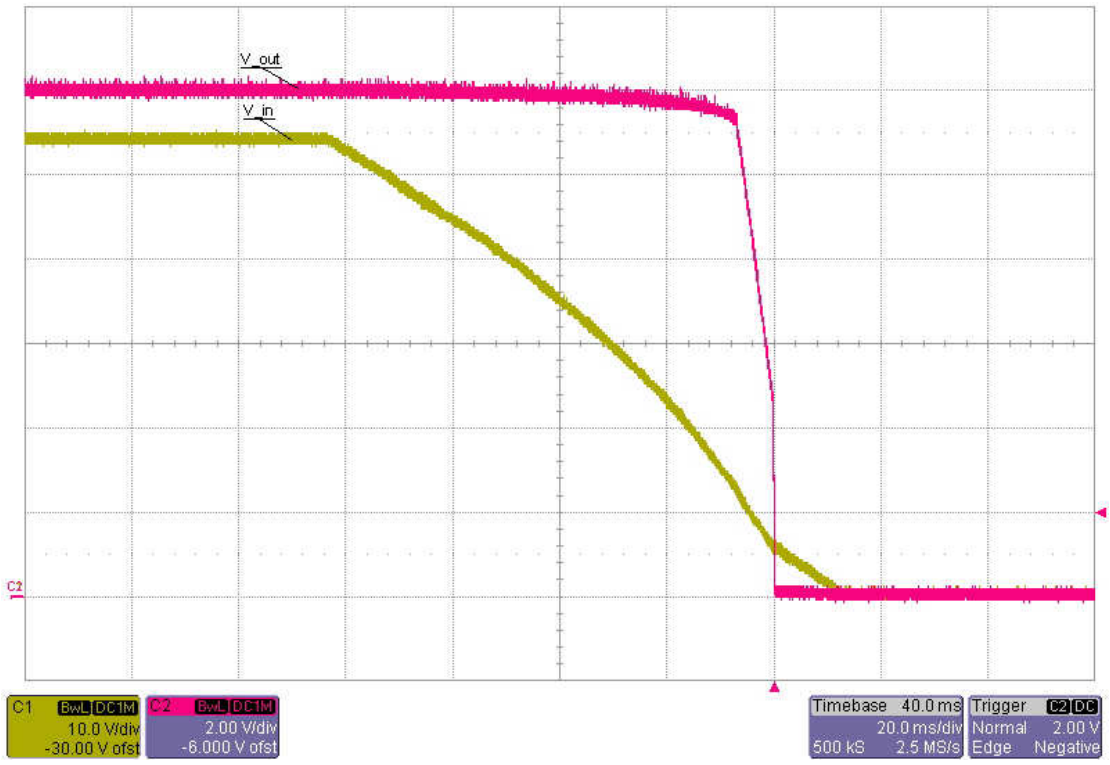


Figure 2

1.3 Switching Node

The drain-source voltage on the switching node is shown in Figure 3. The image is captured with 54V input voltage and 515mA load on the 12.0V output.

Channel C2: **Drain-source voltage**, -2.6V minimum voltage, 55.0V maximum voltage 10V/div, 2us/div

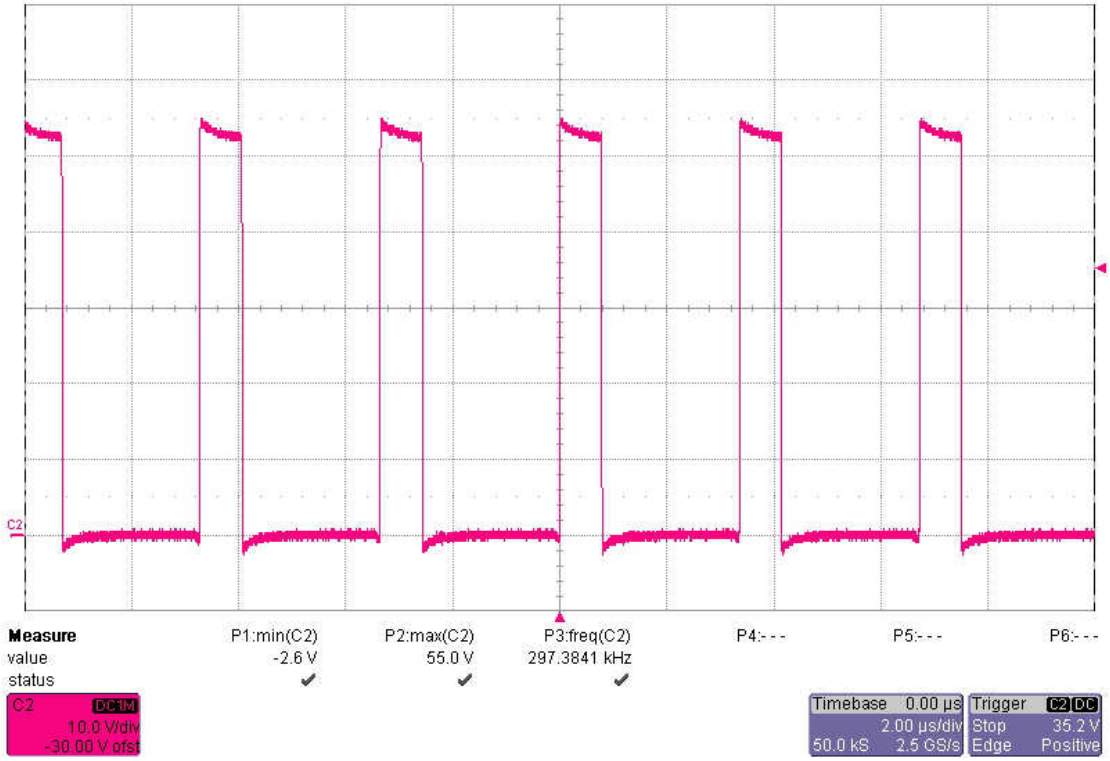


Figure 3

1.4 Output Ripple

The output ripple voltage is shown in Figure 4. The input voltage is set at 54.0V with 515mA load on the output.

Channel C2: **Output voltage @ 54.0V input**, 22mV peak-peak (0.2%)
20mV/div, 5us/div, AC coupled

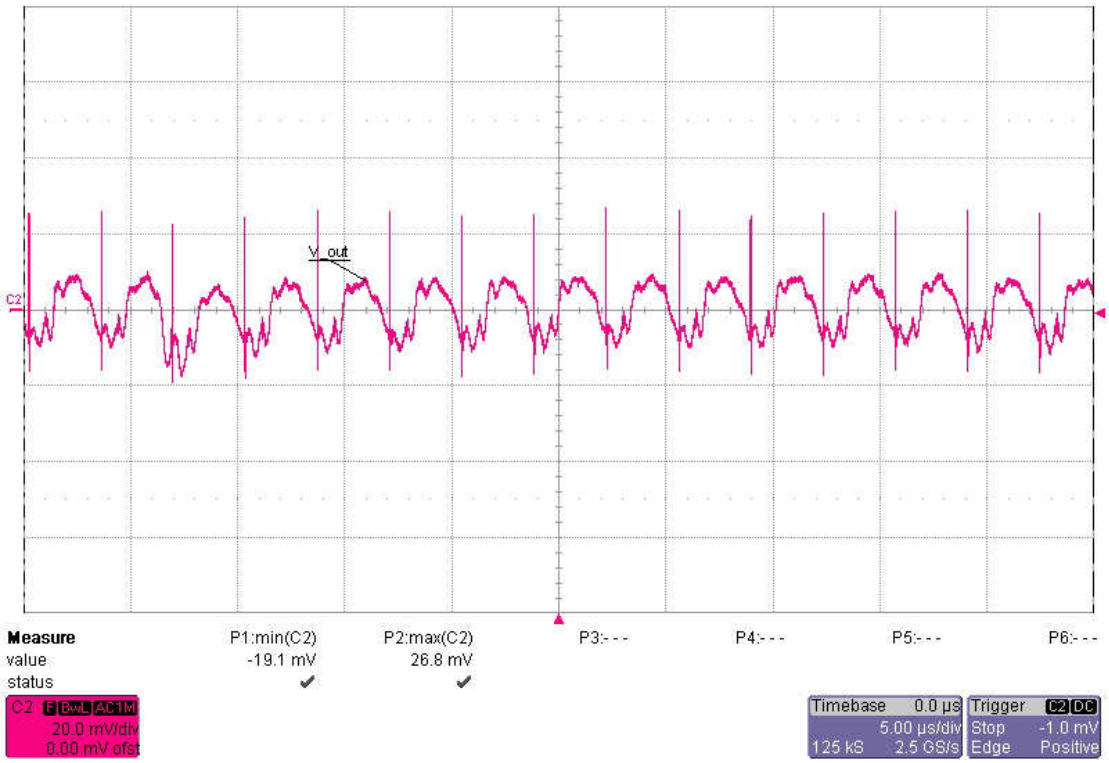


Figure 4

1.5 Efficiency & Load Regulation

The efficiency and load regulation are shown in Figure 5 and Figure 6.

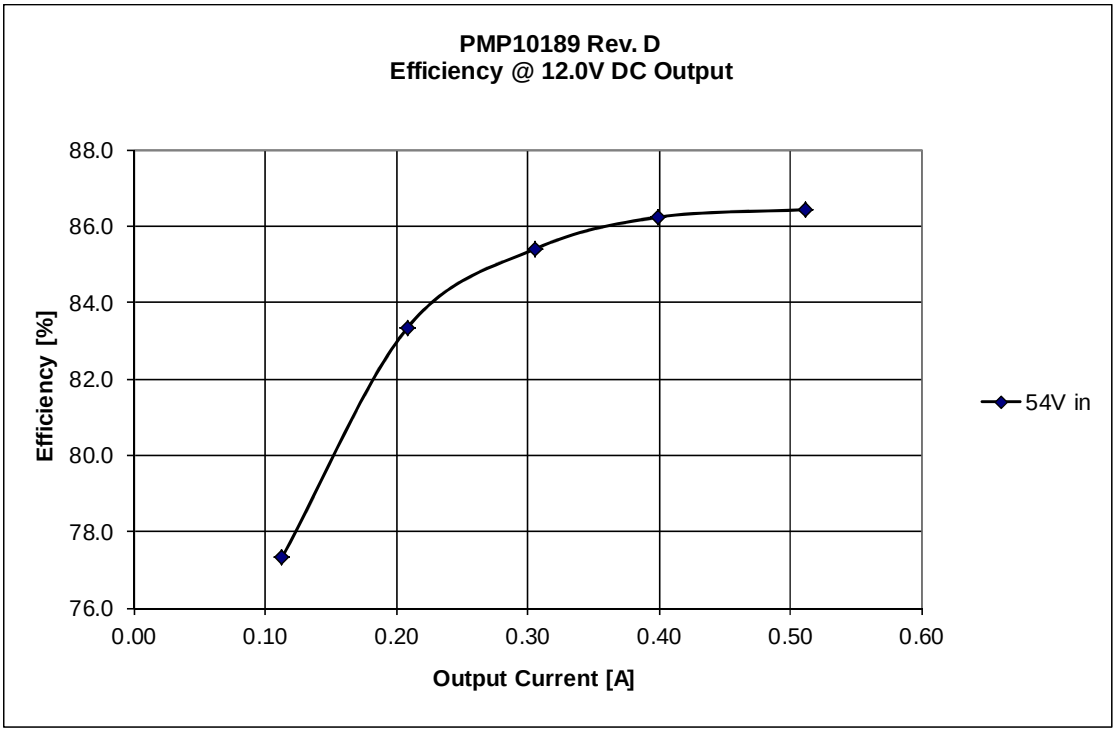


Figure 5

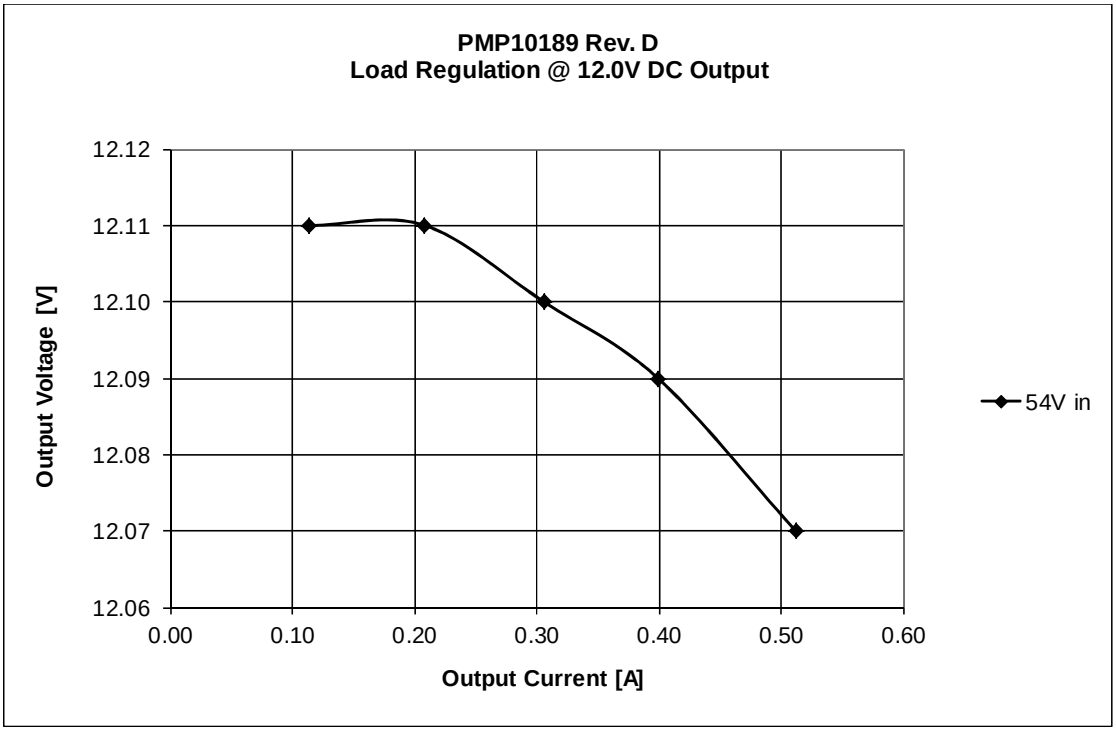


Figure 6

2 LM5017 - +3.3V @ 230mA

2.1 Startup

The startup waveform is shown in Figure 7. The input voltage is set at 12.0V with no load on the 3.3V output.

Channel C1: **12.0V Input voltage**
2V/div, 5ms/div

Channel C2: **3.3V Output voltage**
1V/div, 5ms/div

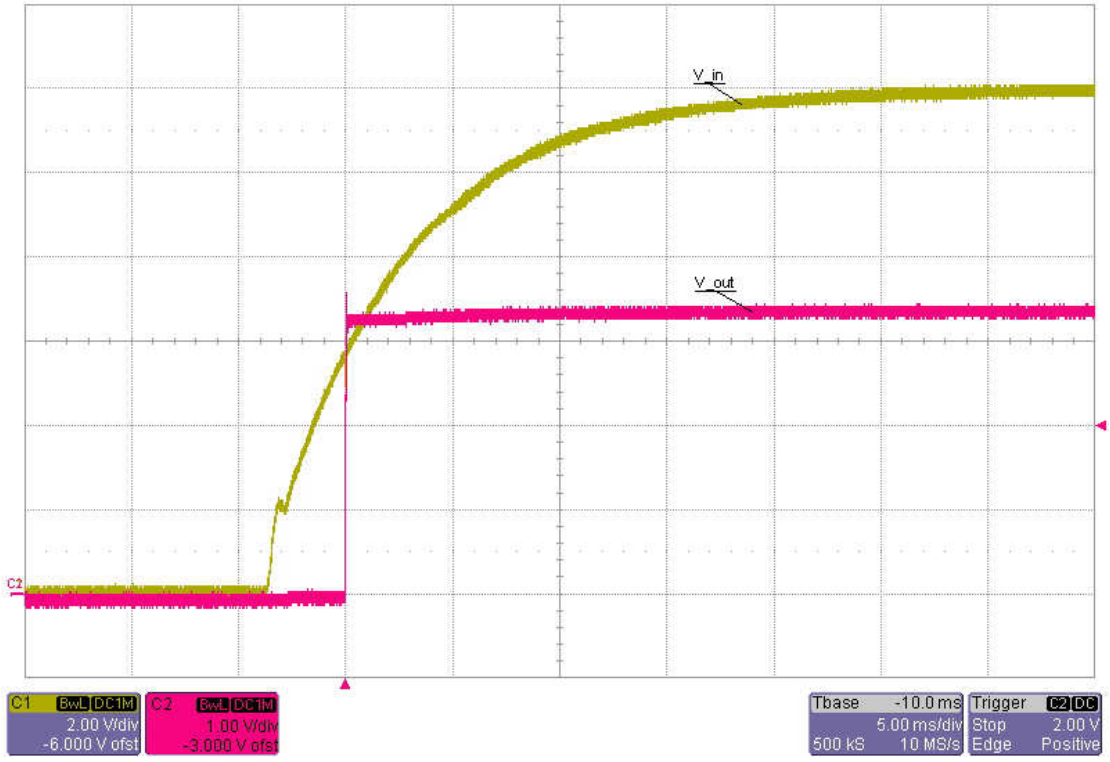


Figure 7

2.2 Shutdown

The shutdown is shown in Figure 8. The input voltage is set at 12.0V with 230mA load on the output.

Channel C1: **12.0V Input voltage**
2V/div, 5ms/div

Channel C2: **3.3V Output voltage**
1V/div, 5ms/div

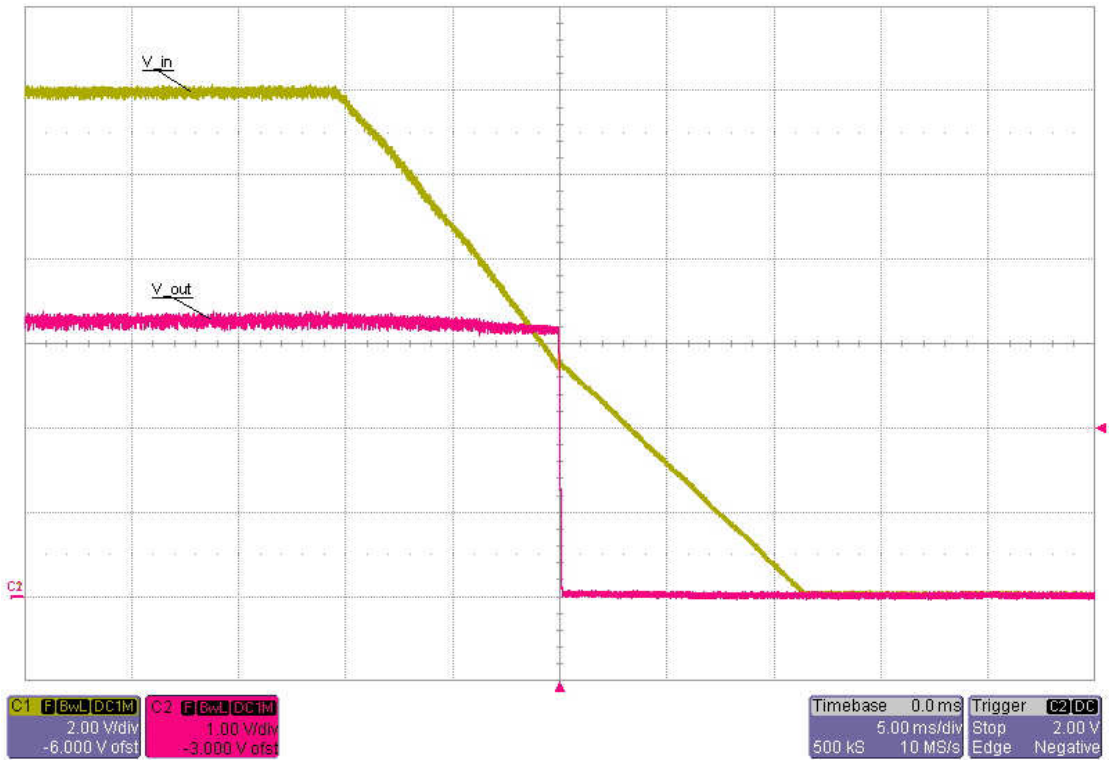


Figure 8

2.3 Switching Node

The drain-source voltage on the switching node is shown in Figure 9. The image is captured with 12V input voltage and 230mA load on the 3.3V output.

Channel C2: **Drain-source voltage**, -1.3V minimum voltage, 14.0V maximum voltage 5V/div, 1us/div

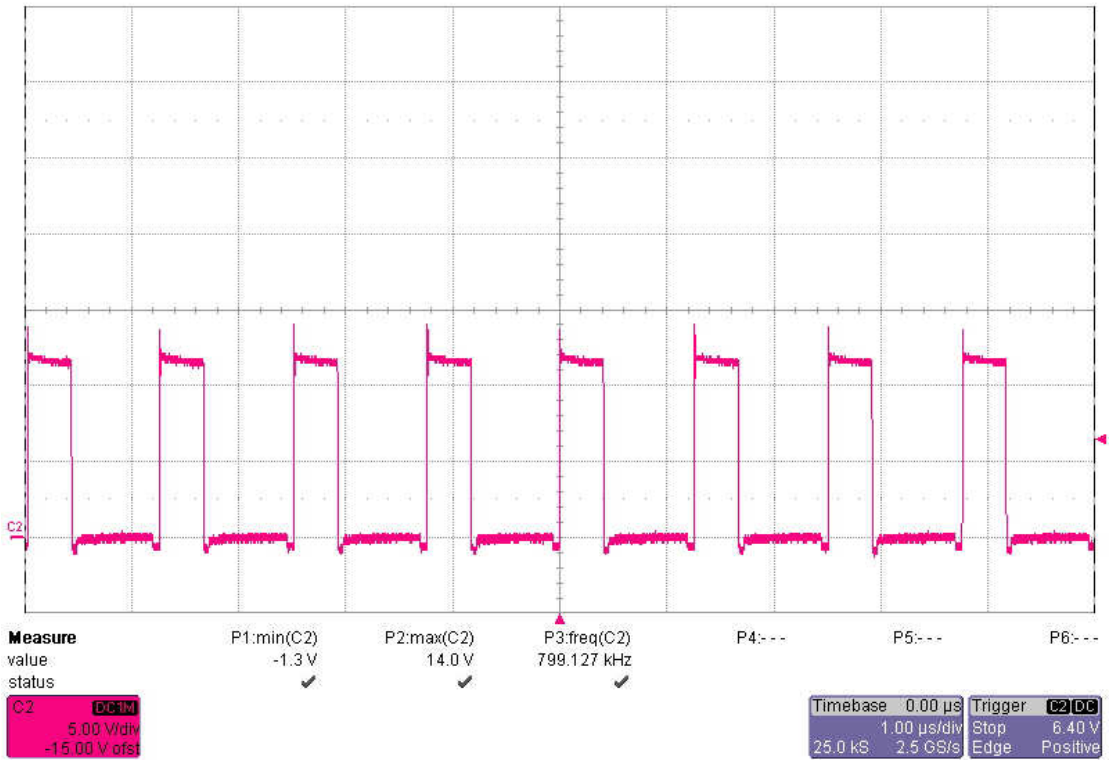


Figure 9

2.4 Output Ripple

The output ripple voltage is shown in Figure 10. The input voltage is set at 12.0V with 230mA load on the output.

Channel C2: **Output voltage @ 12.0V input**, 6mV peak-peak (0.2%)
20mV/div, 2us/div, AC coupled

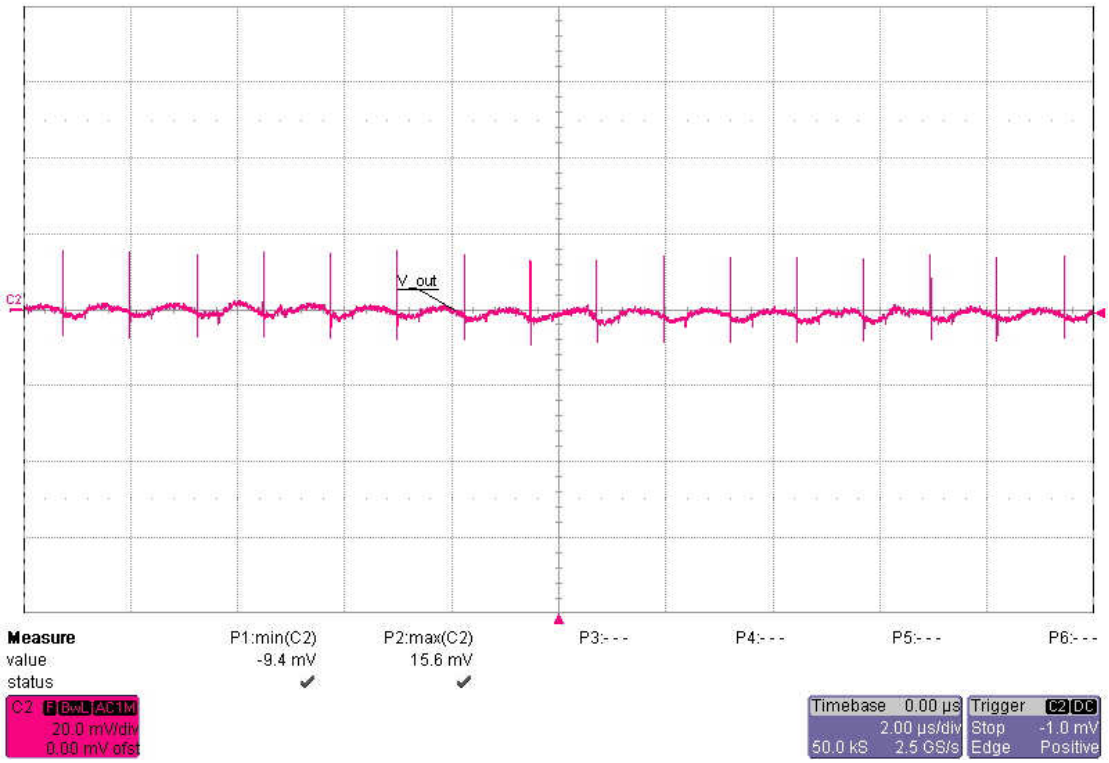


Figure 10

2.5 Efficiency & Load Regulation

The efficiency and load regulation are shown in Figure 11 and Figure 12.

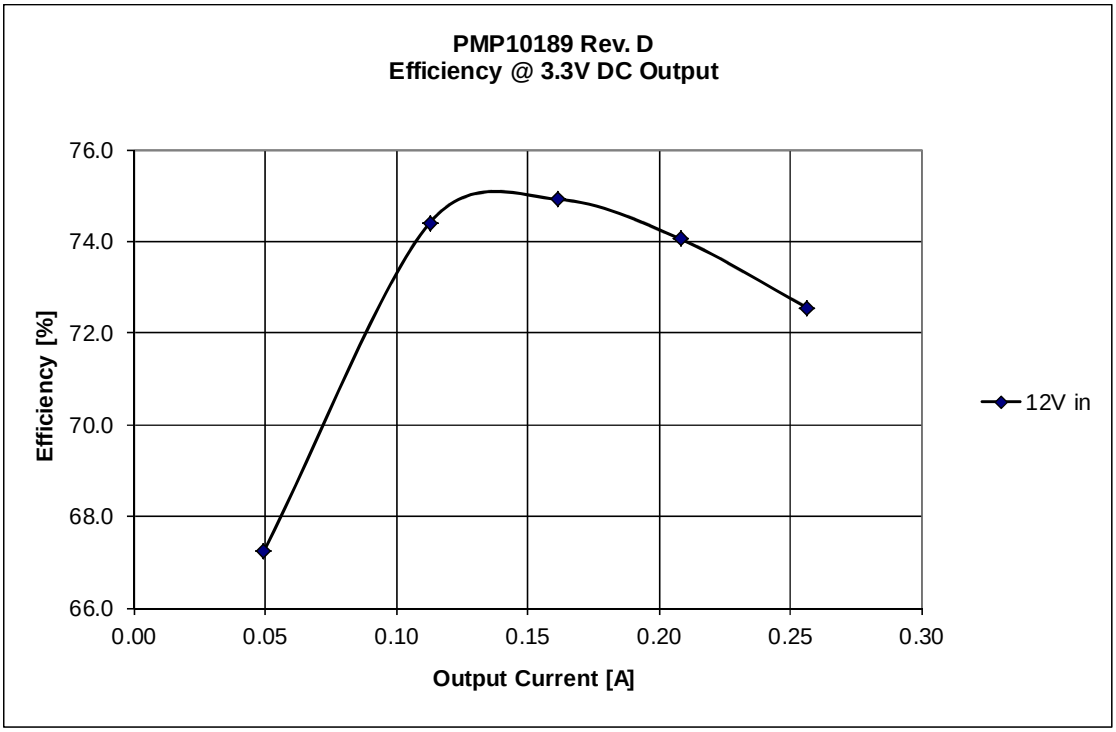


Figure 11

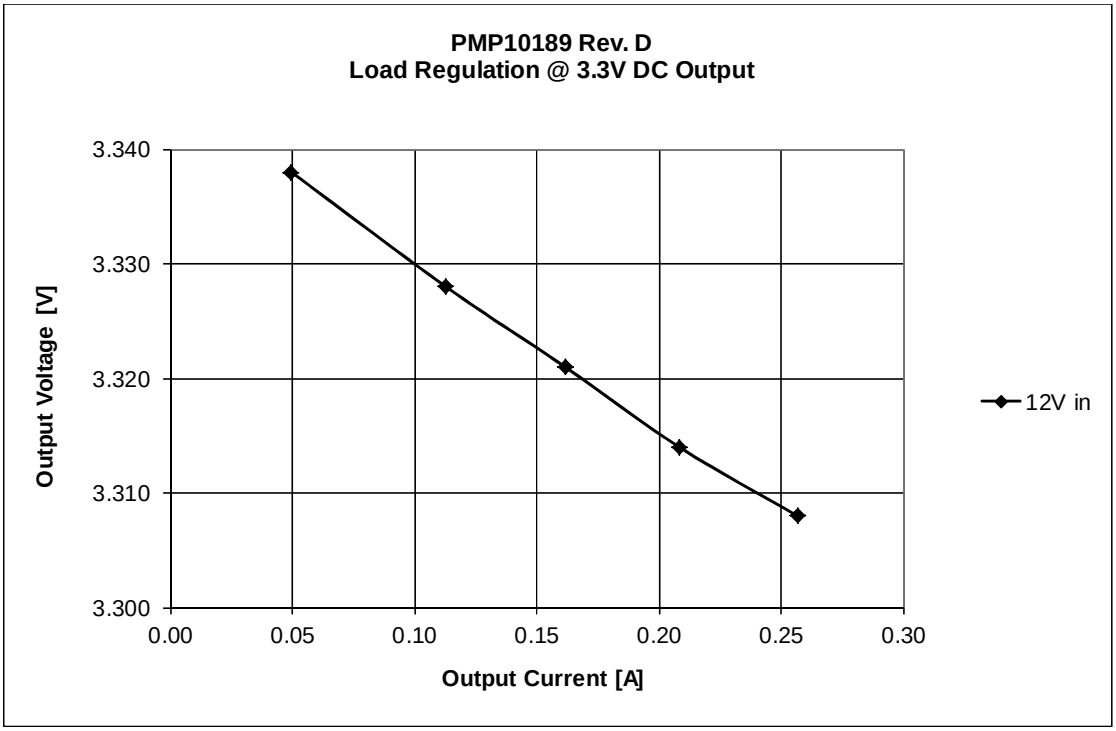


Figure 12

3 TPS62160 - +5.0V @ 430mA

3.1 Startup

The startup waveform is shown in Figure 13. The input voltage is set at 12.0V with no load on the 5.0V output.

Channel C1: **12.0V Input voltage**
2V/div, 5ms/div

Channel C2: **5.0V Output voltage**
2V/div, 5ms/div

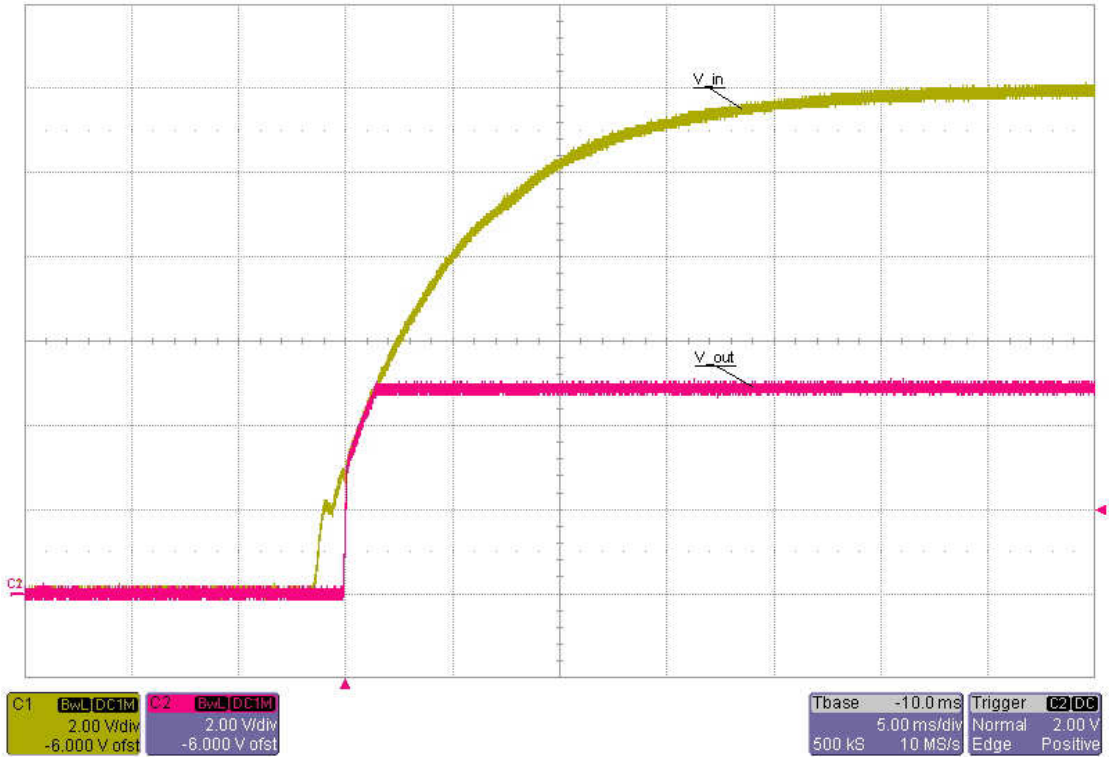


Figure 13

3.2 Shutdown

The shutdown is shown in Figure 14. The input voltage is set at 12.0V with 430mA load on the output.

Channel C1: **12.0V Input voltage**
2V/div, 5ms/div

Channel C2: **5.0V Output voltage**
2V/div, 5ms/div

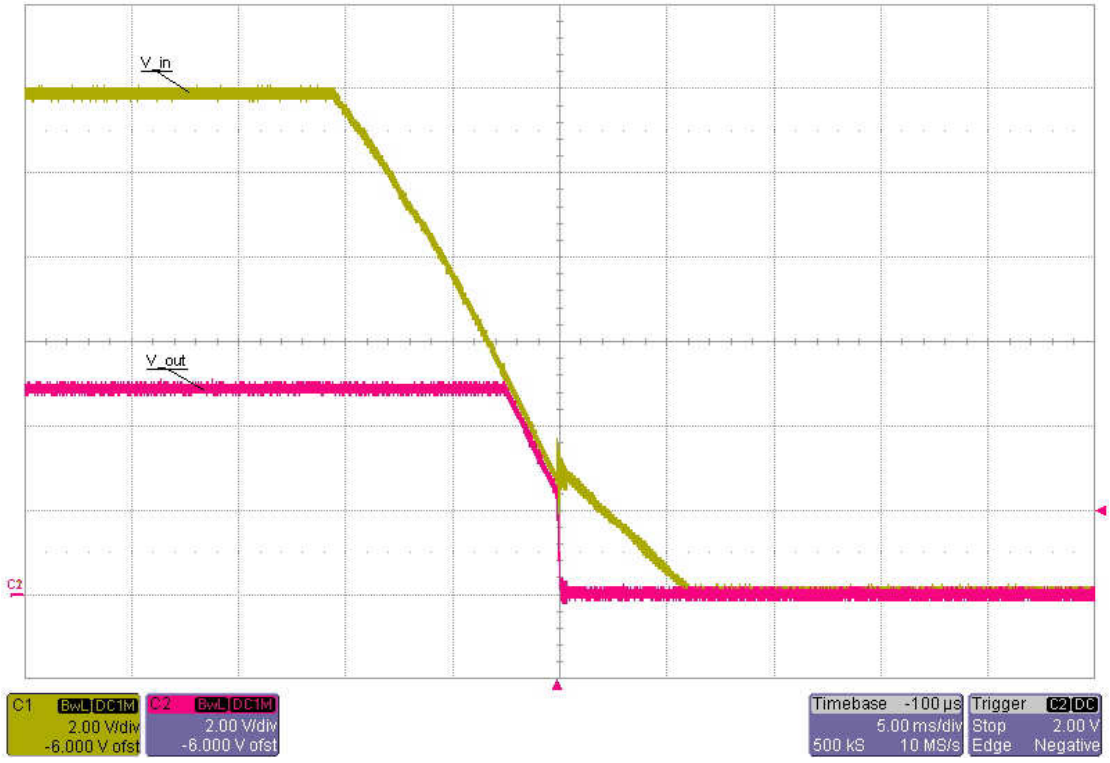


Figure 14

3.3 Switching Node

The drain-source voltage on the switching node is shown in Figure 15. The image is captured with 12V input voltage and 430mA load on the 5.0V output.

Channel C2: **Drain-source voltage**, -1.0V minimum voltage, 13.0V maximum voltage 2V/div, 500ns/div

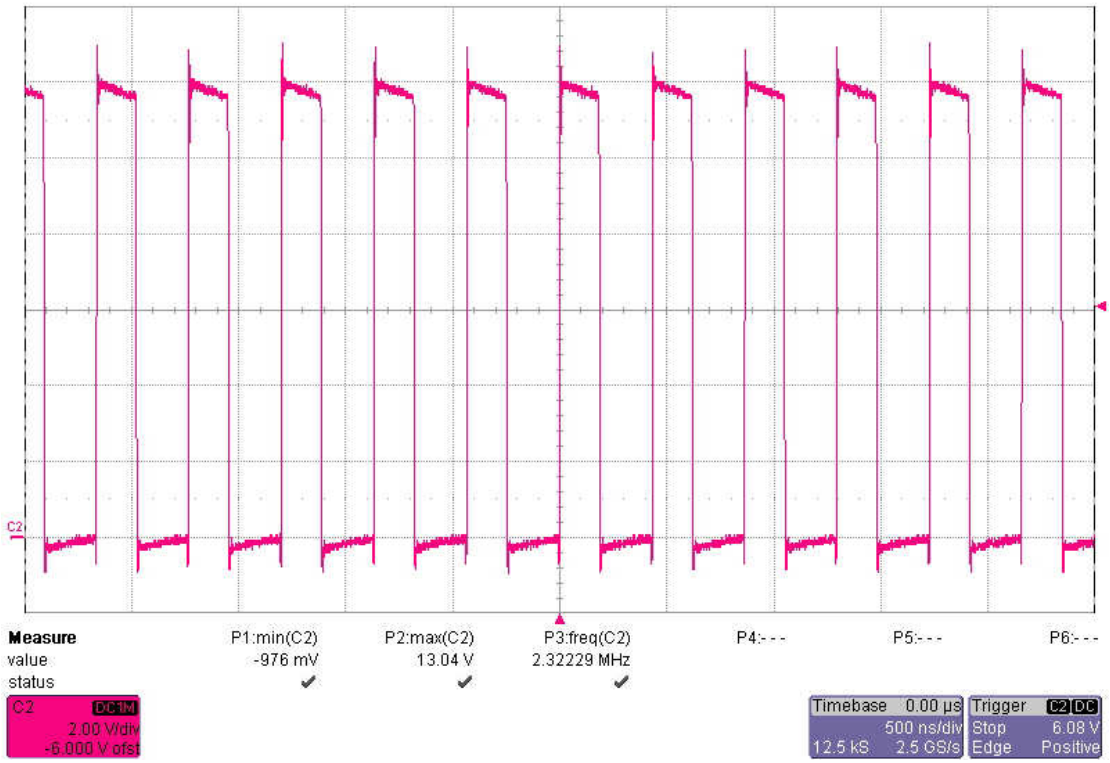


Figure 15

3.4 Output Ripple

The output ripple voltage is shown in Figure 16. The input voltage is set at 12.0V with 430mA load on the output.

Channel C2: **Output voltage @ 12.0V input**, 8mV peak-peak (0.2%)
20mV/div, 1us/div, AC coupled

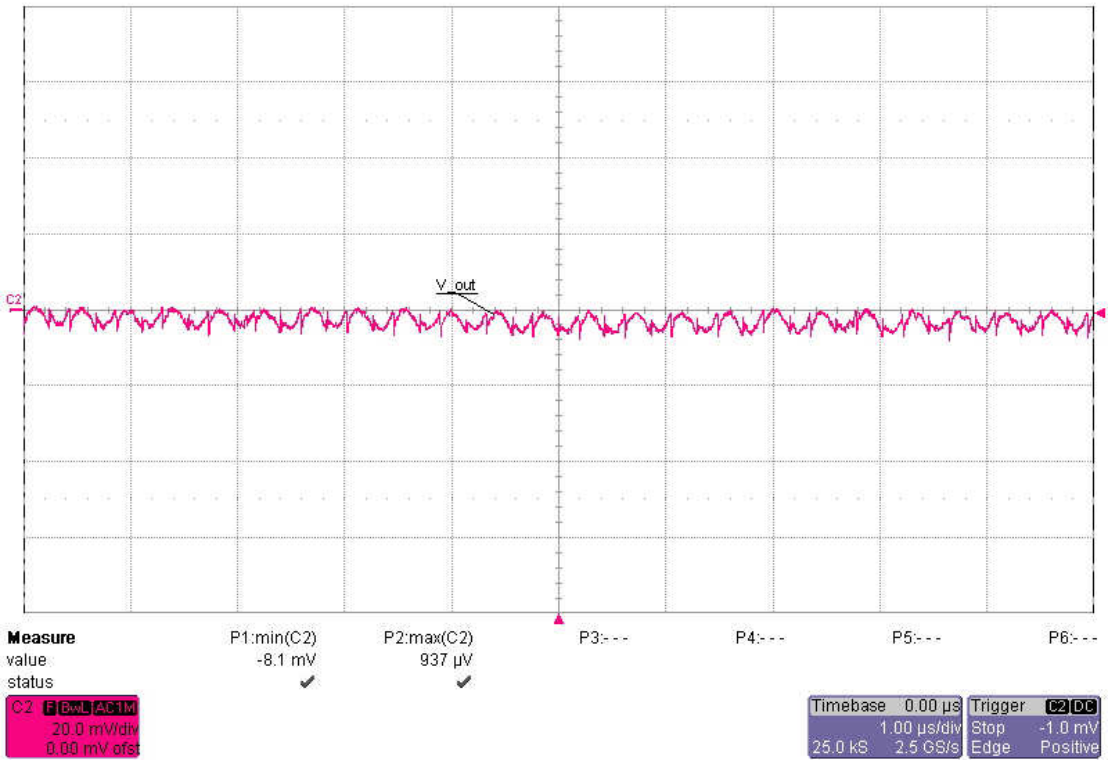


Figure 16

3.5 Efficiency & Load Regulation

The efficiency and load regulation are shown in Figure 17 and Figure 18.

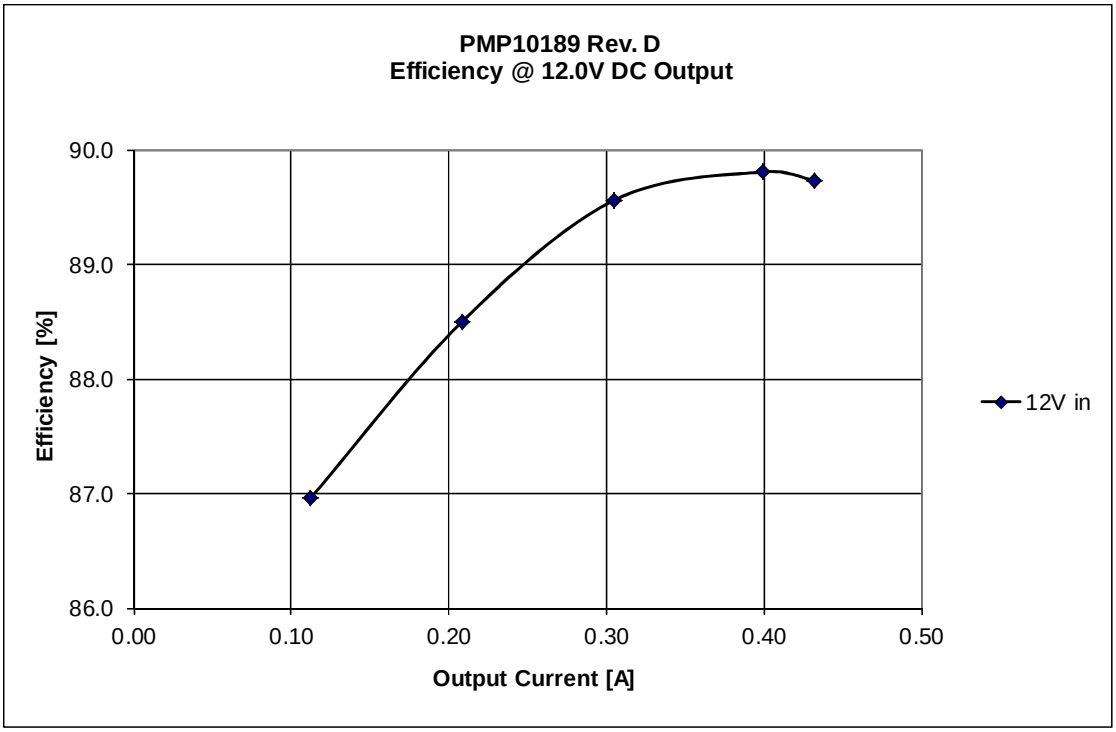


Figure 17

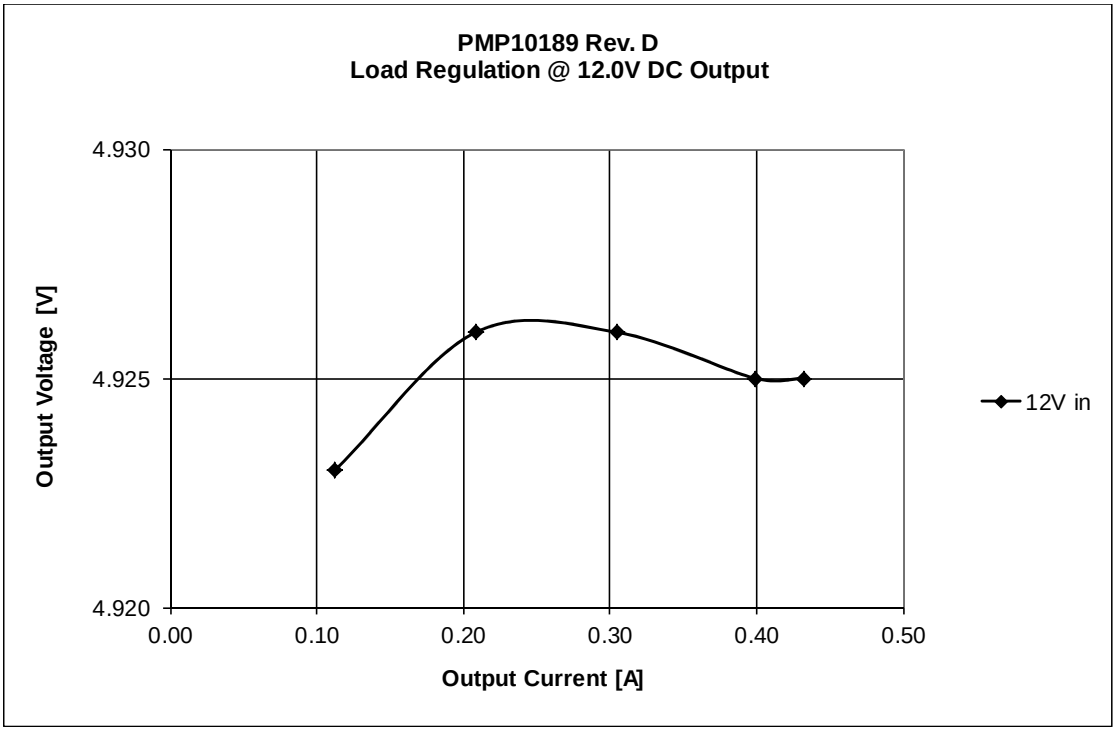


Figure 18

3.6 Frequency Response

Figure 19 shows the loop response at 12.0V input voltage and 430mA load.

12V input

- 430mA load 80 deg phase margin, 17.1 kHz bandwidth, -25 dB gain margin

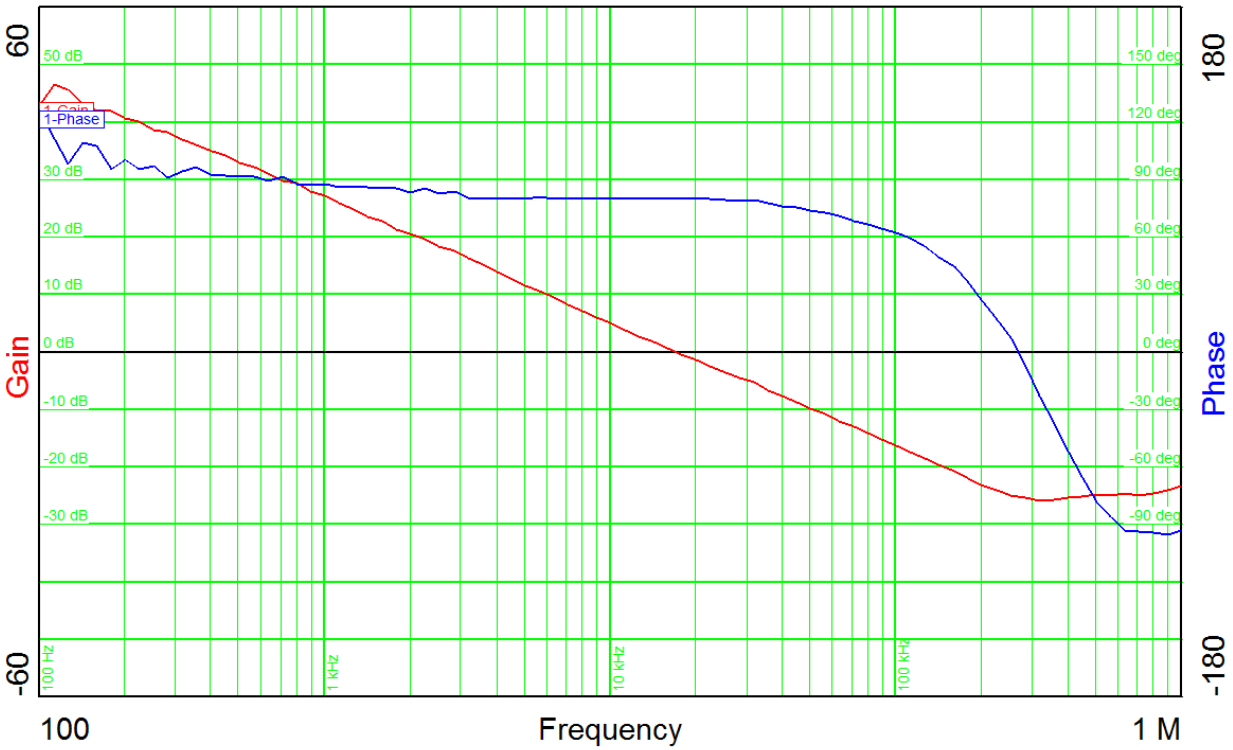


Figure 19

4 TLV62080 - +1.2V @ 700mA

4.1 Startup

The startup waveform is shown in Figure 20. The input voltage is set at 5.0V with no load on the 1.2V output.

Channel C1: **5.0V Input voltage**
2V/div, 5ms/div

Channel C2: **1.2V Output voltage**
2V/div, 5ms/div

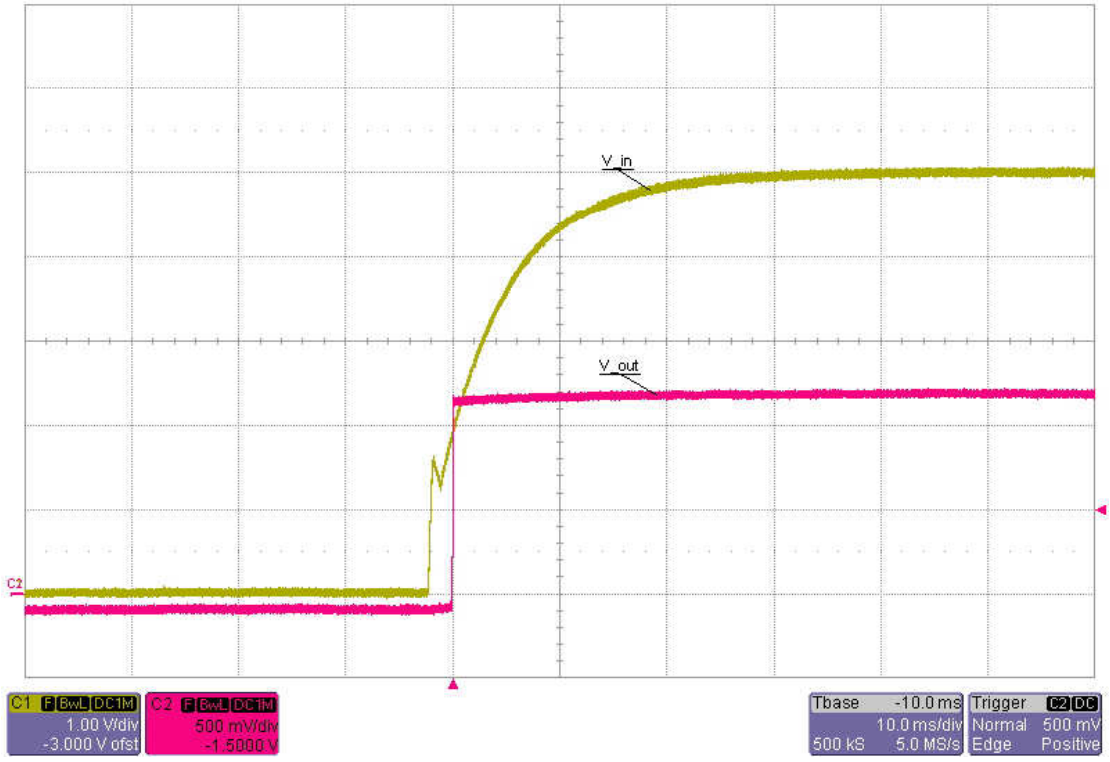


Figure 20

4.2 Shutdown

The shutdown is shown in Figure 21. The input voltage is set at 5.0V with 700mA load on the output.

Channel C1: **5.0V Input voltage**
1V/div, 2ms/div

Channel C2: **1.2V Output voltage**
500mV/div, 2ms/div

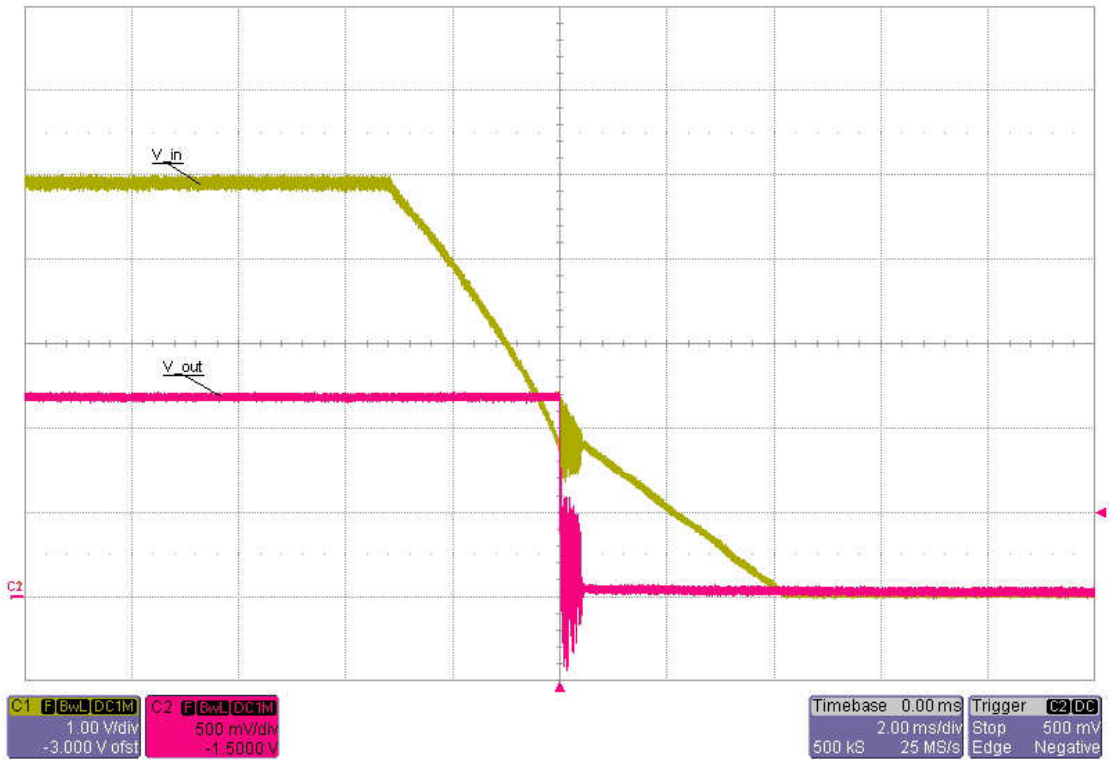


Figure 21

4.3 Switching Node

The drain-source voltage on the switching node is shown in Figure 22. The image is captured with 5V input voltage and 700mA load on the 1.2V output.

Channel C2: **Drain-source voltage**, -1.0V minimum voltage, 5.0V maximum voltage 1V/div, 500ns/div

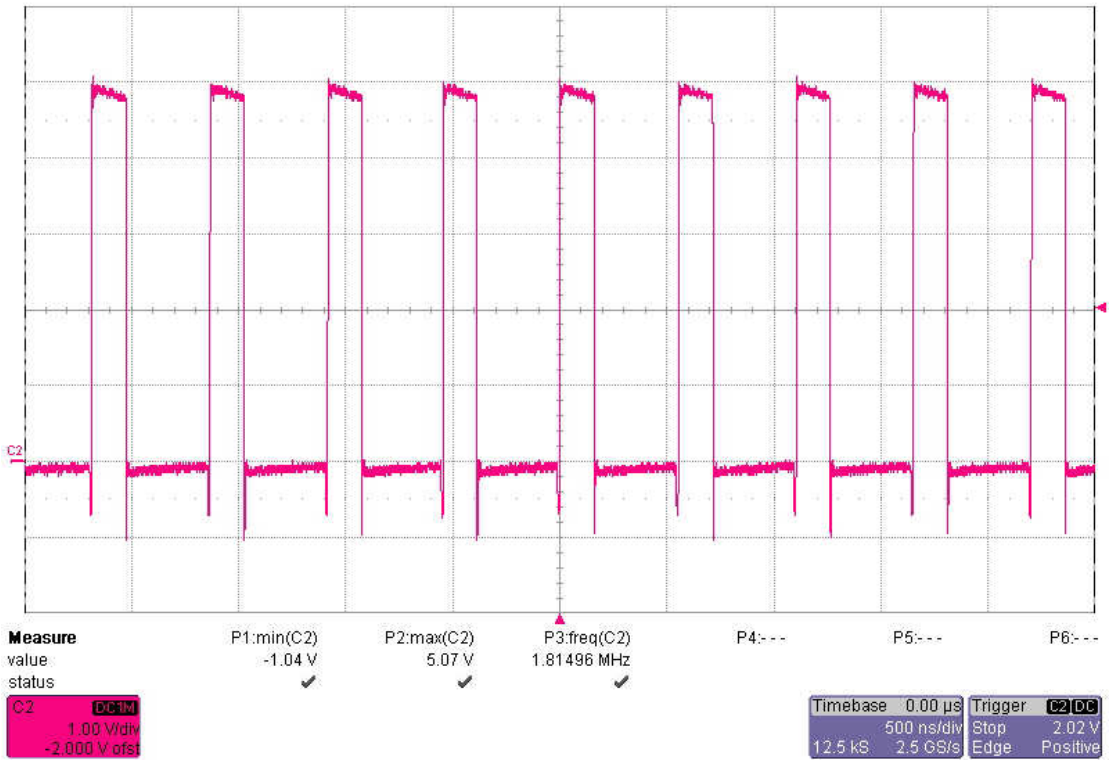


Figure 22

4.4 Output Ripple

The output ripple voltage is shown in Figure 23. The input voltage is set at 5.0V with 700mA load on the output.

Channel C2: **Output voltage @ 5.0V input**, 2mV peak-peak (0.2%)
20mV/div, 1us/div, AC coupled

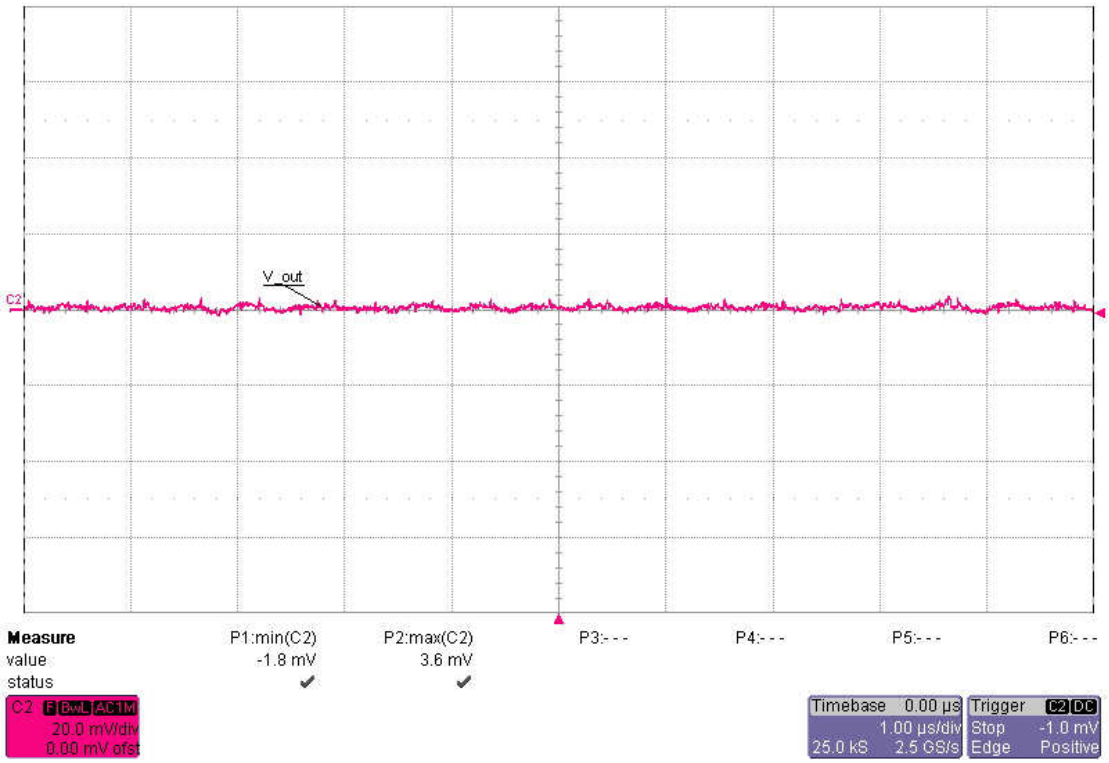


Figure 23

4.5 Efficiency & Load Regulation

The efficiency and load regulation are shown in Figure 24 and Figure 25.

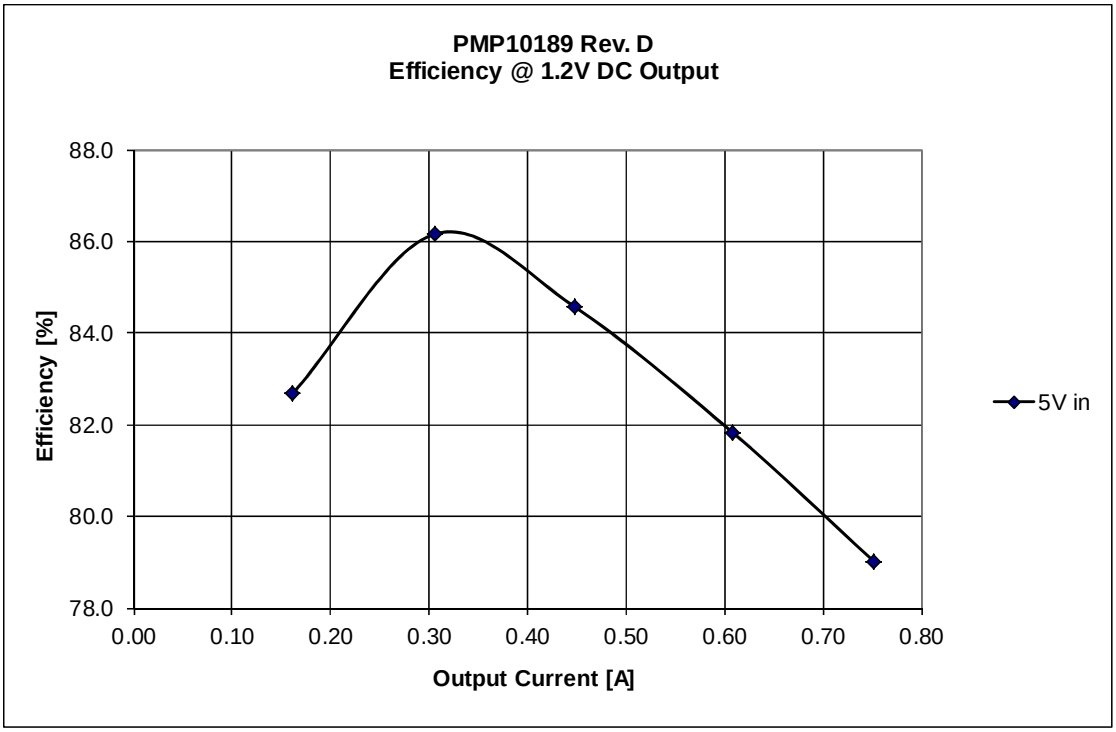


Figure 24

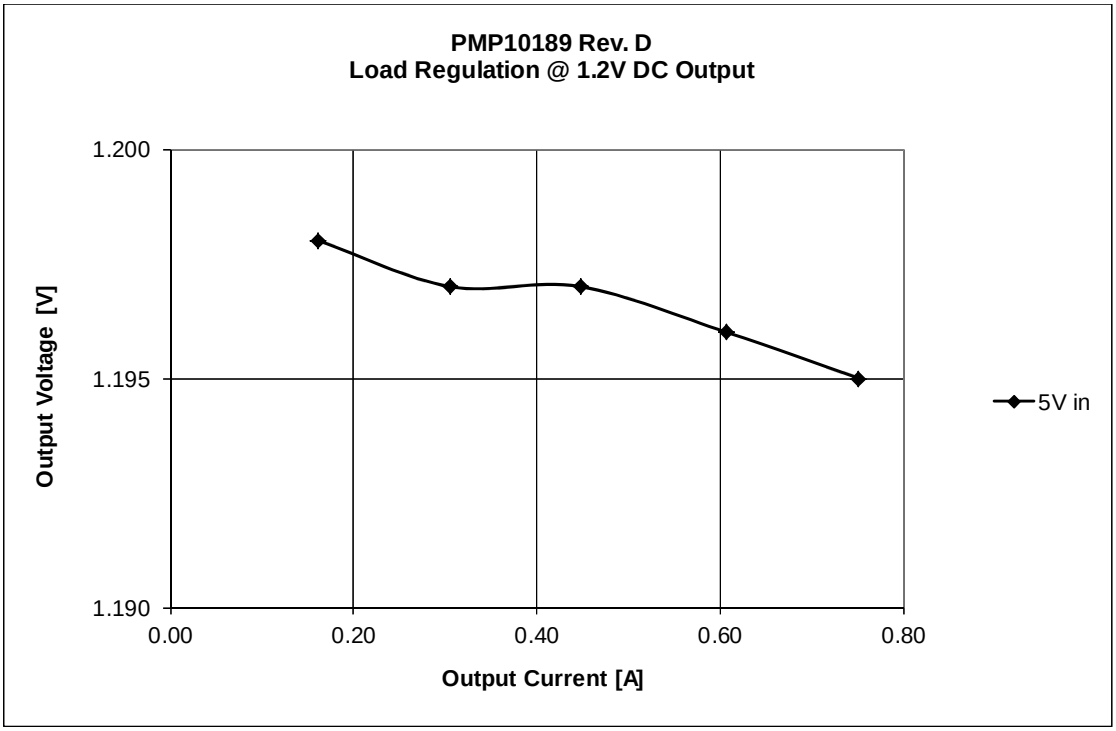


Figure 25

4.6 Frequency Response

Figure 26 shows the loop response at 5.0V input voltage and 700mA load.

5V input

- 700mA load 77 deg phase margin, 28.5 kHz bandwidth, -26 dB gain margin

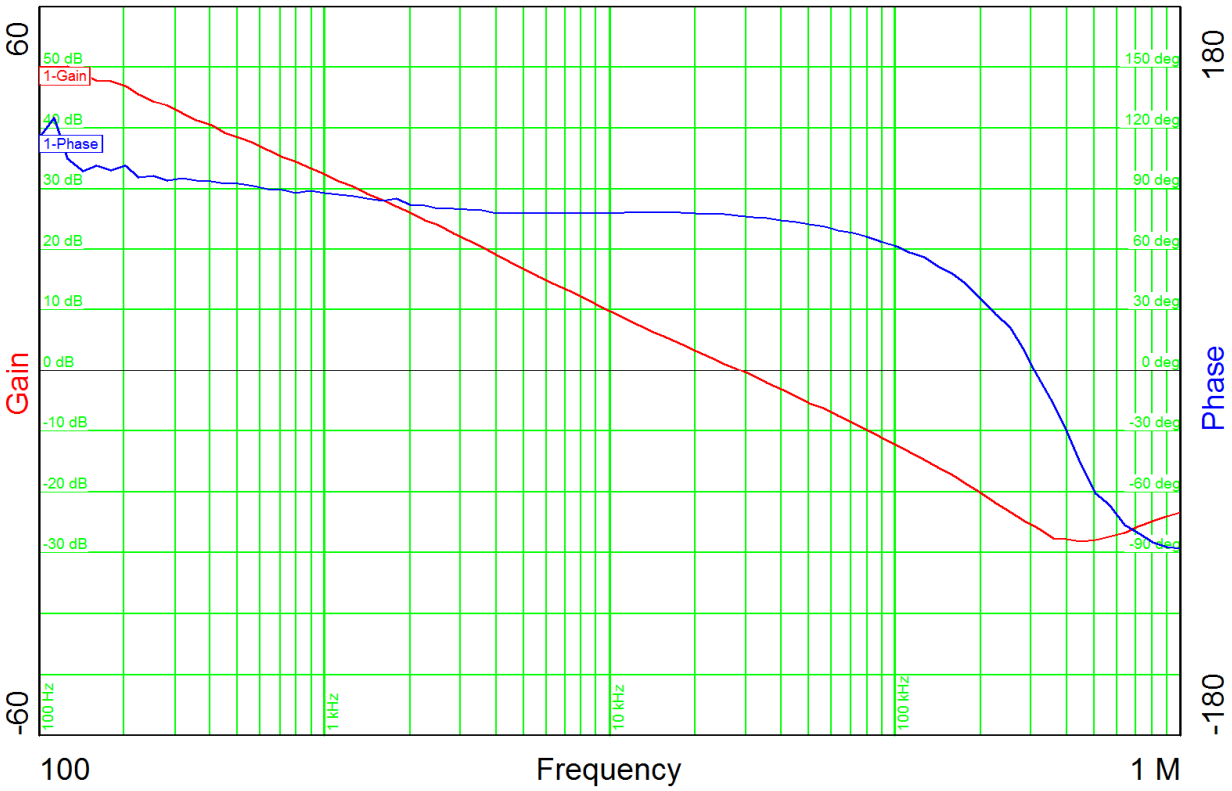


Figure 26

5 TPS62160 - +3.3V @ 620mA

5.1 Startup

The startup waveform is shown in Figure 27. The input voltage is set at 12.0V with no load on the 3.3V output.

Channel C1: **12.0V Input voltage**
2V/div, 5ms/div

Channel C2: **3.3V Output voltage**
1V/div, 5ms/div

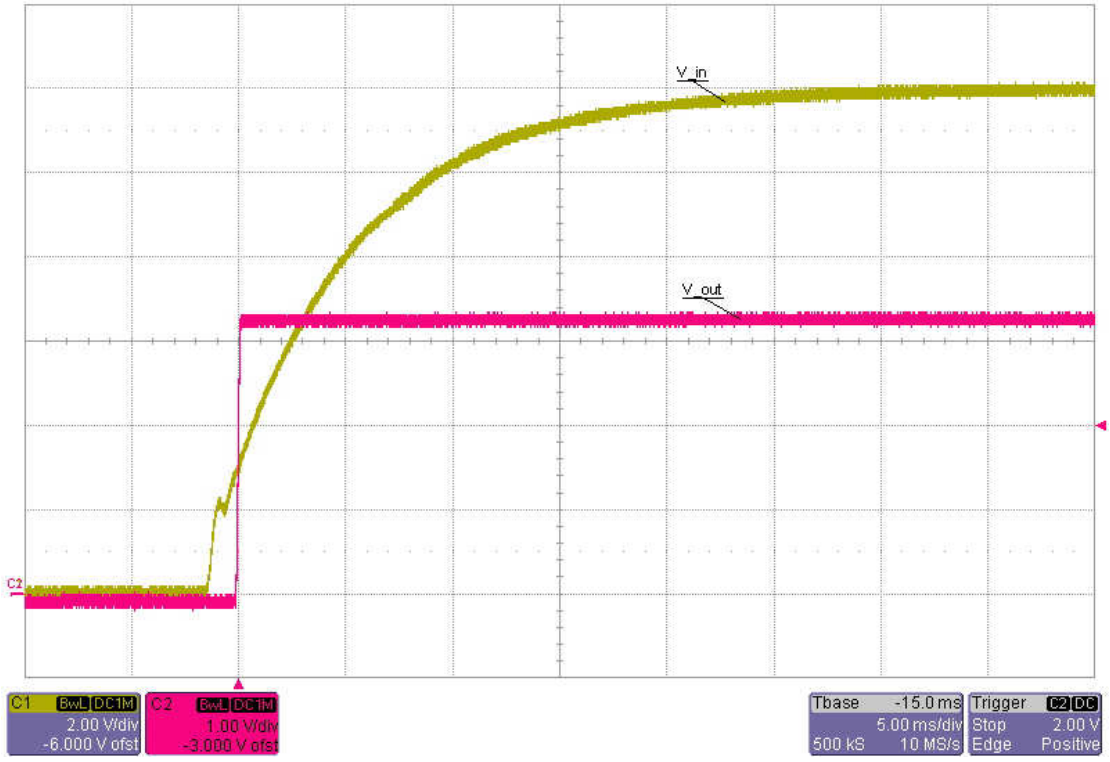


Figure 27

5.2 Shutdown

The shutdown is shown in Figure 28. The input voltage is set at 12.0V with 620mA load on the output.

Channel C1: **12.0V Input voltage**
2V/div, 2ms/div

Channel C2: **3.3V Output voltage**
1V/div, 2ms/div

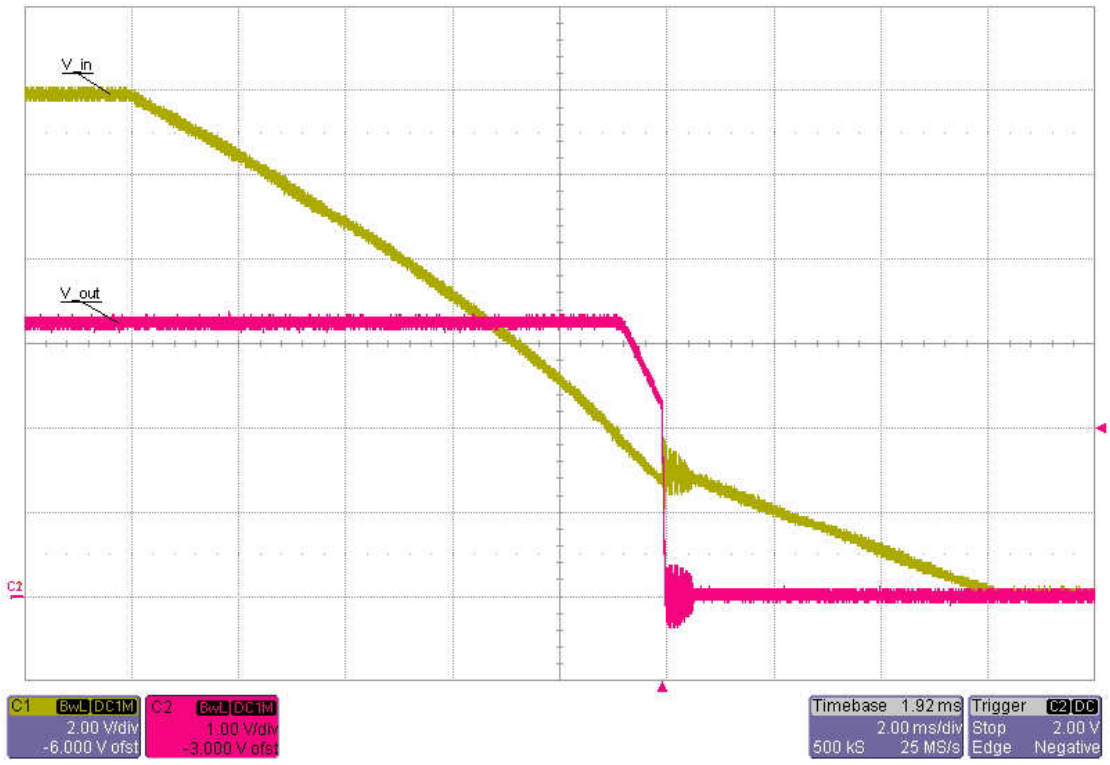


Figure 28

5.3 Switching Node

The drain-source voltage on the switching node is shown in Figure 29. The image is captured with 12V input voltage and 620mA load on the 3.3V output.

Channel C2: **Drain-source voltage**, -1.0V minimum voltage, 13.2V maximum voltage 2V/div, 500ns/div

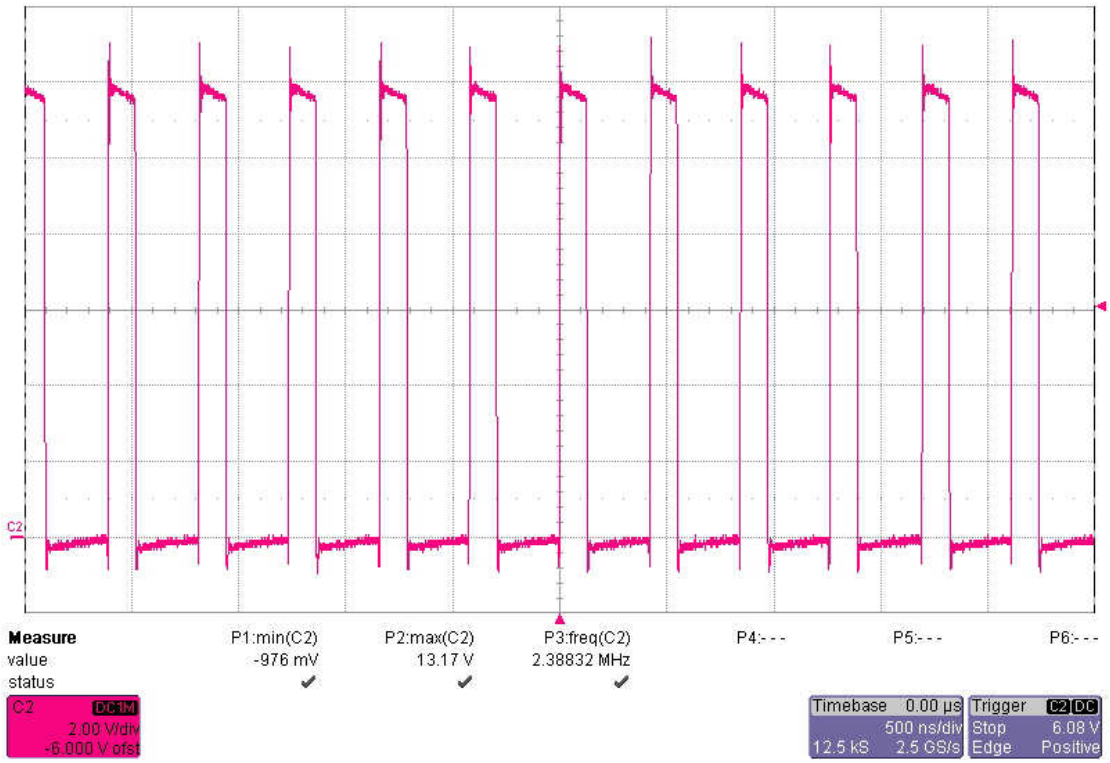


Figure 29

5.4 Output Ripple

The output ripple voltage is shown in Figure 30. The input voltage is set at 12.0V with 620mA load on the output.

Channel C2: **Output voltage @ 12.0V input**, 10mV peak-peak (0.3%)
20mV/div, 1us/div, AC coupled

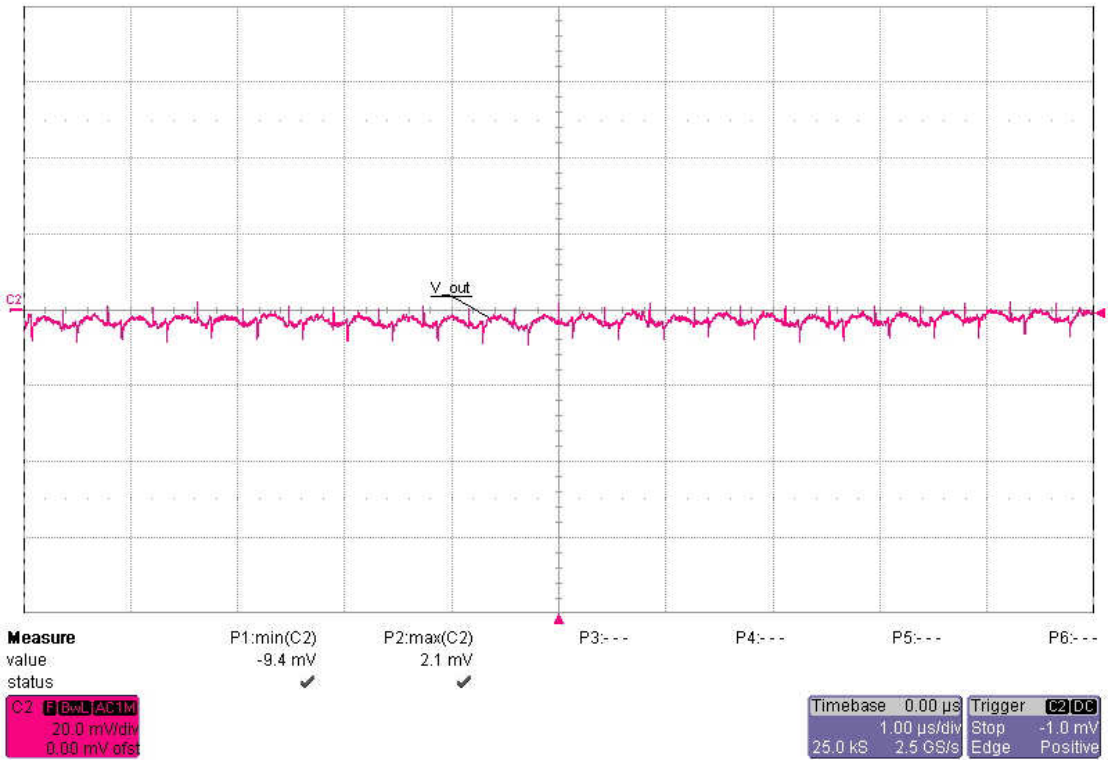


Figure 30

5.5 Efficiency & Load Regulation

The efficiency and load regulation are shown in Figure 31 and Figure 32.

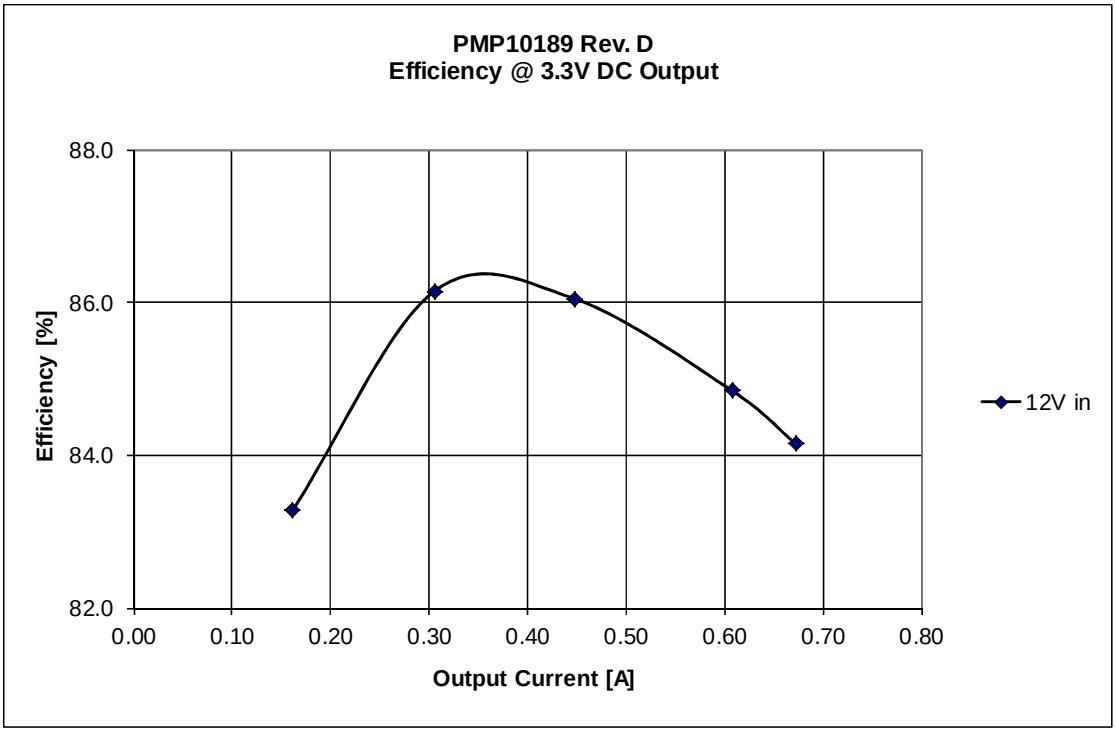


Figure 31

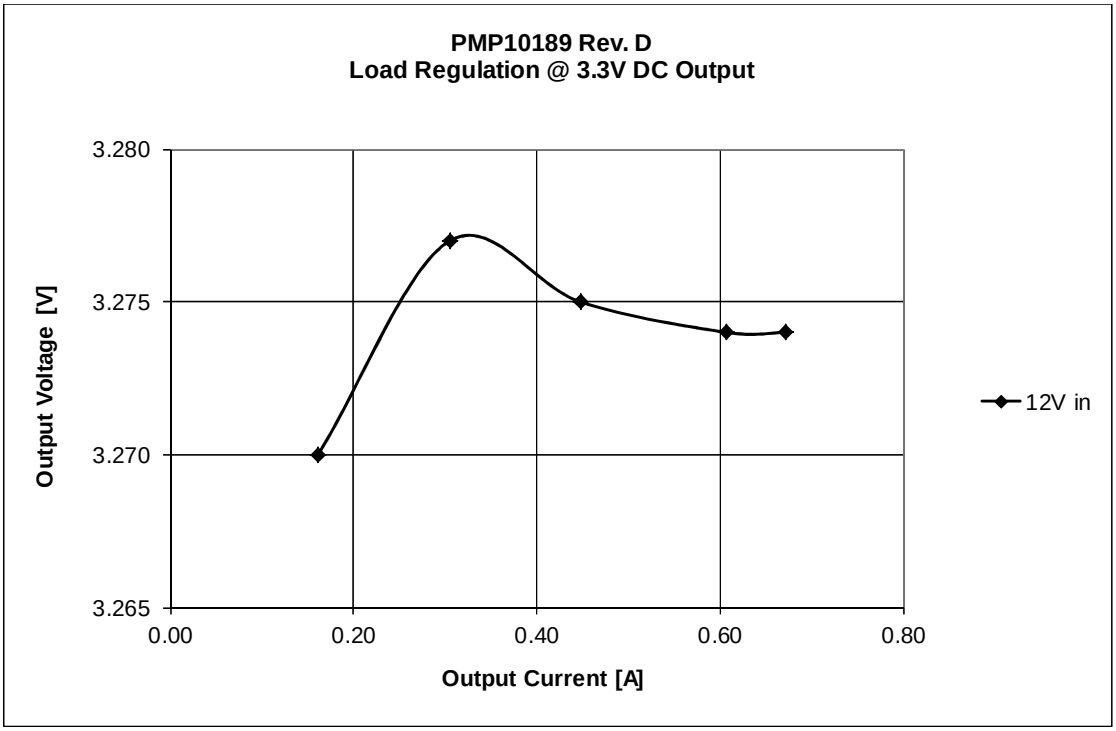


Figure 32

5.6 Frequency Response

Figure 33 shows the loop response at 12.0V input voltage and 620mA load.

12V input

- 620mA load 78 deg phase margin, 25.8 kHz bandwidth, -22 dB gain margin

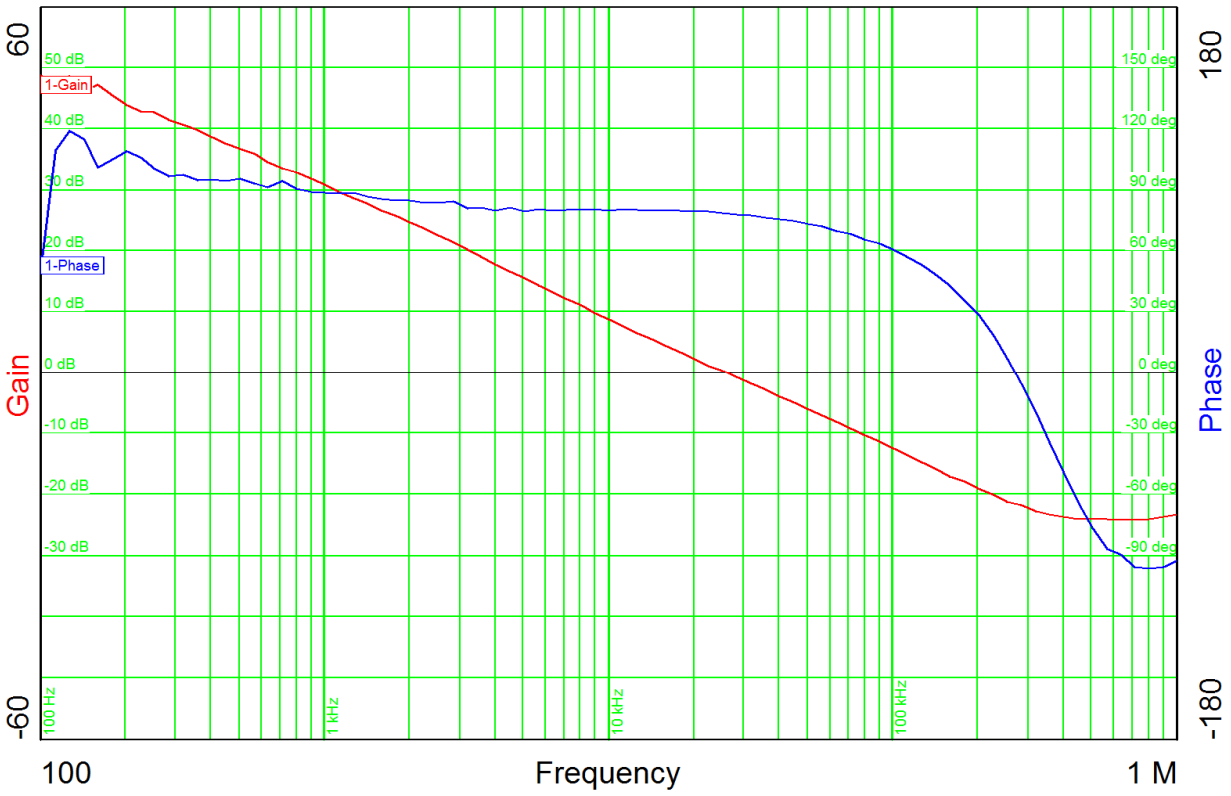


Figure 33

6 Thermal Measurement

The thermal image (Figure 34) shows the circuit at an ambient temperature of 21 °C with an input voltage of 54.0V and full load on all outputs.

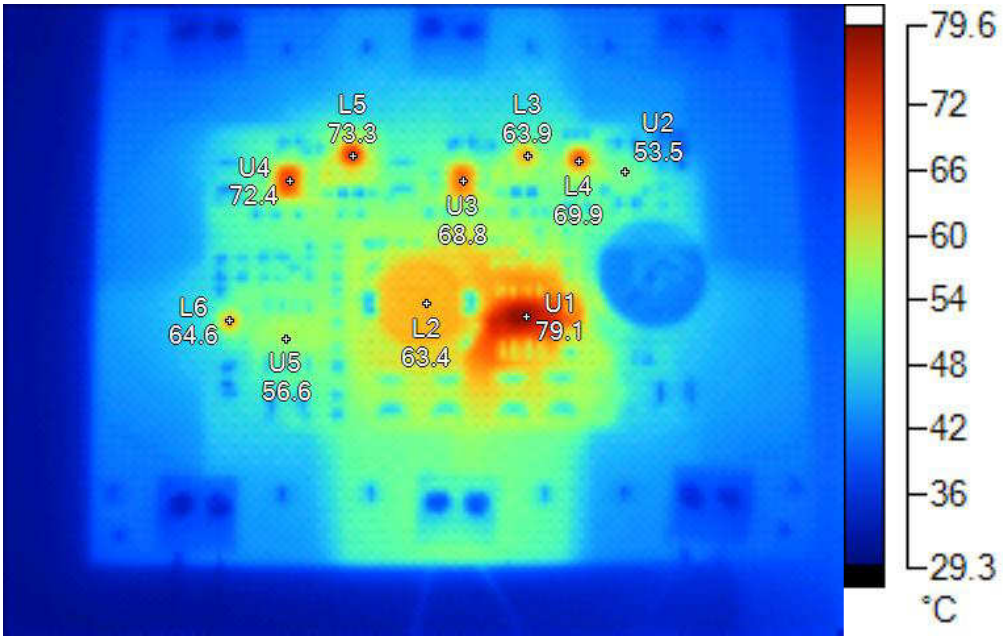


Figure 34

Markers

Name	Temperature	Emissivity	Background
L6	64.6°C	0.95	21.0°C
U5	56.6°C	0.95	21.0°C
L2	63.4°C	0.95	21.0°C
U1	79.1°C	0.95	21.0°C
U4	72.4°C	0.95	21.0°C
L5	73.3°C	0.95	21.0°C
U3	68.8°C	0.95	21.0°C
L3	63.9°C	0.95	21.0°C
L4	69.9°C	0.95	21.0°C
U2	53.5°C	0.95	21.0°C

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