Test Data
For PMP10712
08/011/2015

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1. Design Specifications

Vin Minimum	**3.3 V- Full Load**
Vin Maximum	**5.5V**
Vin Nominal	**3.6V**
Vout	**120V**
Iout	**10mA**
Switching Frequency(SMPS)	**130 KHz**
Isolation	**2KVAC**

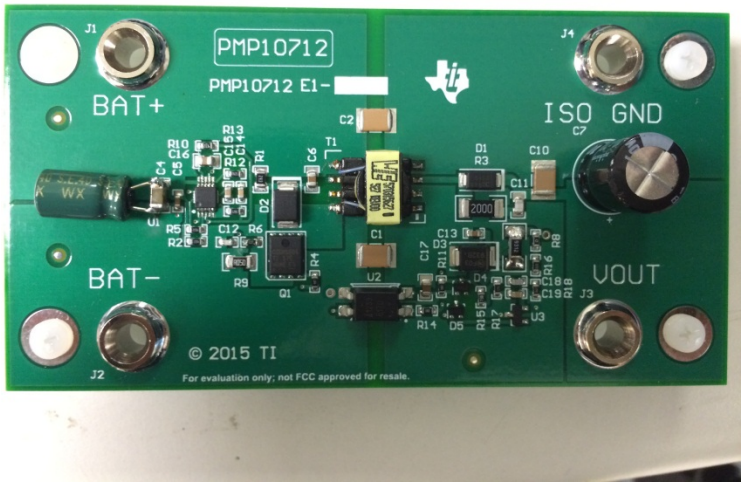
2. Circuit Description

PMP10712 is a 1.2W isolated flyback design that supports very low Vin of 3.3V-6V and is capable of delivering 10mA at 120V output. The design uses LM3481 Boost controller IC which works on current mode operation and can be synchronized to any frequency between 100KHz to 1 MHz.

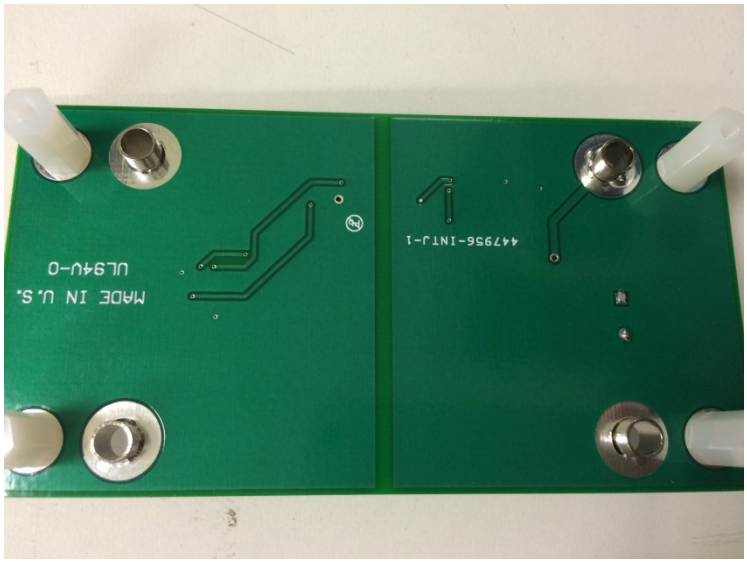
This design was built on a 2 layer board and is a simple, low-BOM-count, and low-cost design providing an isolated output.

3. PMP10712 Board Photos

Board Dimensions: 2125 mil *4055 mil

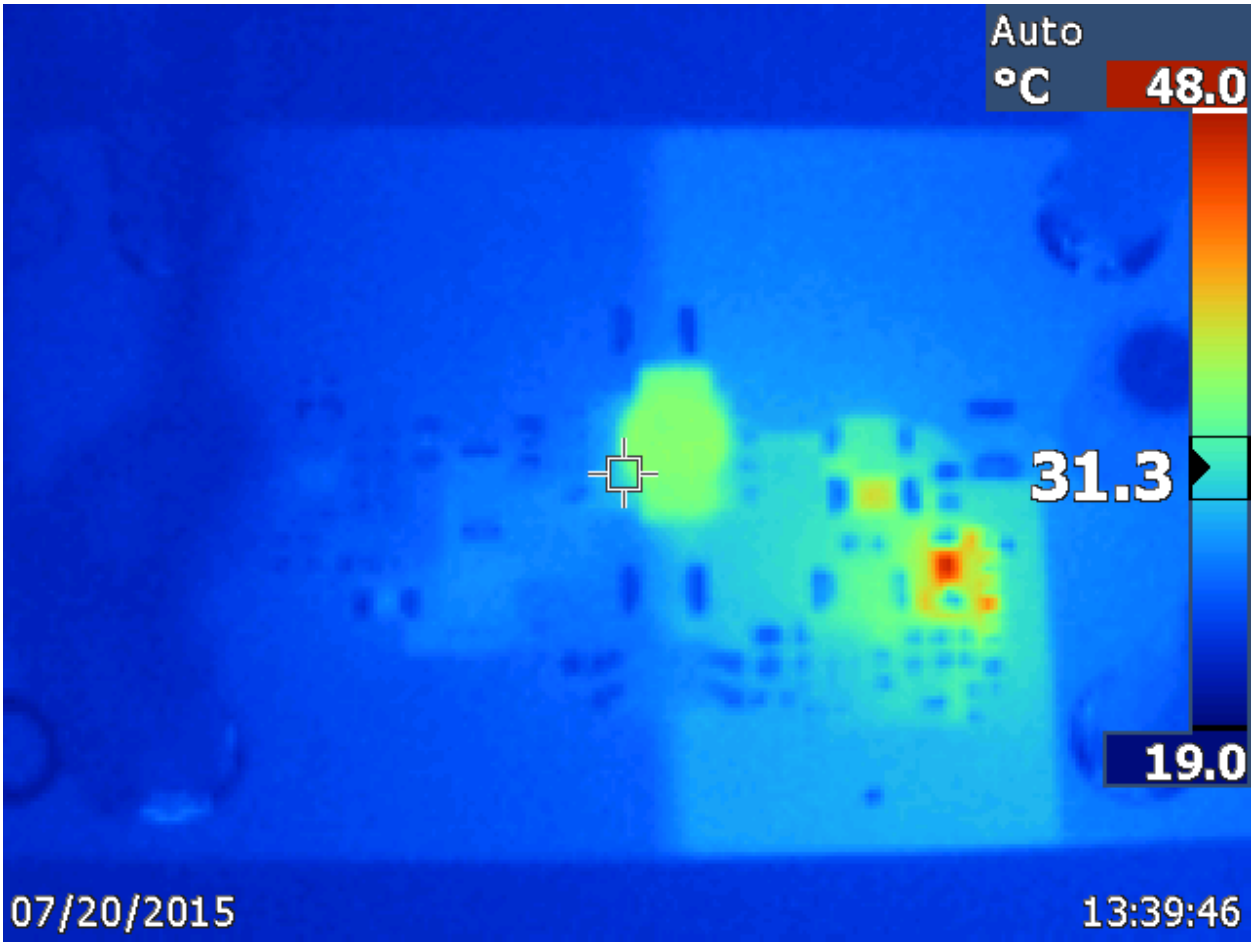


Board Photo (Top)



Board Photo (Bottom)

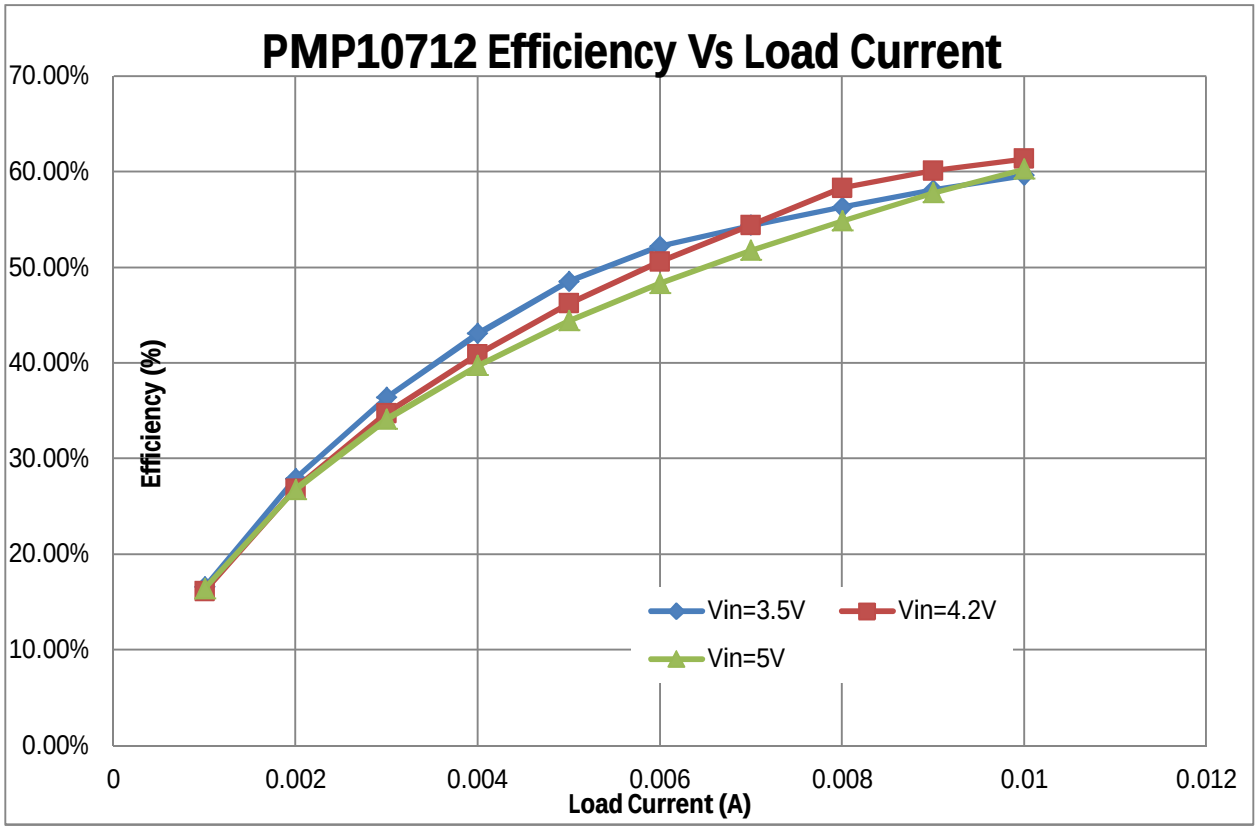
4. Thermal Data



IR thermal image taken at steady state with 3.5 Vin and 120V@10mA output

5. Test results

5.1 Efficiency Chart



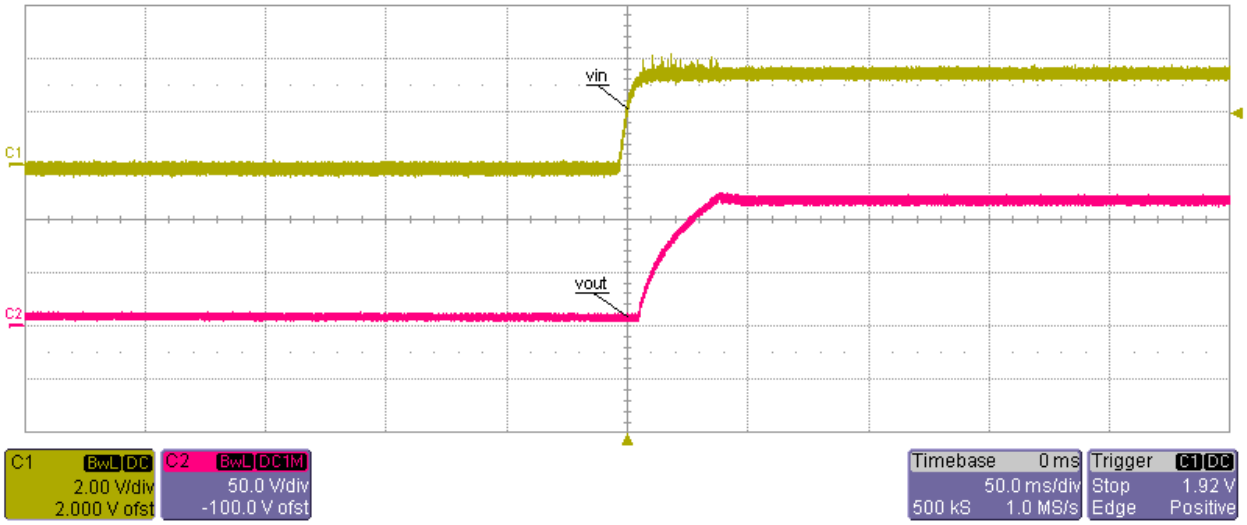
5.2 Efficiency Data

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Pin (W)	Pout (W)	Efficiency (%)
3.5	0.202	117.3	0.001	0.707	0.1173	16.59%
3.5	0.24	117.3	0.002	0.84	0.2346	27.93%
3.5	0.276	117.3	0.003	0.966	0.3519	36.43%
3.5	0.311	117.3	0.004	1.0885	0.4692	43.11%
3.5	0.345	117.3	0.005	1.2075	0.5865	48.57%
3.5	0.385	117.3	0.006	1.3475	0.7038	52.23%
3.5	0.431	117.3	0.007	1.5085	0.8211	54.43%
3.5	0.476	117.3	0.008	1.666	0.9384	56.33%
3.5	0.519	117.3	0.009	1.8165	1.0557	58.12%
3.5	0.562	117.3	0.01	1.967	1.173	59.63%
Vin (V)	**Iin (A)**	**Vout (V)**	**Iout (A)**	**Pin (W)**	**Pout (W)**	**Efficiency (%)**
4.2	0.173	117.3	0.001	0.7266	0.1173	16.14%
4.2	0.208	117.3	0.002	0.8736	0.2346	26.85%
4.2	0.241	117.3	0.003	1.0122	0.3519	34.77%
4.2	0.273	117.3	0.004	1.1466	0.4692	40.92%
4.2	0.302	117.3	0.005	1.2684	0.5865	46.24%
4.2	0.331	117.3	0.006	1.3902	0.7038	50.63%
4.2	0.359	117.3	0.007	1.5078	0.8211	54.46%
4.2	0.383	117.3	0.008	1.6086	0.9384	58.34%
4.2	0.418	117.3	0.009	1.7556	1.0557	60.13%
4.2	0.455	117.3	0.01	1.911	1.173	61.38%

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Pin (W)	Pout (W)	Efficiency (%)
5	0.143	117.3	0.001	0.715	0.1173	16.41%
5	0.175	117.3	0.002	0.875	0.2346	26.81%
5	0.206	117.3	0.003	1.03	0.3519	34.17%
5	0.236	117.3	0.004	1.18	0.4692	39.76%
5	0.264	117.3	0.005	1.32	0.5865	44.43%
5	0.291	117.3	0.006	1.455	0.7038	48.37%
5	0.317	117.3	0.007	1.585	0.8211	51.80%
5	0.342	117.3	0.008	1.71	0.9384	54.88%
5	0.365	117.3	0.009	1.825	1.0557	57.85%
5	0.389	117.3	0.01	1.945	1.173	60.31%

6. Test results

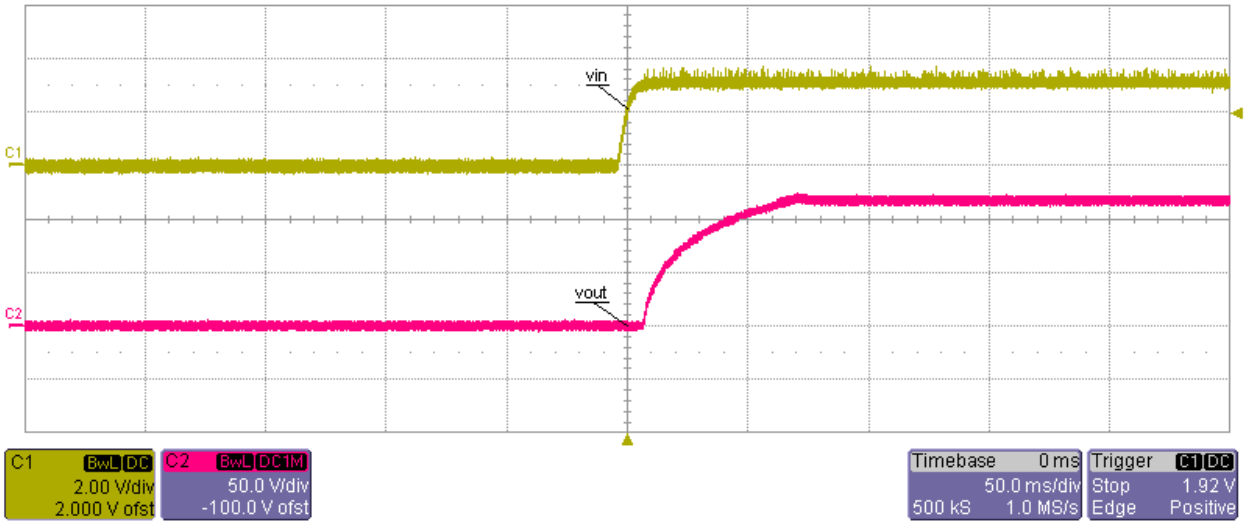
6.1 Startup



Startup into No Load at 3.5 Vin

C1- Vin

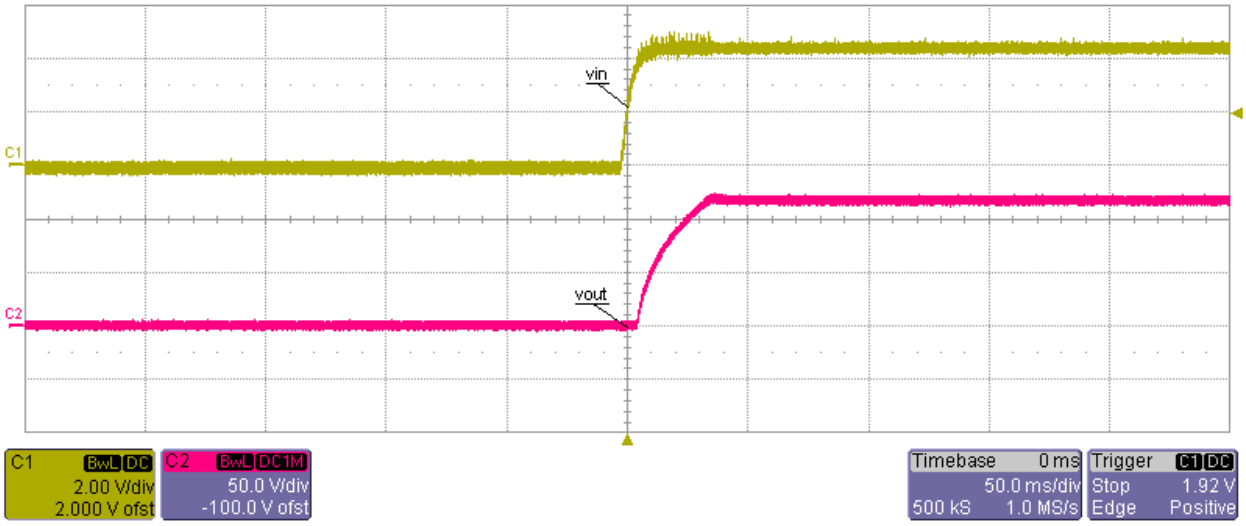
C2-Vout



Startup into Full Load(10mA) at 3.5 Vin

C1- Vin

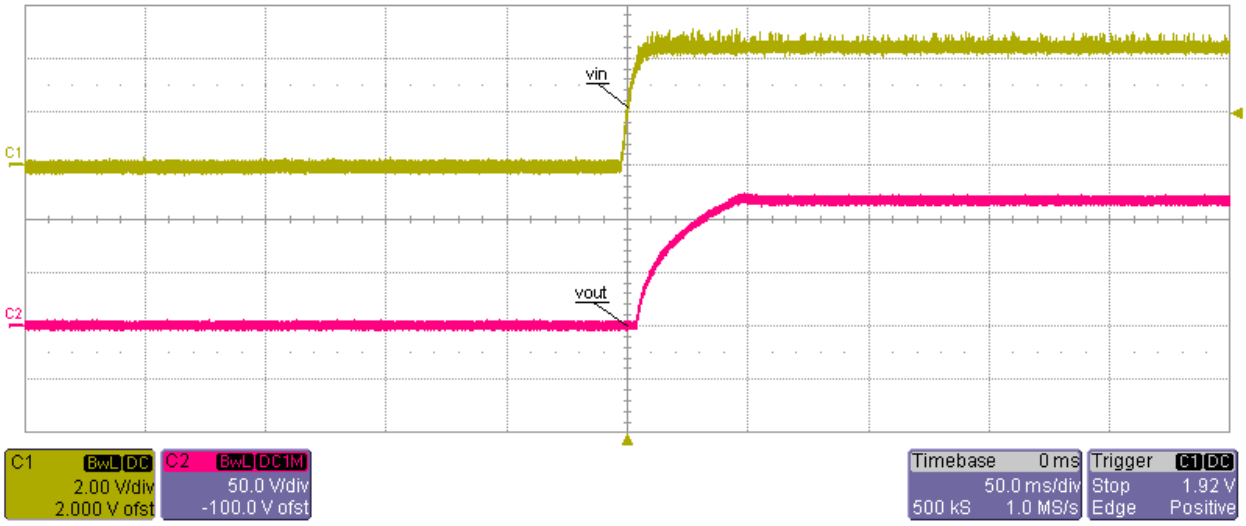
C2-Vout



Startup into No Load at 5 Vin

C1- Vin

C2-Vout

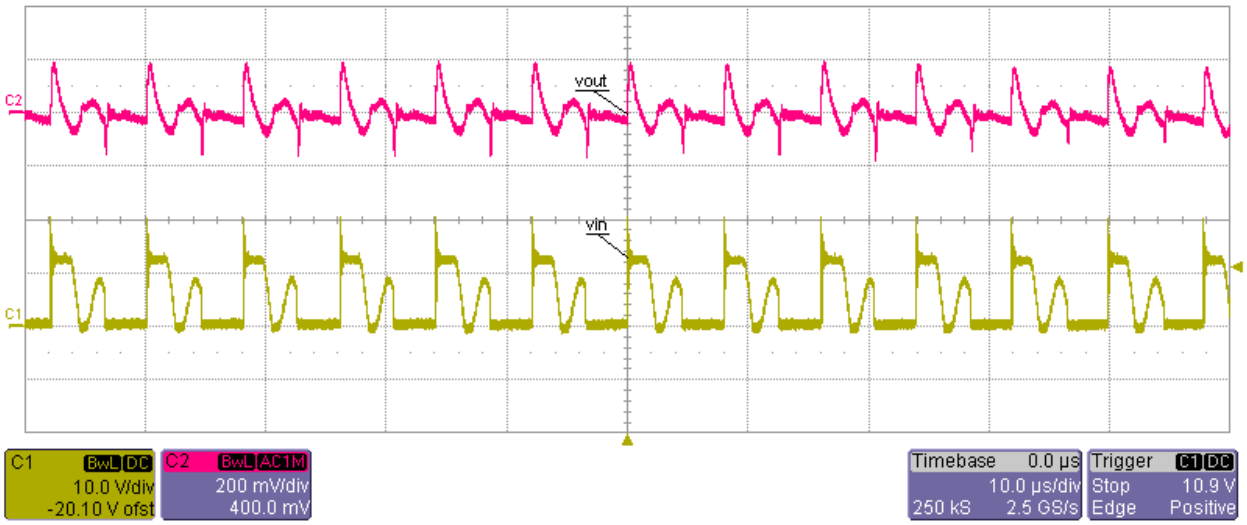


Startup into Full Load(10mA) at 5 Vin

C1- Vin

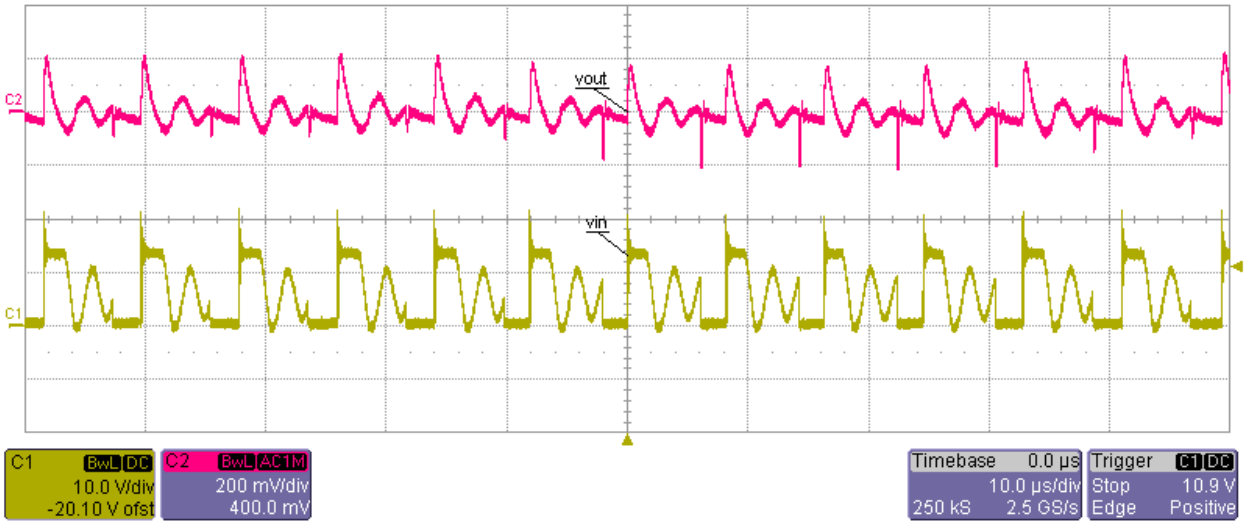
C2-Vout

6.2 Output Voltage Ripple and Switch Node Voltage



Ch1 - Switch Node Voltage

Ch2-Output Voltage Ripple at 3.5Vin @ 10mA output



Ch1 - Switch Node Voltage

Ch2-Output Voltage Ripple at 5Vin @ 10mA output

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