Test Data
For PMP9291
2/5/2014

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1. Design Specifications

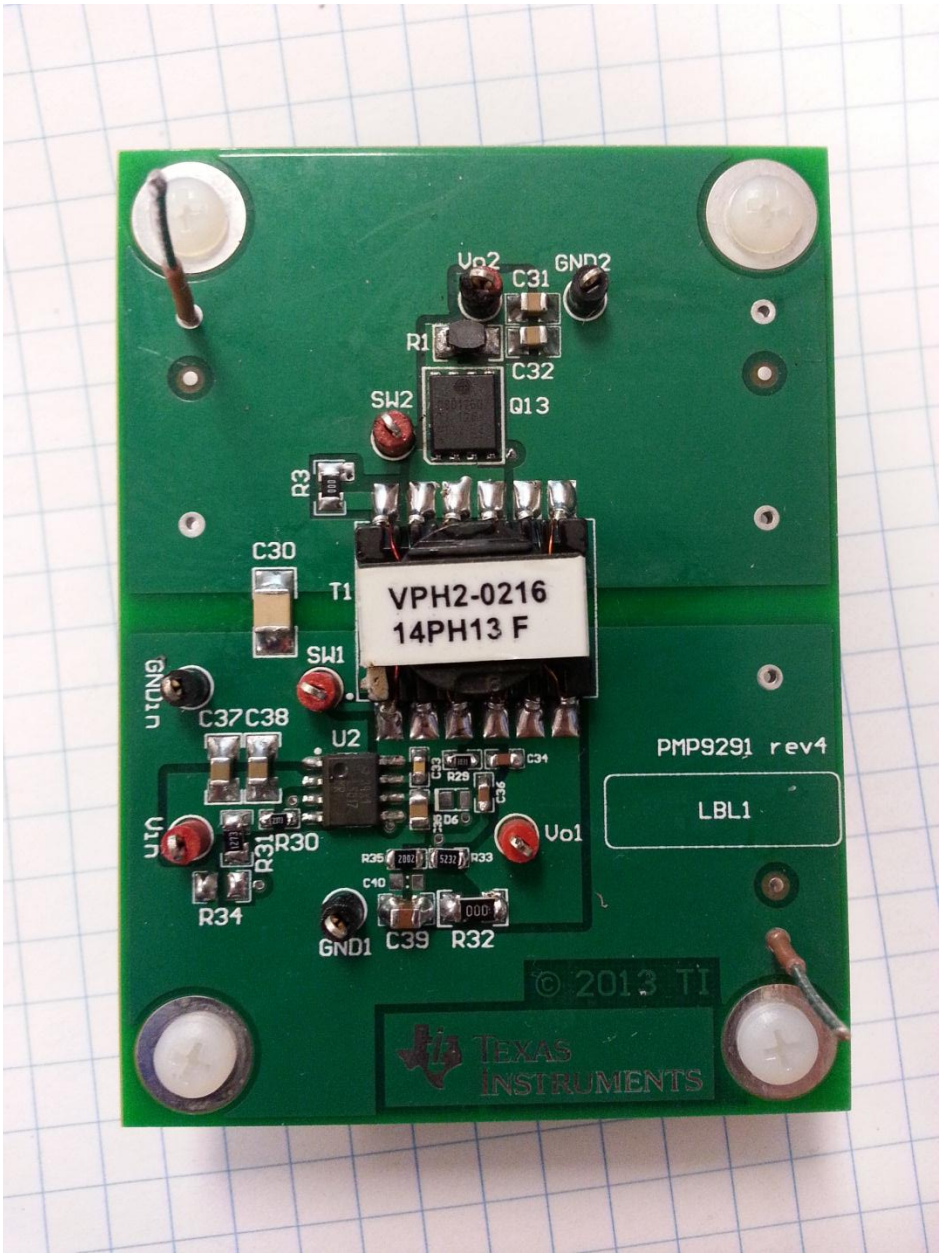
Vin	**10.8VDC to 13.2VDC (12VDC Nominal)**
Vout	**5VDC**
Iout	**0.3A Max.**
Approximate Switching Frequency	**≈240KHz**

2. Circuit Description

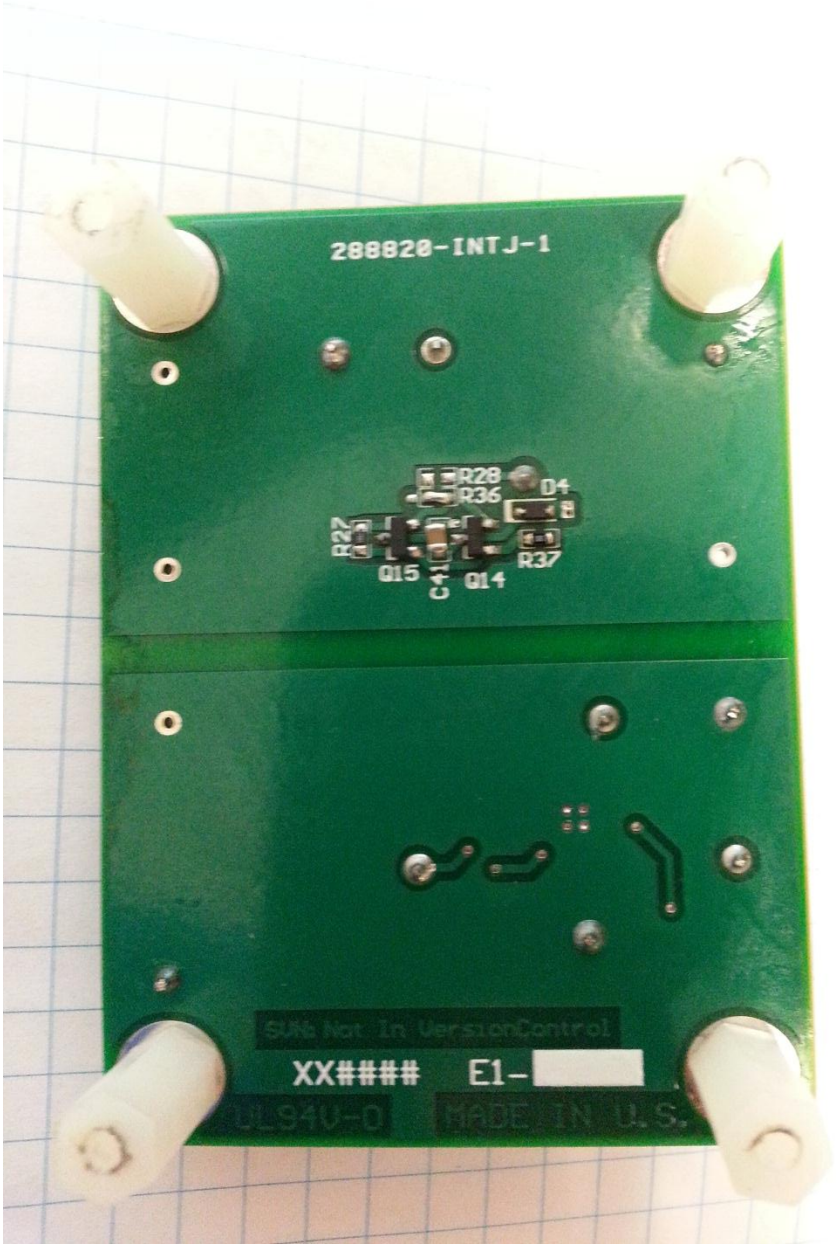
PMP9291 is an Isolated Flybuck Converter using a synchronous buck regulator with Self-Driven Synchronous Rectification on the Secondary Side. The design accepts an input voltage of 10.8Vin to 13.2Vin and provides an isolated output of 5Vout capable of supplying a maximum of 0.3A of current to the load. This design was built on a 4-layer PCB. The secondary-side self-driven synchronous rectification offers benefits of higher efficiency, no need for pre-load, and much lower output voltage tolerances (4.916Vout ± 3.1% over entire line and load range) without the need for opto-coupler and discrete voltage reference. A comparison of output voltage regulation over line and load between this design and an analogous non-synchronous flybuck converter (PMP9354) are given and compared in Sections 5.5 and 5.6. The design uses a readily-available off-the-shelf VERSA-PAC series transformer.

3. PMP9291 Board Photos

Board Dimensions: 2” x 2.7”

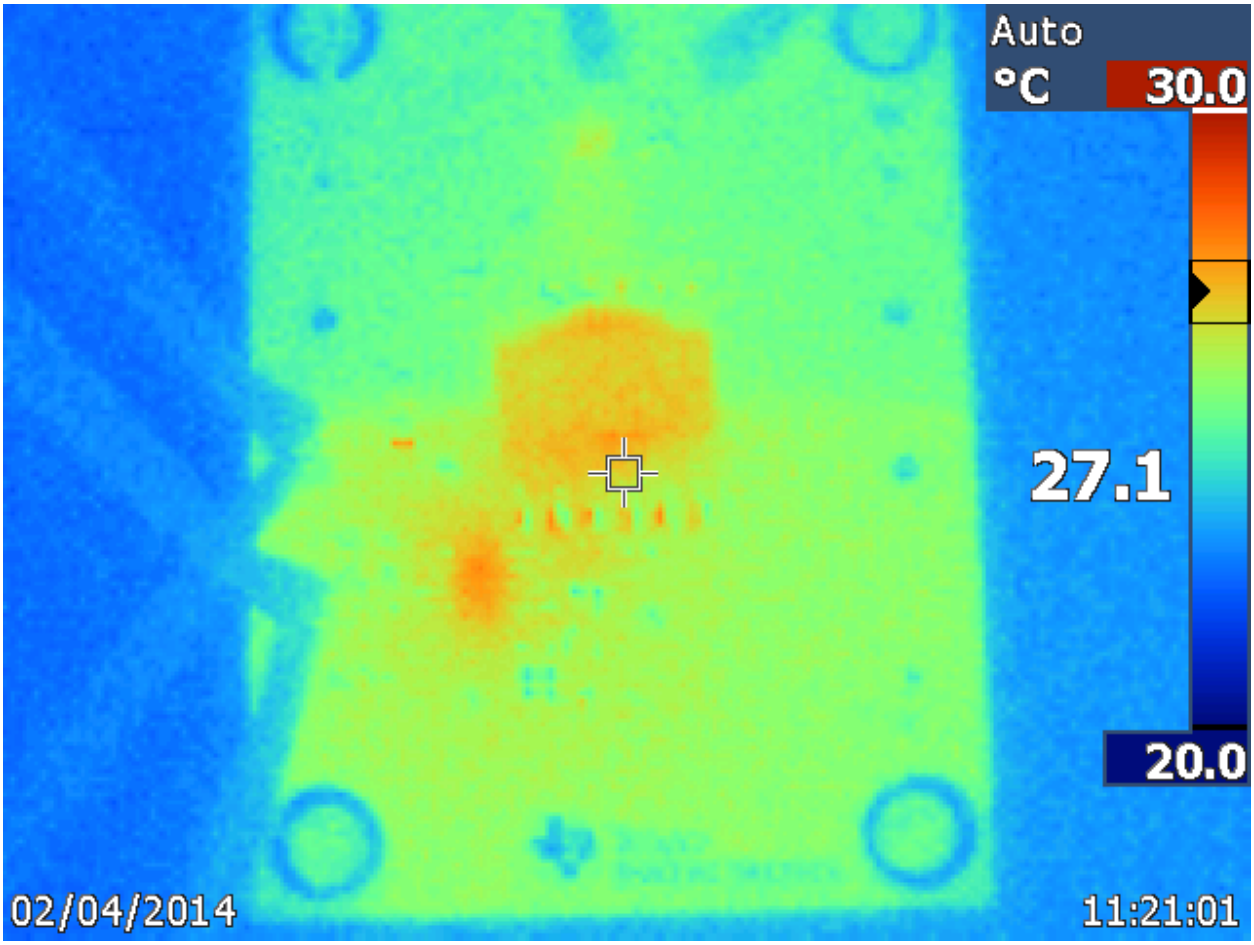


Board Photo (Top)



Board Photo (Bottom)

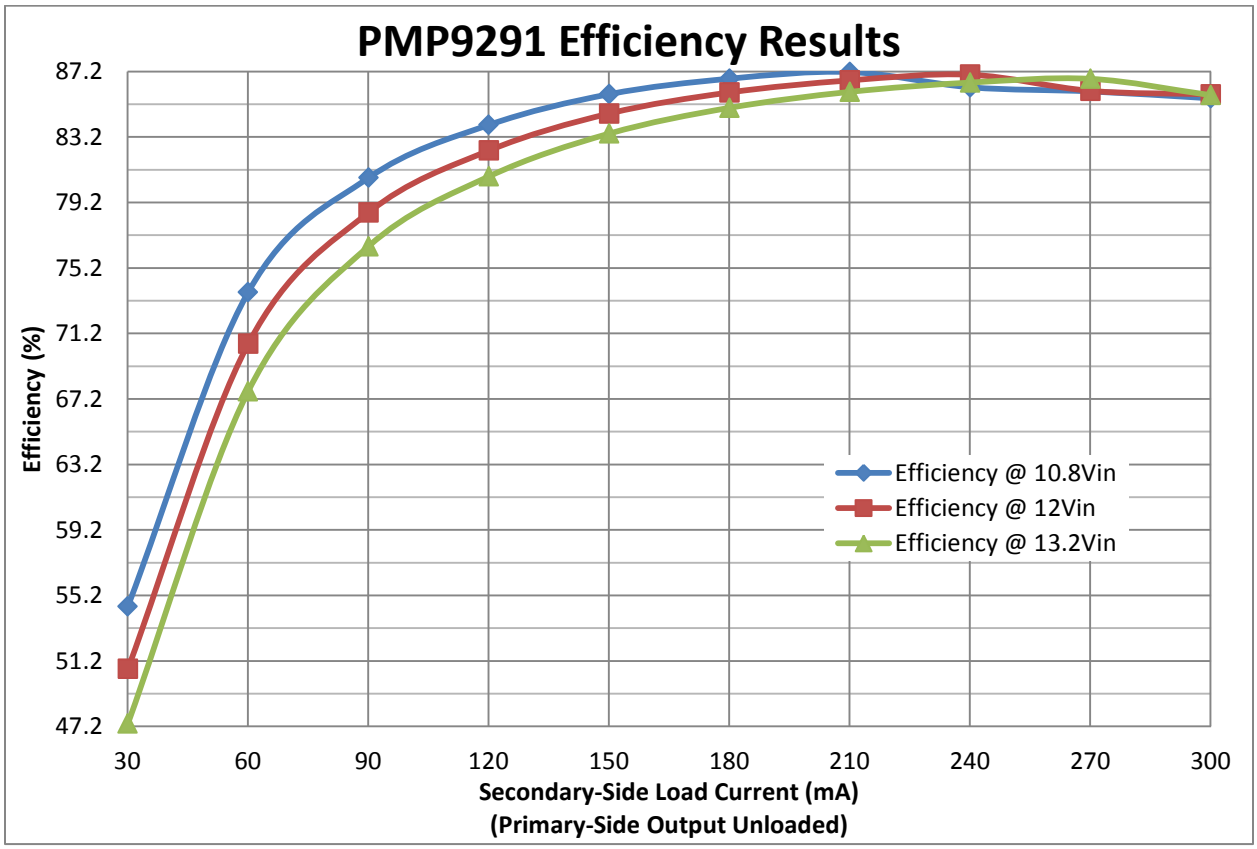
4. Thermal Data



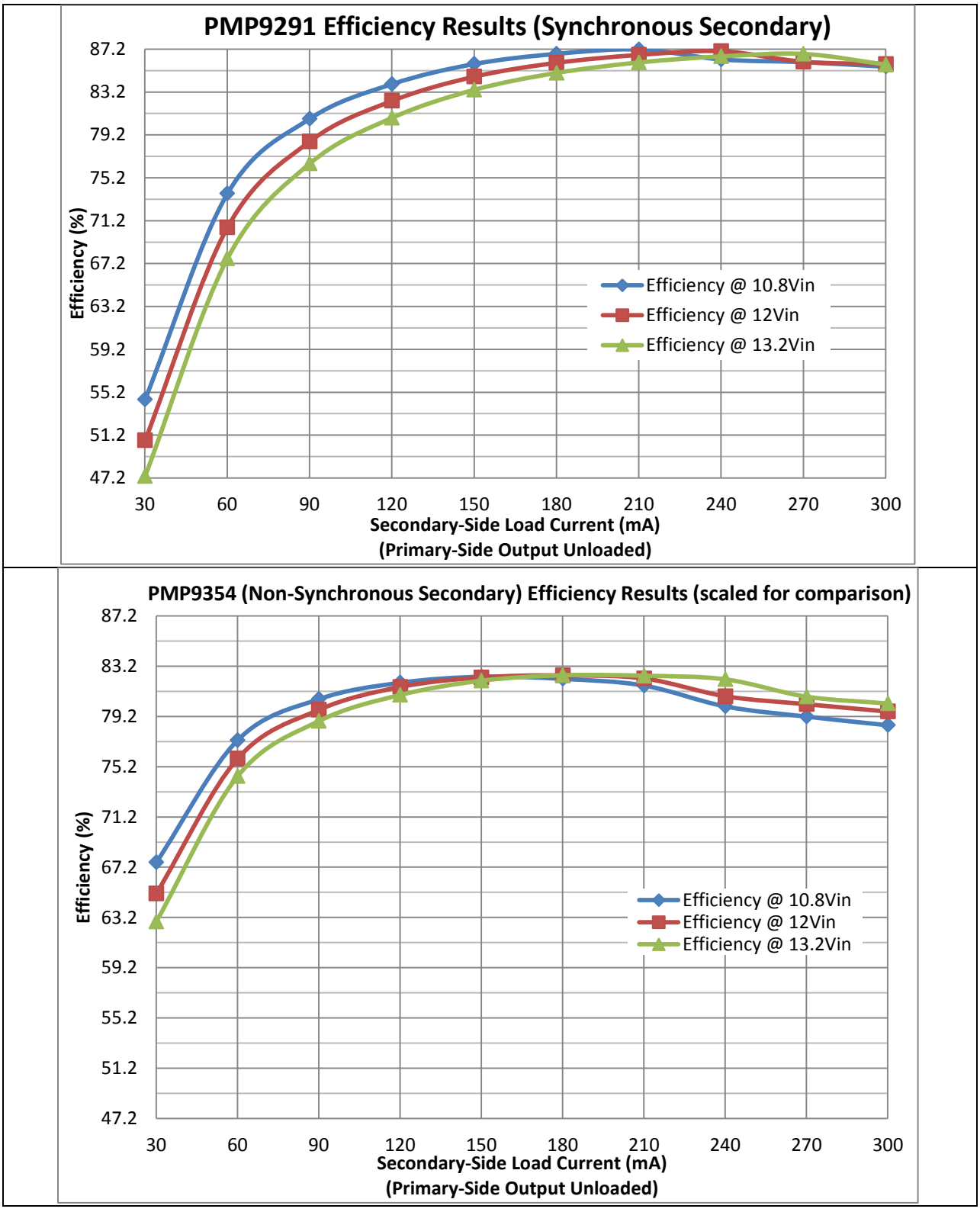
IR thermal image taken at steady state with 12Vin and 0.3A load (no airflow)

5. Efficiency and Line/Load Regulation

5.1 Efficiency Chart



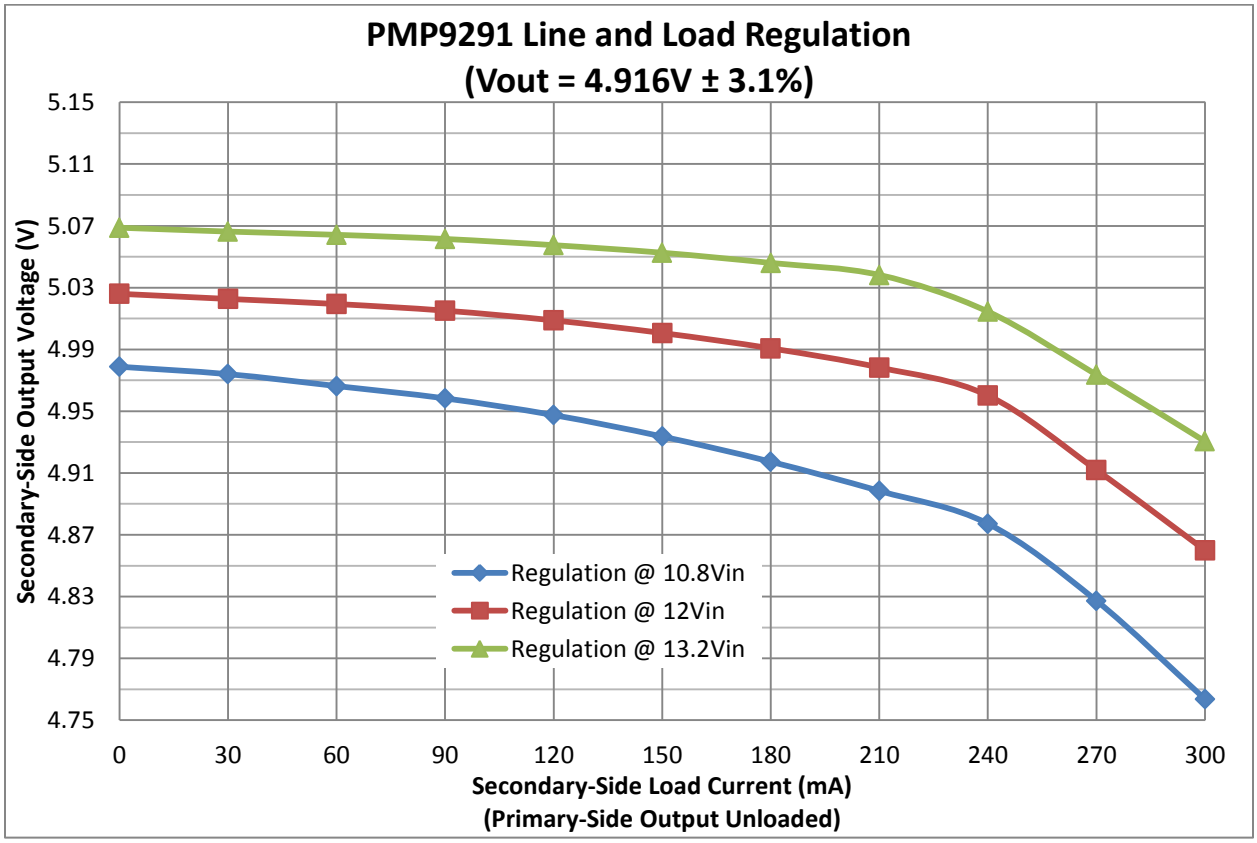
5.2 Efficiency Comparison between PMP9291 (Synchronous Secondary) and PMP9354 (Non-Synchronous Secondary)



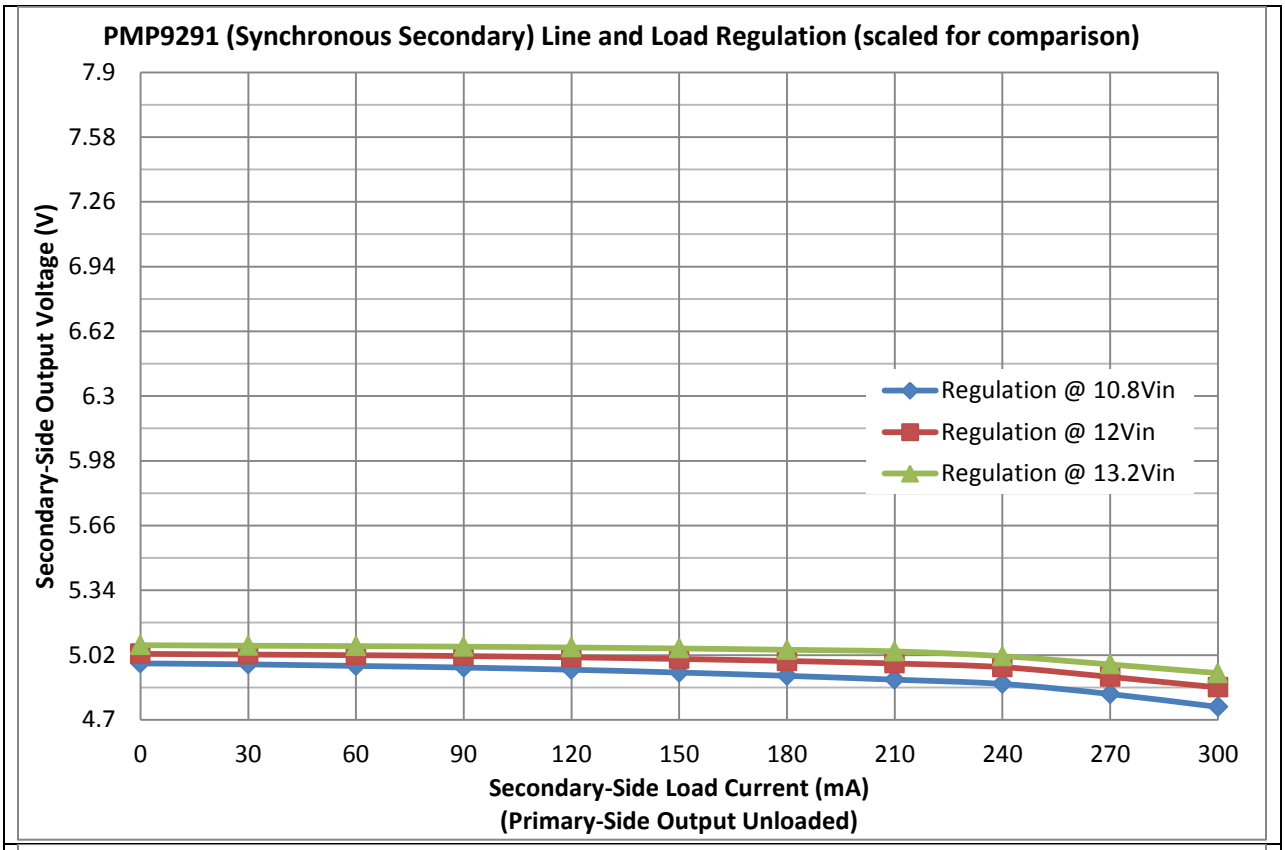
5.3 Efficiency and Line/Load Regulation Data

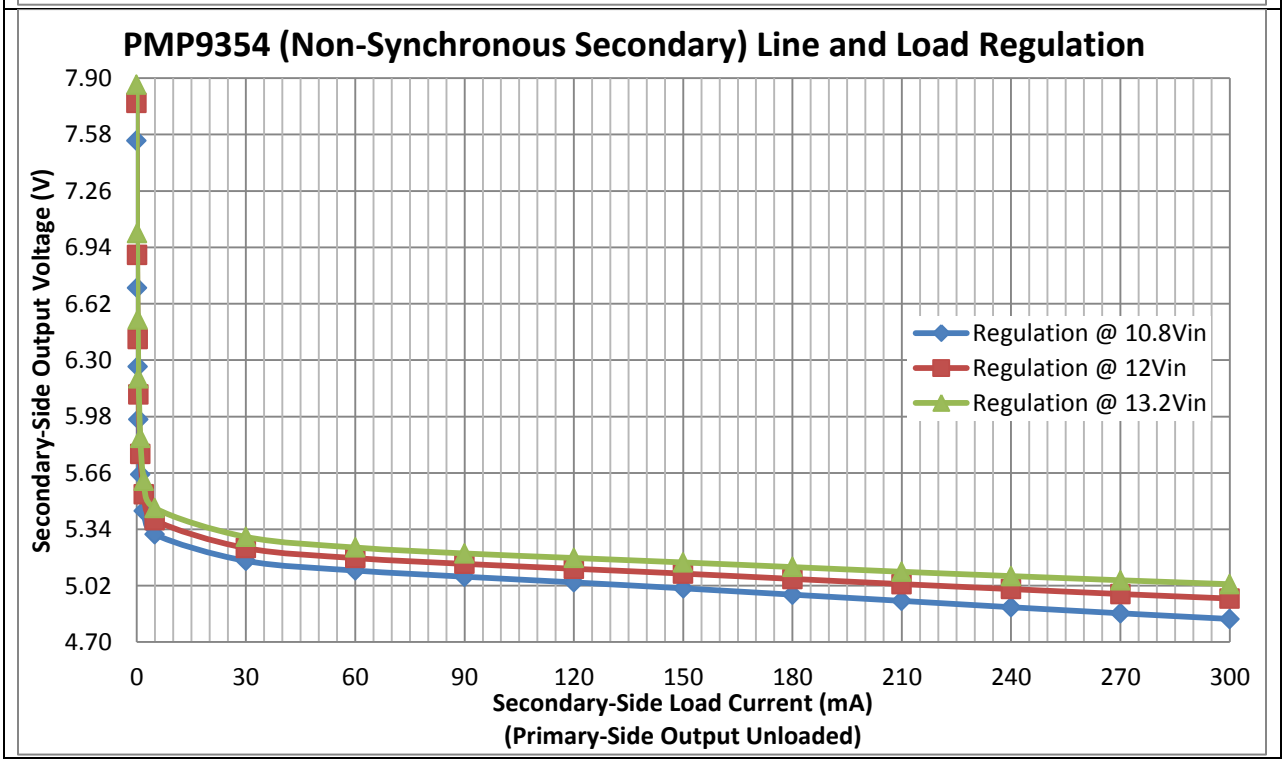
Vin (V)	Iin (mA)	Vout (V)	Iout (mA)	Pin (W)	Pout (W)	Efficiency (%)
10.80	13.271	4.9788	0	0.1433	0.0000	
10.80	25.338	4.974	29.992	0.2736	0.1492	54.5
10.80	37.43	4.9663	59.996	0.4042	0.2980	73.7
10.80	51.216	4.9583	90.008	0.5530	0.4463	80.7
10.80	65.507	4.9475	119.992	0.7073	0.5937	83.9
10.80	79.887	4.9336	150.03	0.8625	0.7402	85.8
10.80	94.497	4.9173	180	1.0202	0.8851	86.8
10.80	109.32	4.8984	210.02	1.1802	1.0288	87.2
10.80	125.72	4.8772	240.01	1.3574	1.1706	86.2
10.80	140.41	4.8273	270.03	1.5160	1.3035	86.0
10.80	154.71	4.7636	300.02	1.6704	1.4292	85.6
Vin (V)	**Iin (mA)**	**Vout (V)**	**Iout (mA)**	**Pin (W)**	**Pout (W)**	**Efficiency (%)**
12.00	14.07	5.026	0	0.1688	0.0000	
12.00	24.777	5.0227	30.013	0.2972	0.1507	50.7
12.00	35.575	5.0194	59.998	0.4268	0.3012	70.6
12.00	47.875	5.0151	90.001	0.5744	0.4514	78.6
12.00	60.822	5.0088	119.997	0.7297	0.6010	82.4
12.00	73.89	5.0006	150.03	0.8865	0.7502	84.6
12.00	87.157	4.9907	180	1.0455	0.8983	85.9
12.00	100.575	4.9783	210.02	1.2065	1.0455	86.7
12.00	114.06	4.9602	240	1.3683	1.1904	87.0
12.00	128.52	4.912	270.01	1.5419	1.3263	86.0
12.00	141.66	4.86	300.02	1.6994	1.4581	85.8
Vin (V)	**Iin (mA)**	**Vout (V)**	**Iout (mA)**	**Pin (W)**	**Pout (W)**	**Efficiency (%)**
13.20	14.689	5.0688	0	0.1939	0.0000	
13.20	24.312	5.0663	29.993	0.3208	0.1520	47.4
13.20	34.024	5.0642	59.997	0.4490	0.3038	67.7
13.20	45.109	5.0615	90	0.5953	0.4555	76.5
13.20	56.921	5.0575	119.995	0.7512	0.6069	80.8
13.20	68.858	5.0526	150.01	0.9087	0.7579	83.4
13.20	80.998	5.046	180.01	1.0688	0.9083	85.0
13.20	93.285	5.0382	210.02	1.2310	1.0581	86.0
13.20	105.41	5.0145	240.01	1.3910	1.2035	86.5
13.20	117.309	4.9736	270.01	1.5480	1.3429	86.8
13.20	130.7	4.9305	300	1.7248	1.4792	85.8

5.4 Line and Load Regulation

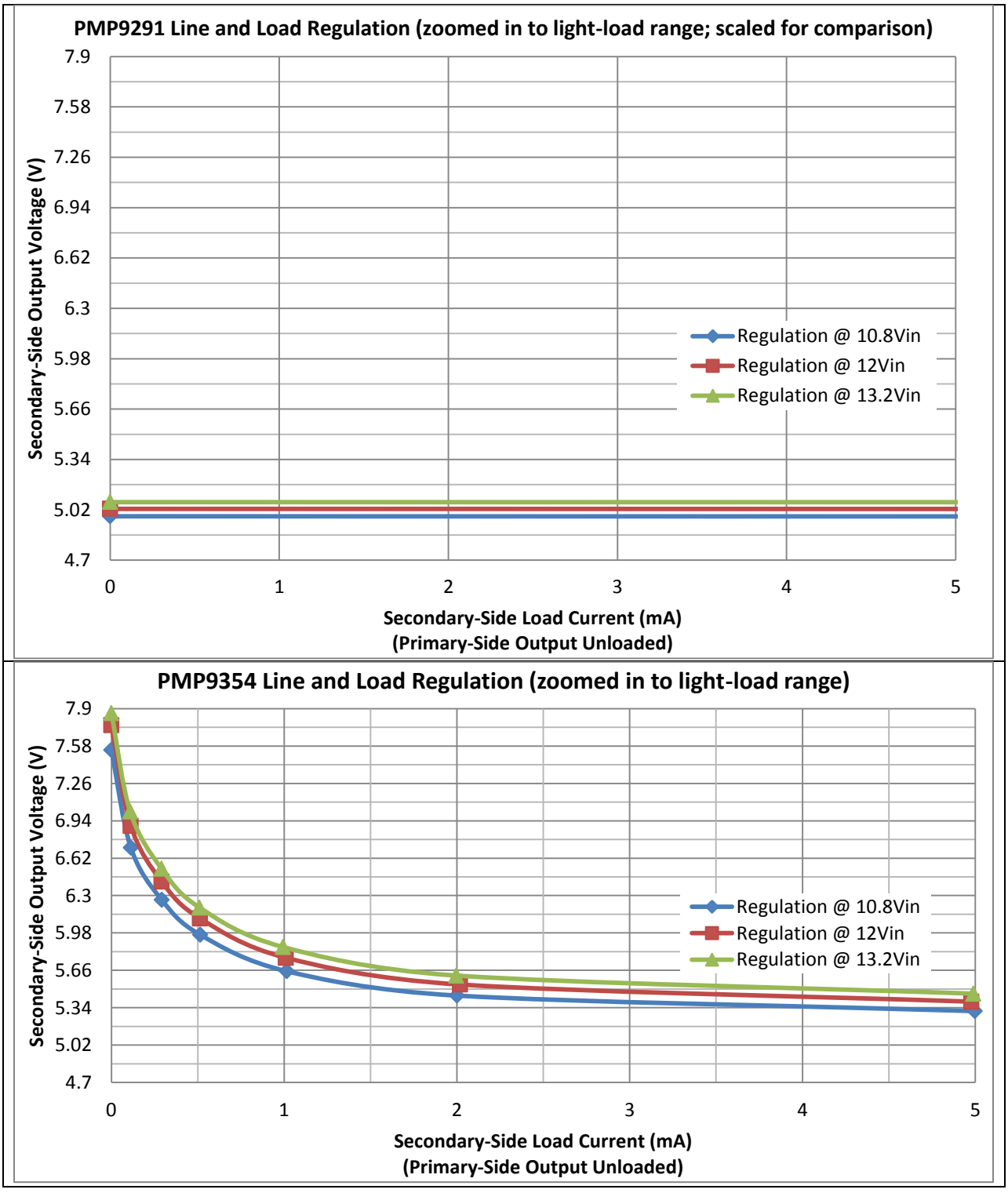


5.5 Line and Load Regulation Comparison between Self-Driven Synchronous Rectification and Diode (Non-Synchronous) Rectification



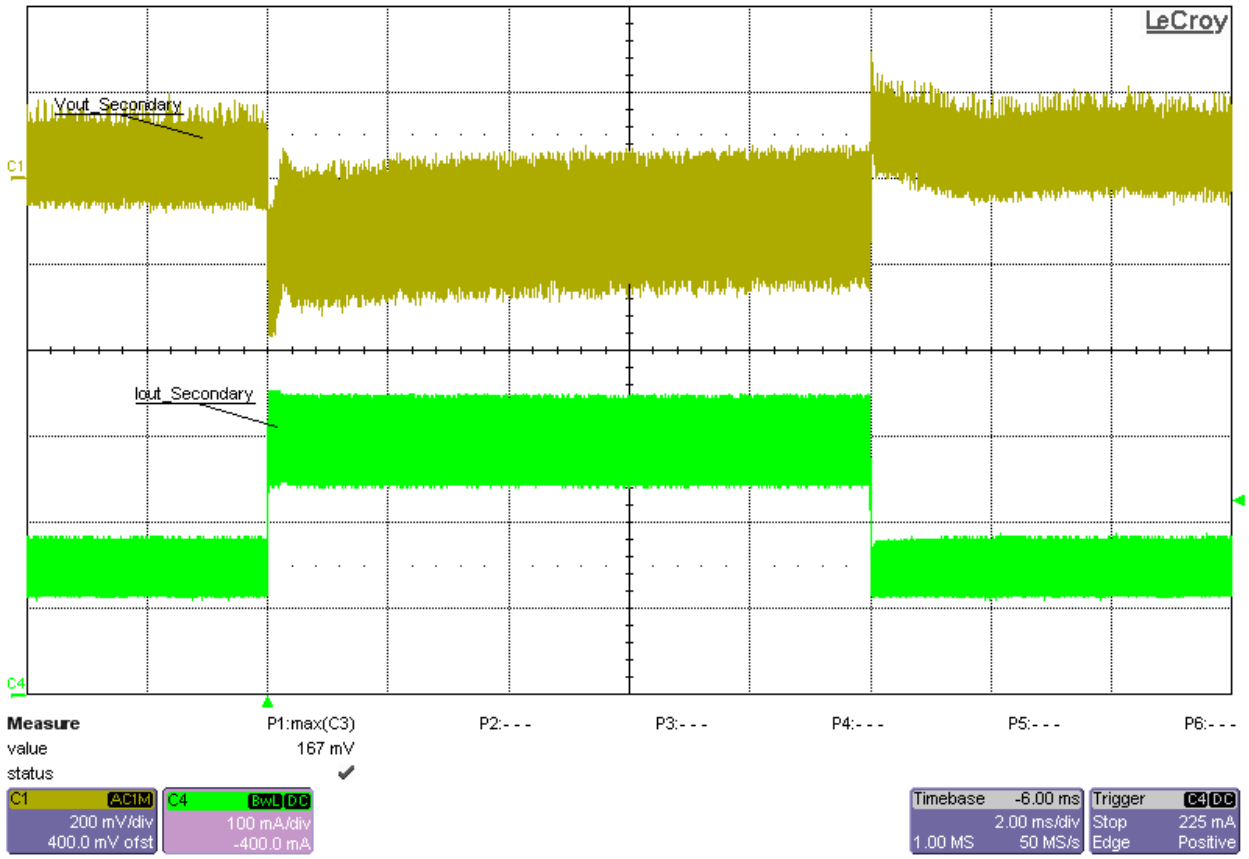


5.6 Line and Load Regulation Comparison between Self-Driven Synchronous Rectification and Diode (Non-Synchronous) Rectification (Zoomed in to light load range)

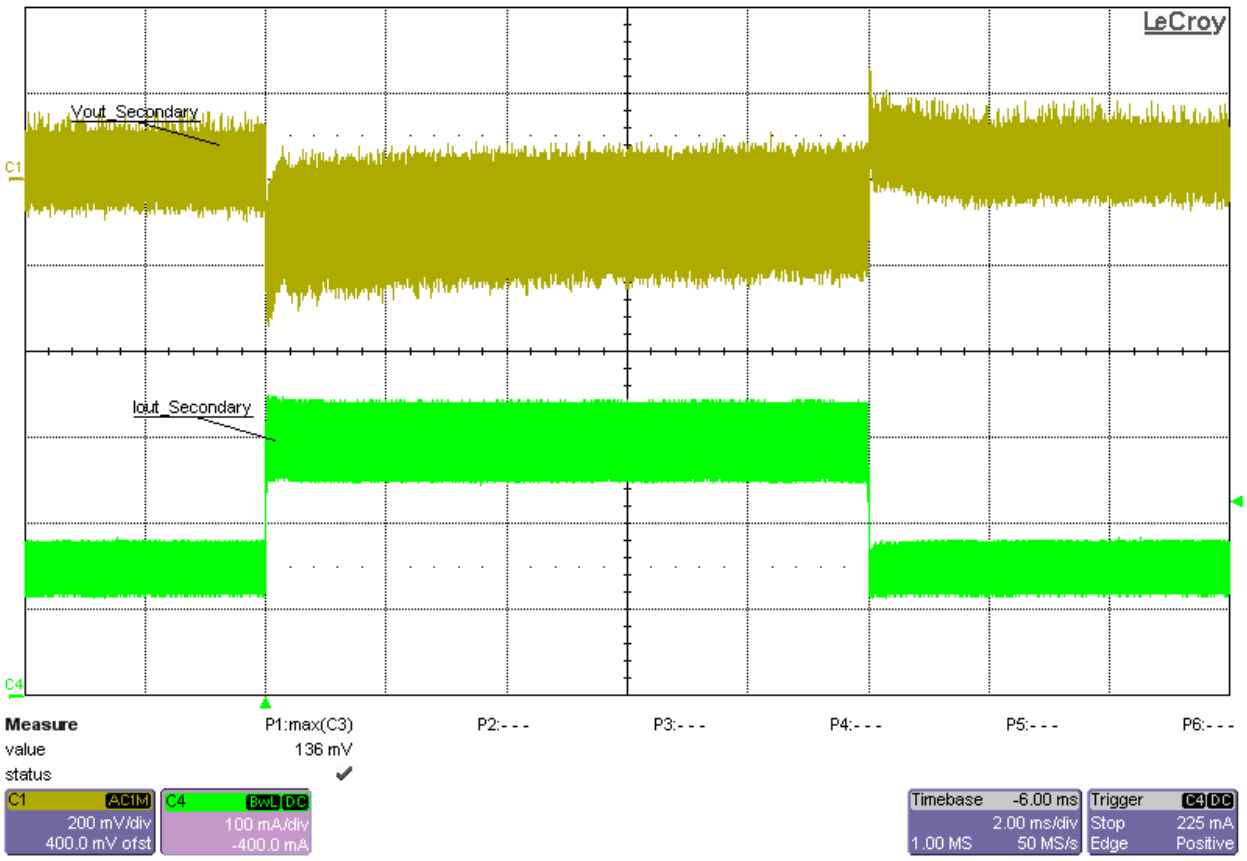


6 Waveforms

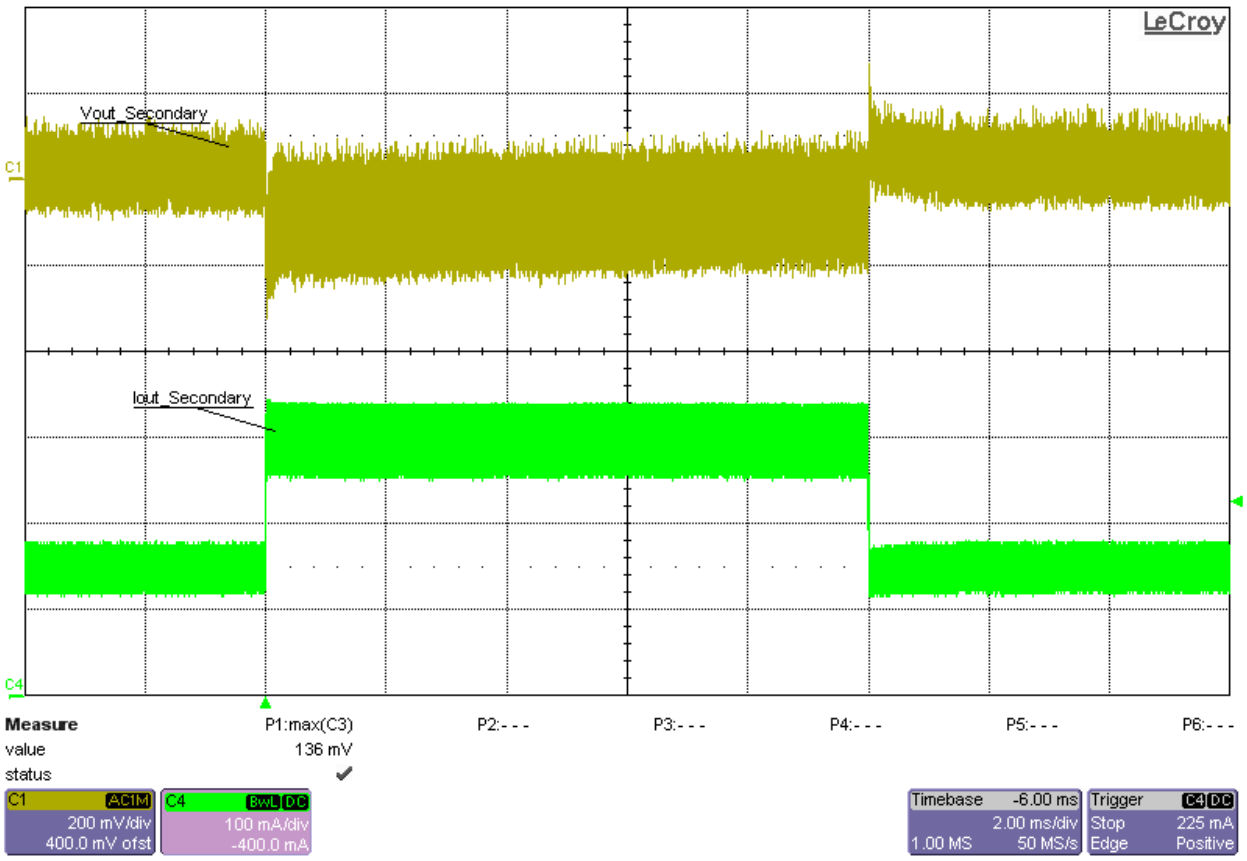
6.1 Load Transient Response



Load Transient Response at 10.8Vin and 50%-to-100% (150mA-to-300mA) Load Step

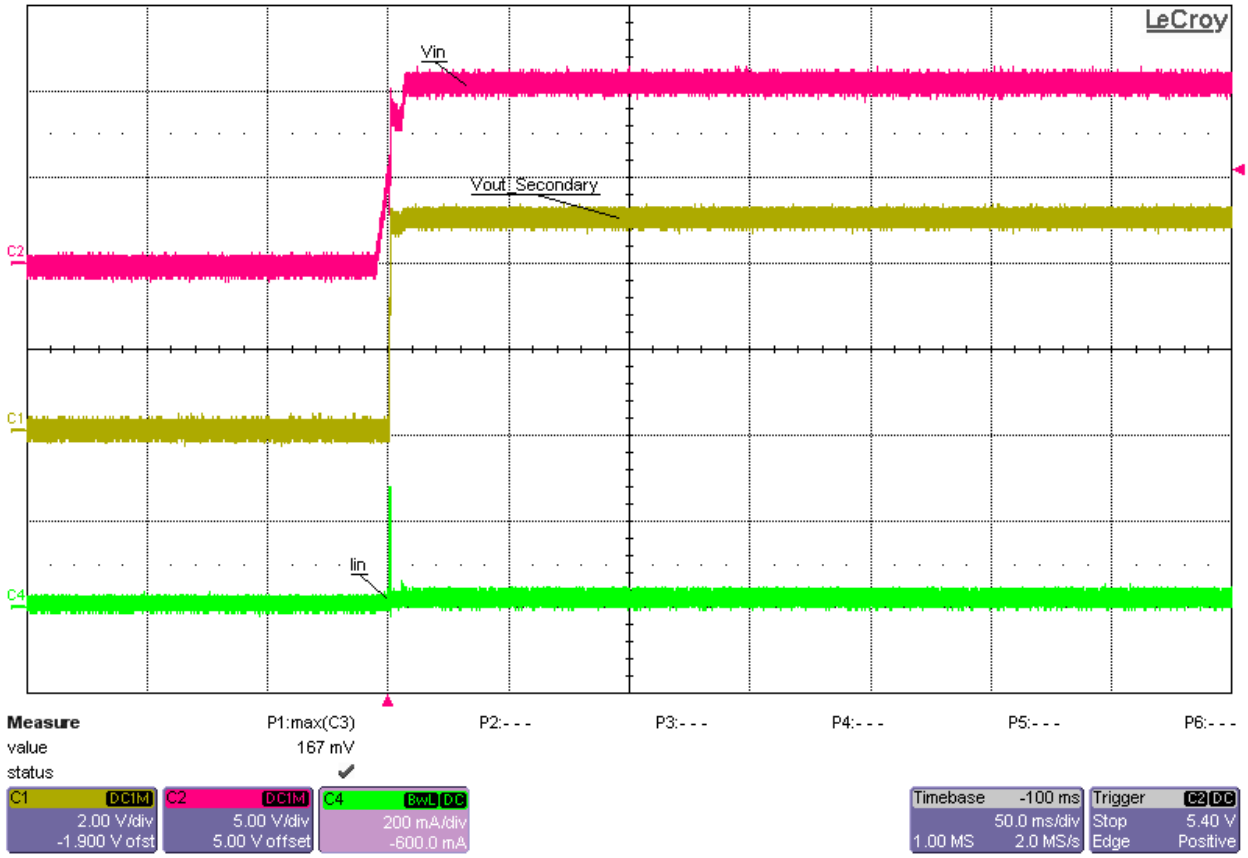


Load Transient Response at 12Vin and 50%-to-100% (150mA-to-300mA) Load Step

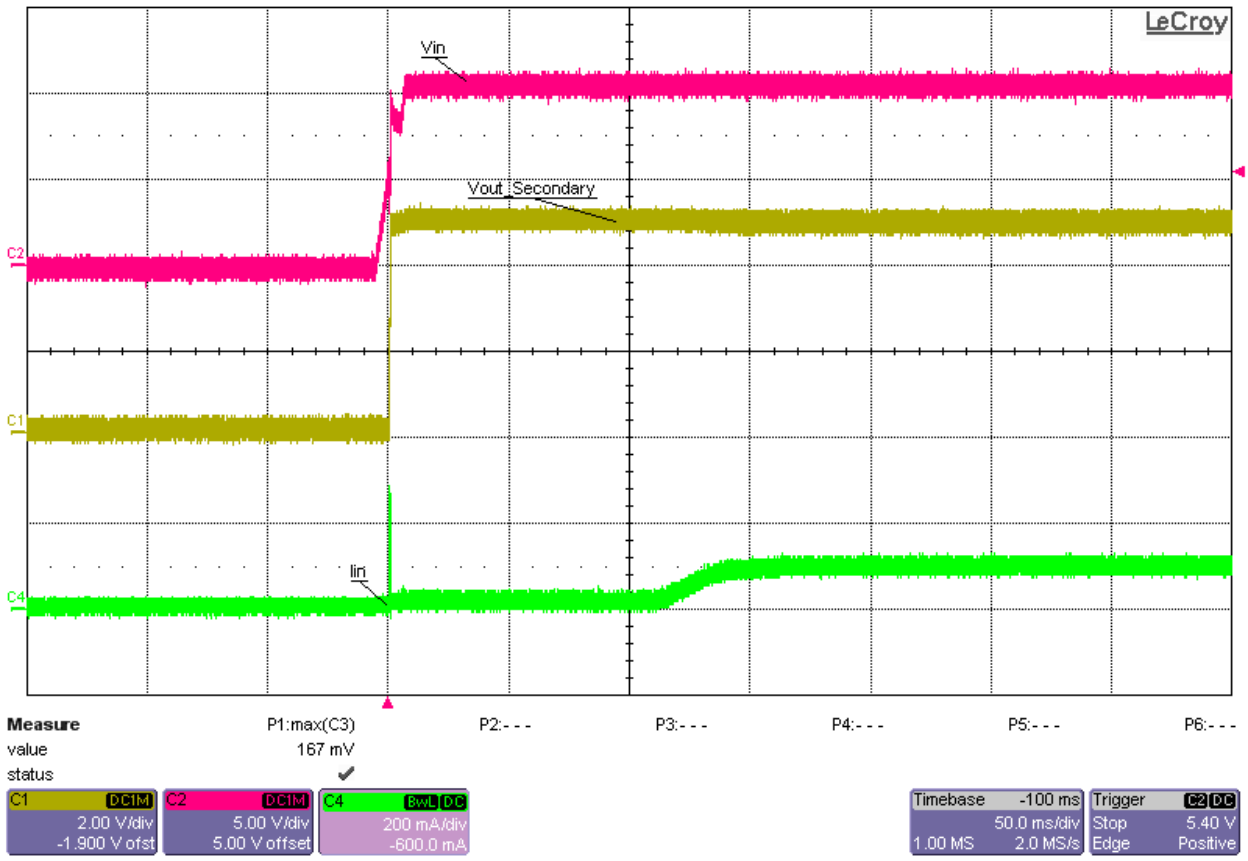


Load Transient Response at 13.2Vin and 50%-to-100% (150mA-to-300mA) Load Step

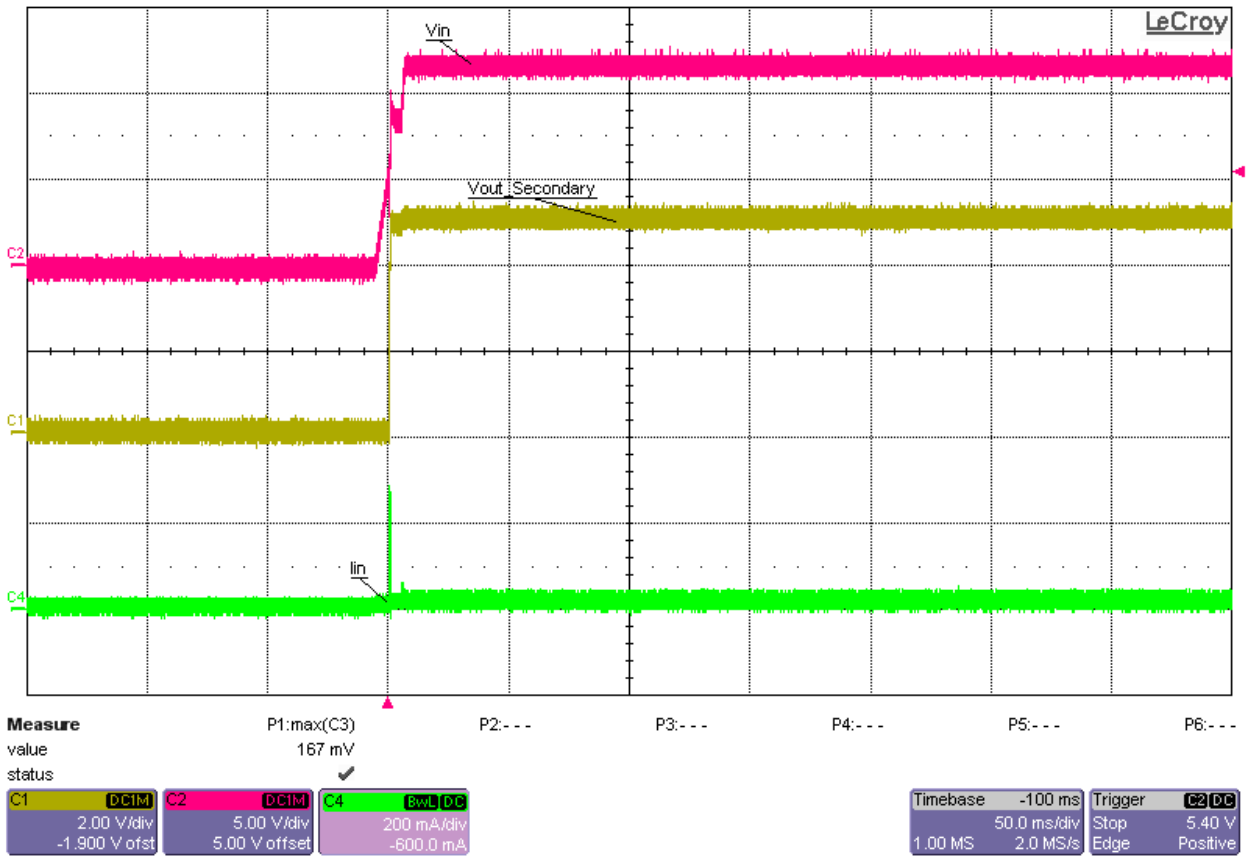
6.2 Startup



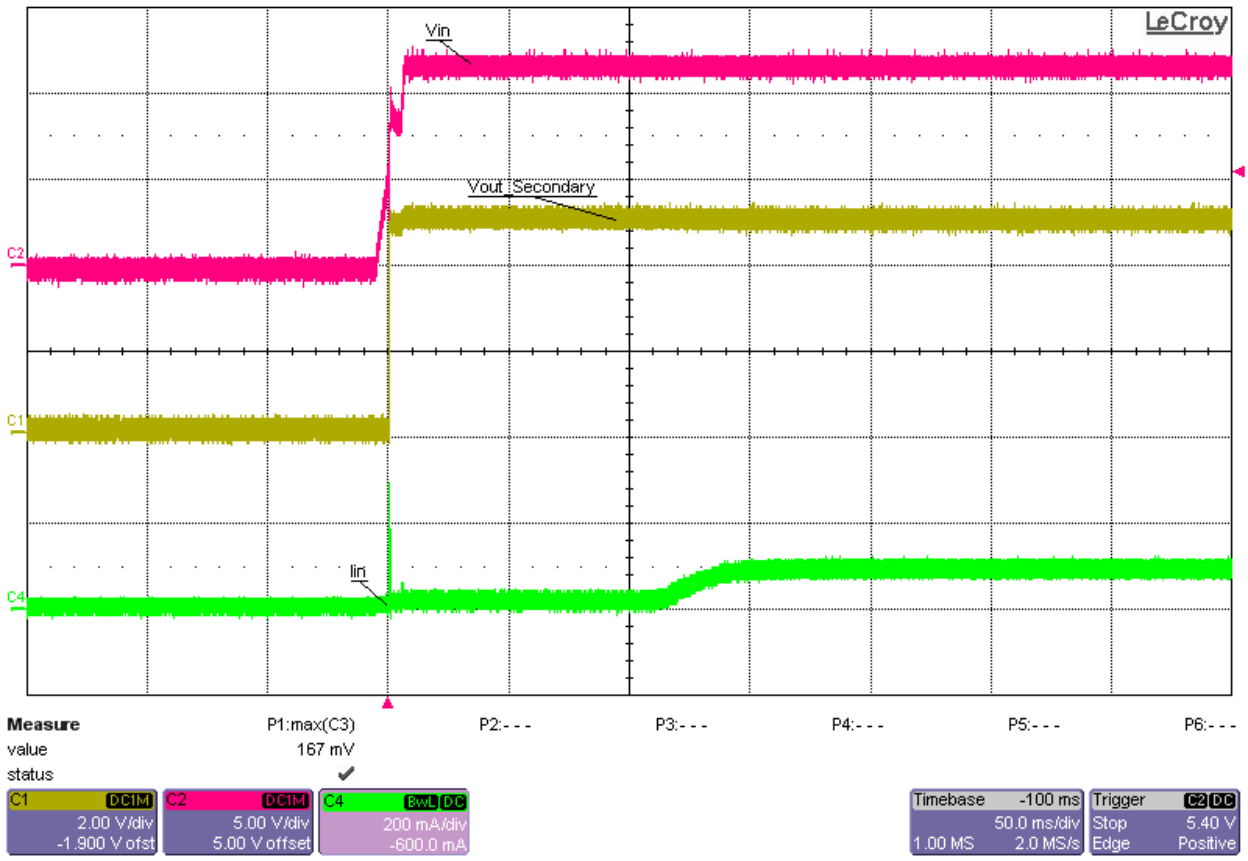
Startup into No Load at 10.8Vin



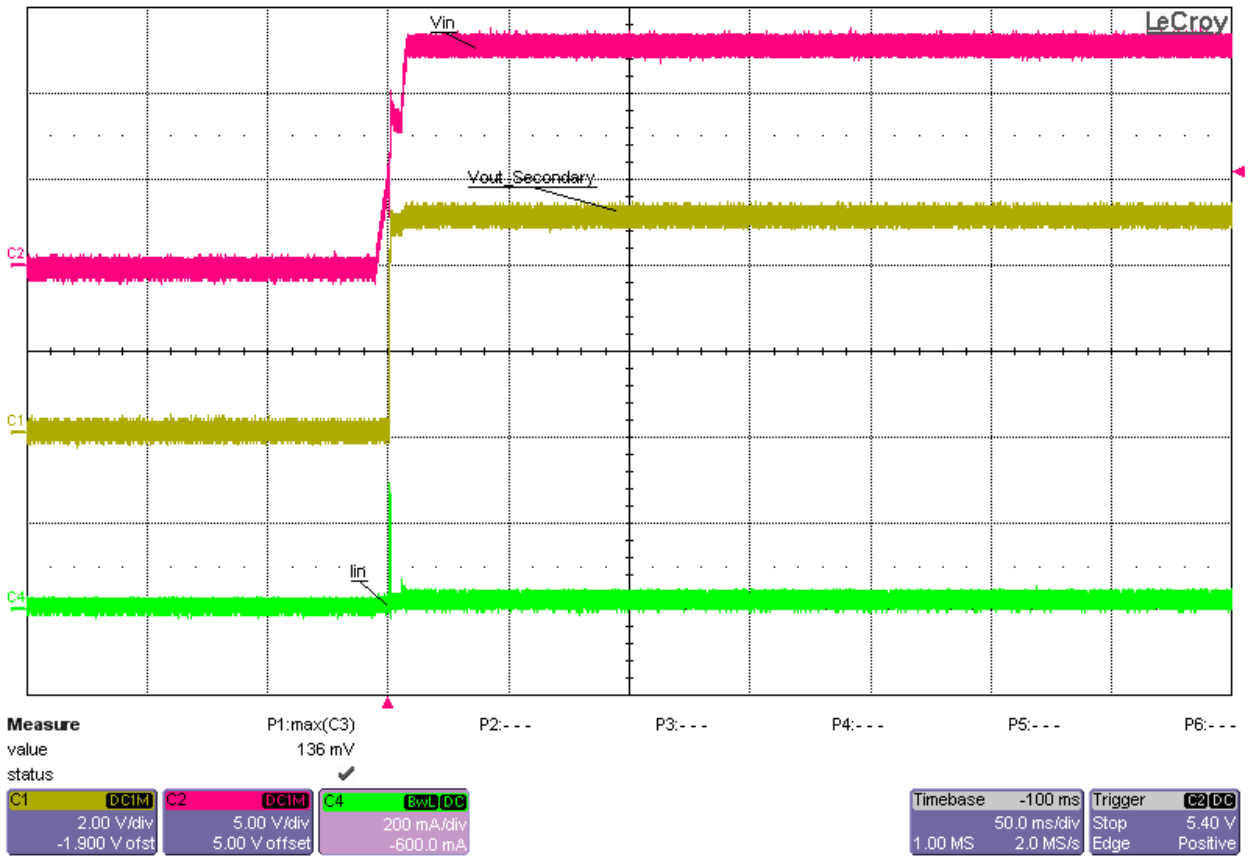
Startup into Full (300mA) Resistive Load at 10.8Vin



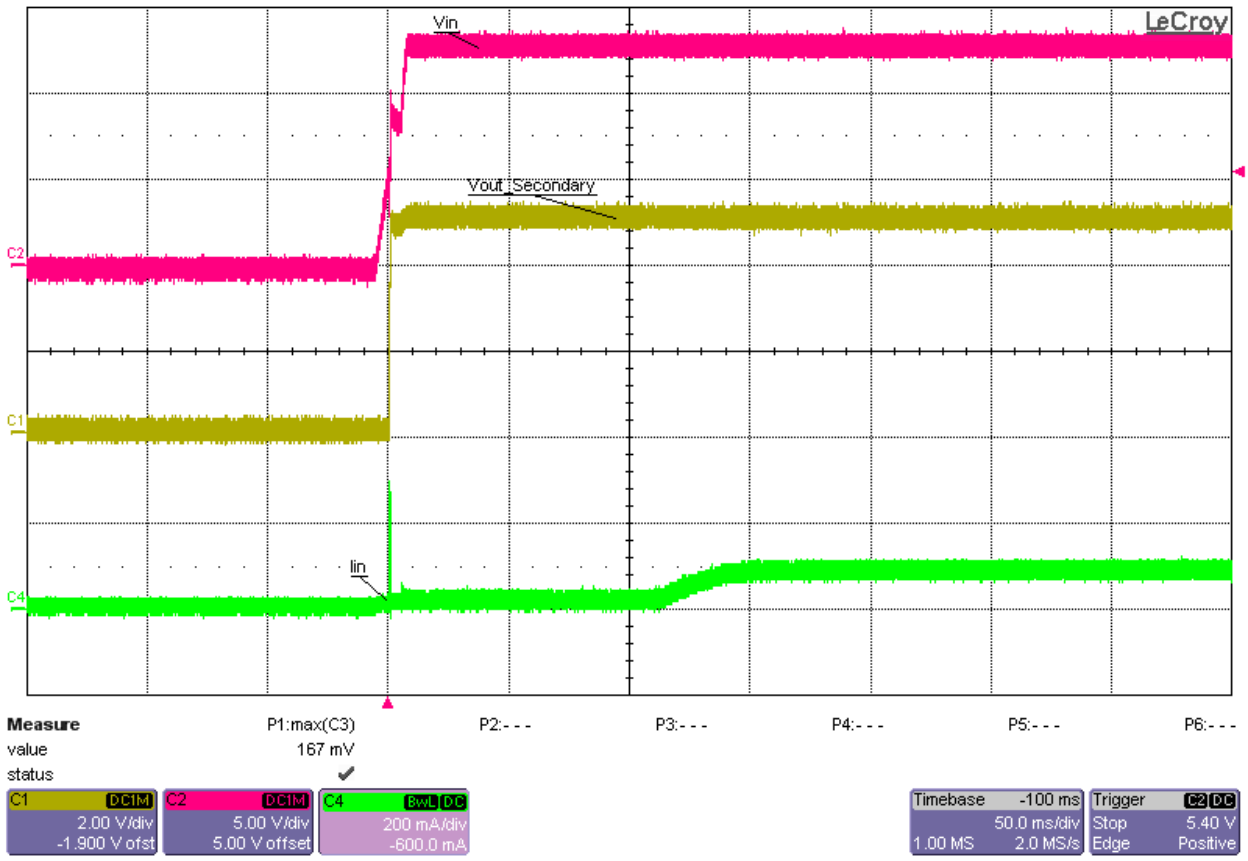
Startup into No Load at 12Vin



Startup into Full (300mA) Resistive Load at 12Vin

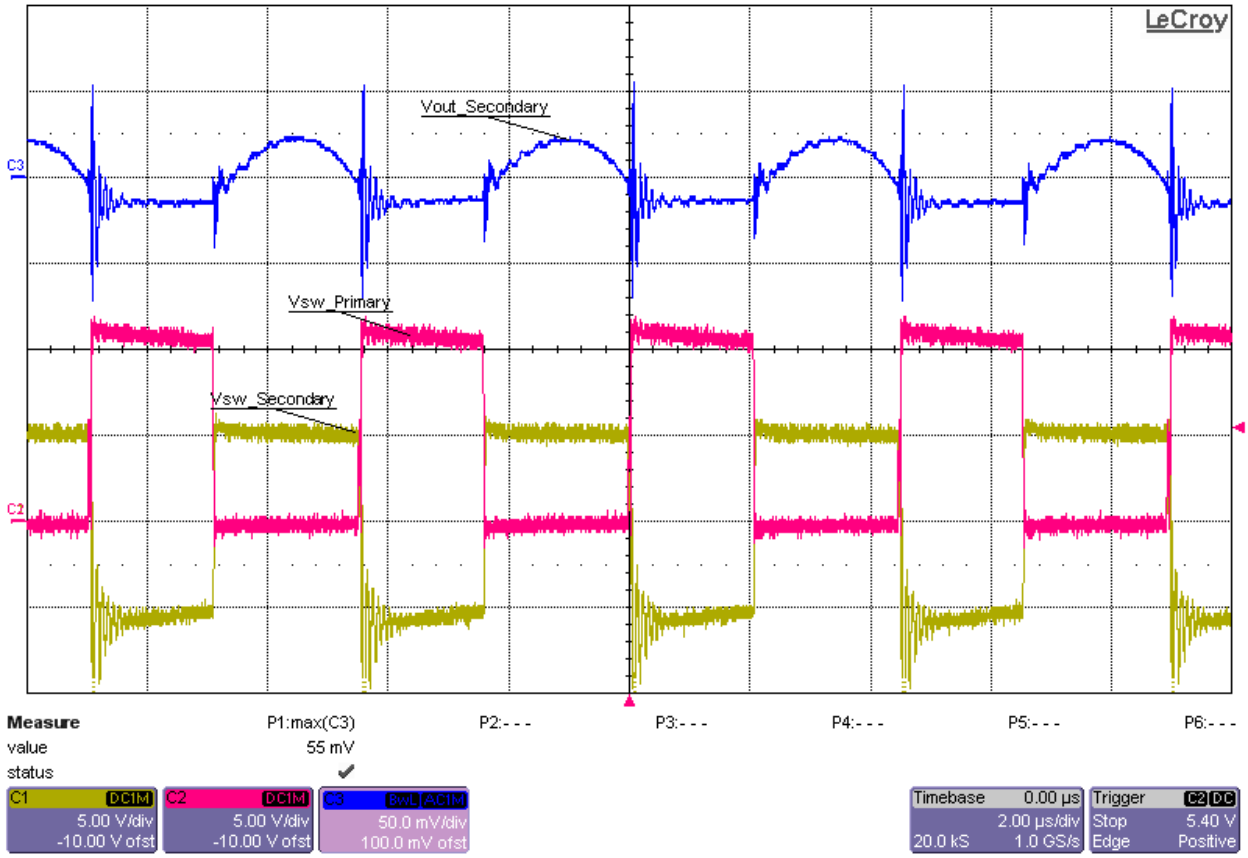


Startup into No Load at 13.2Vin

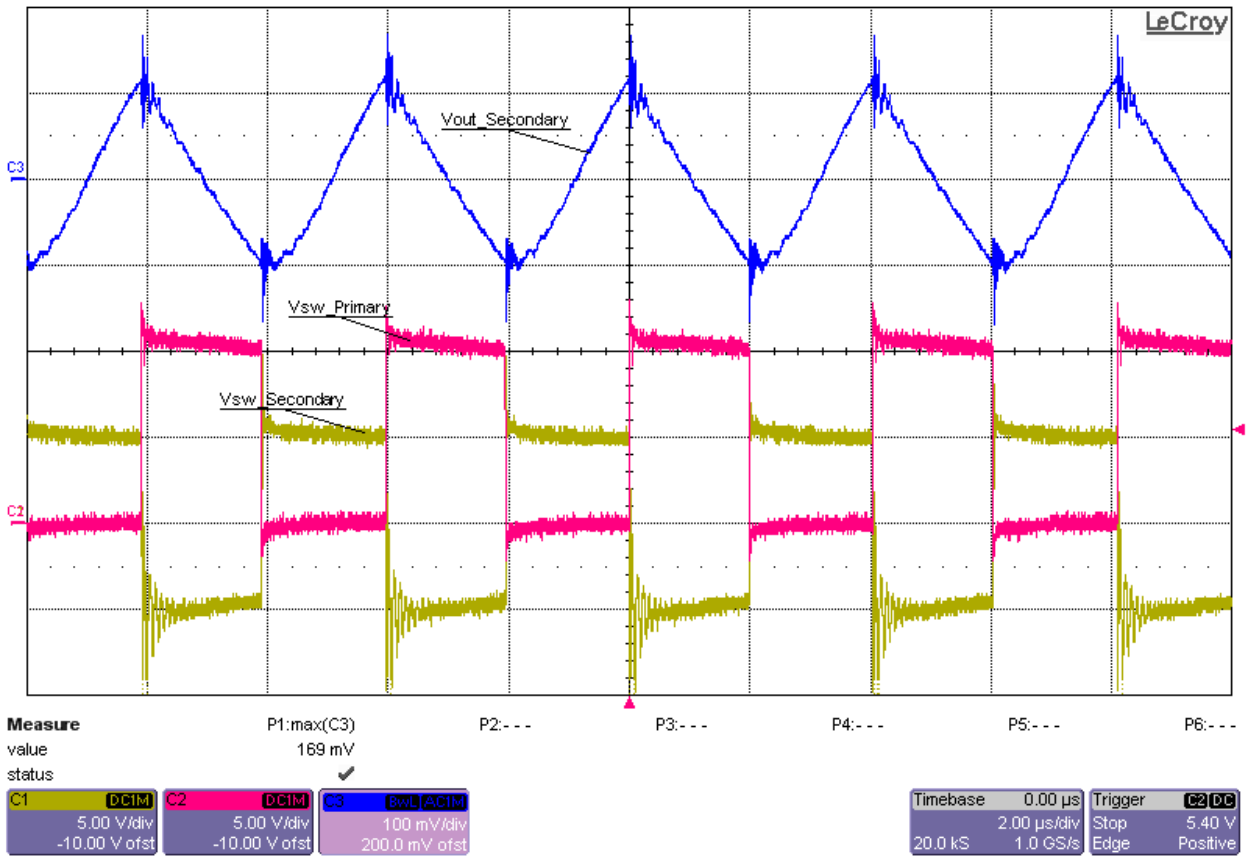


Startup into Full (300mA) Resistive Load at 13.2Vin

6.3 Output Voltage Ripple and Switch Node Voltage

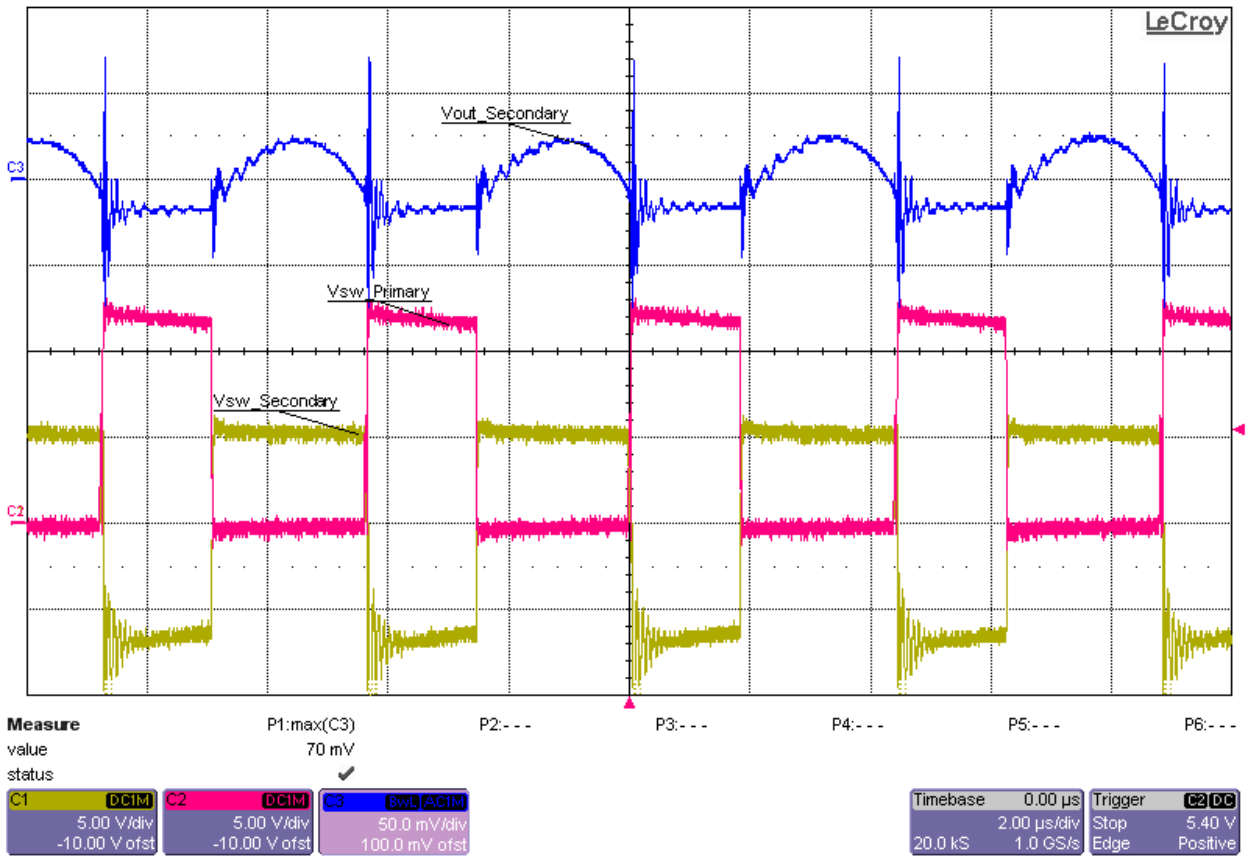


Switch Node and Secondary-Side Output Voltage Ripple at 10.8Vin and No Load (Vripple ≈ 43mVp-p)

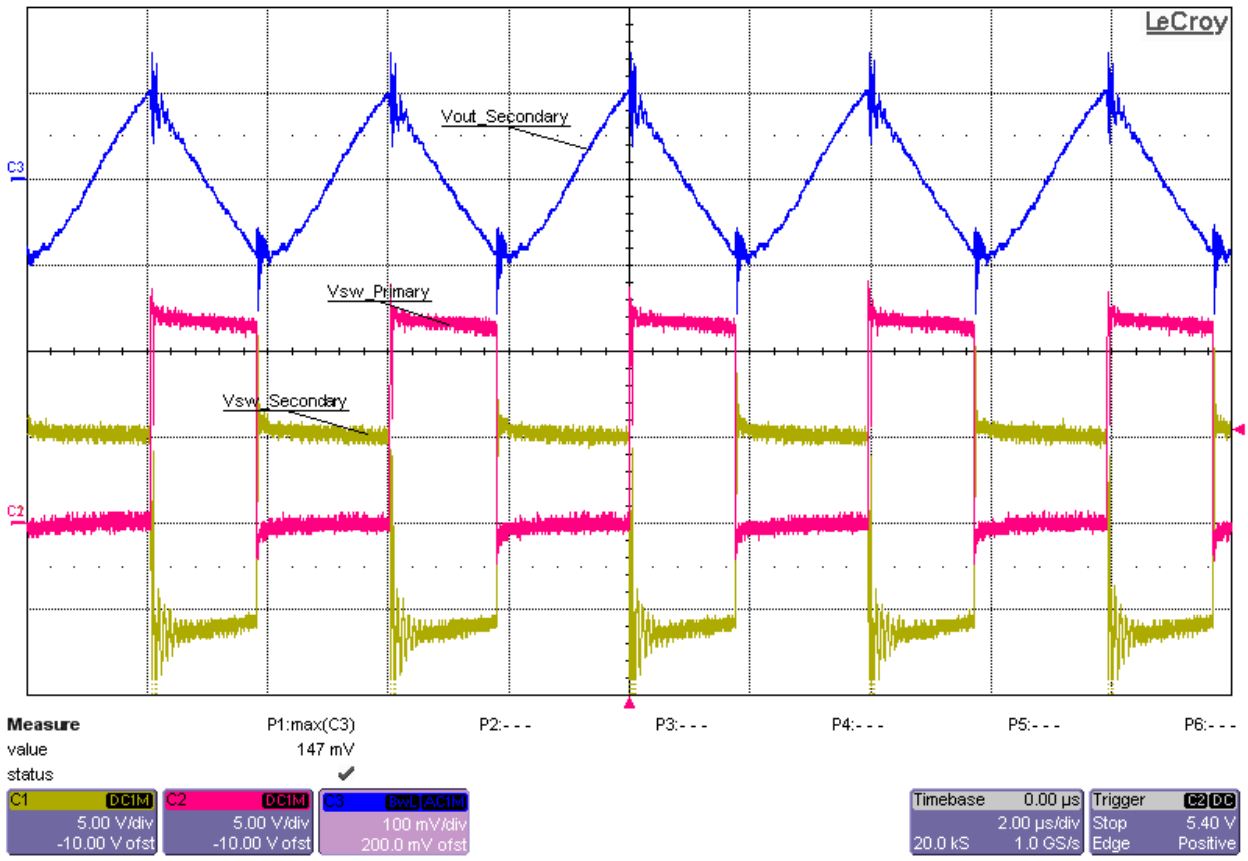


Switch Node and Secondary-Side Output Voltage Ripple at 10.8Vin and Full (300mA) Load

(Vripple ≈ 230mVp-p)

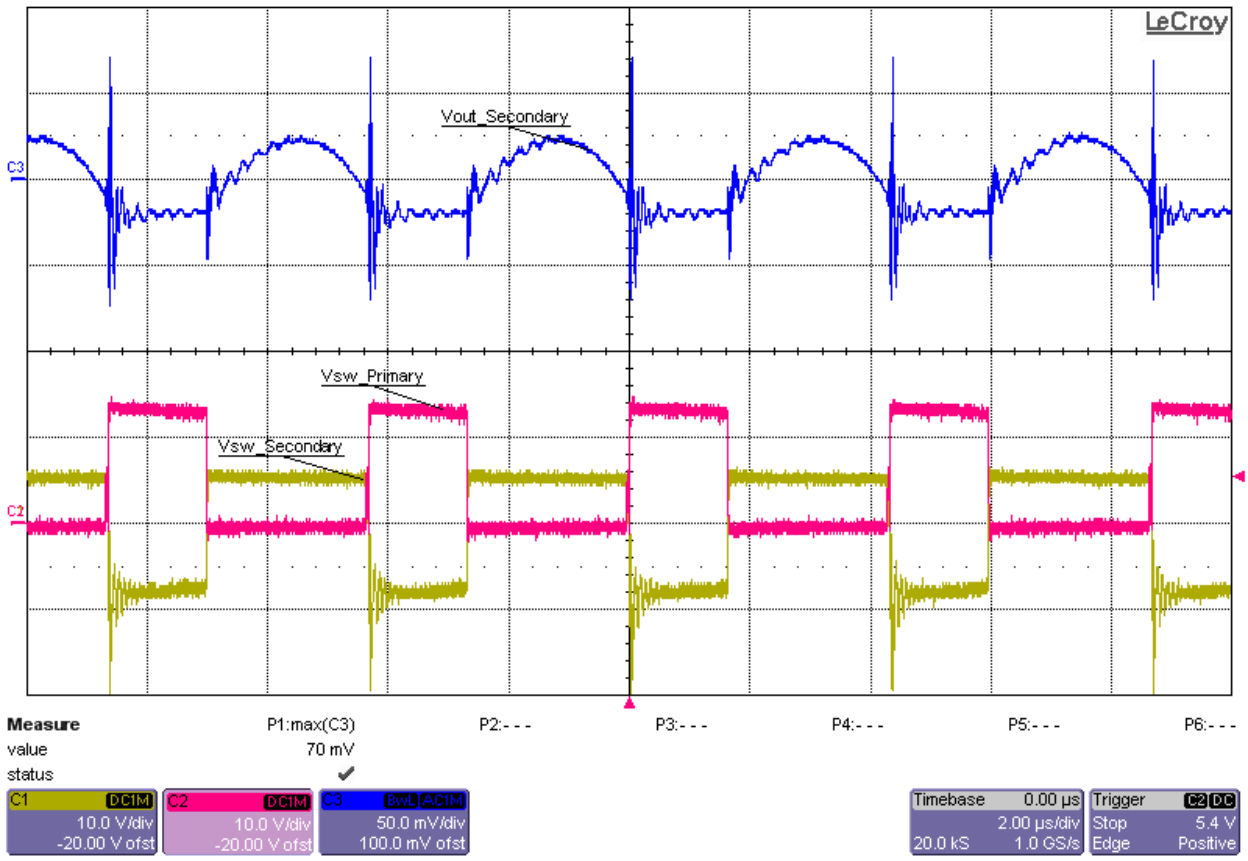


Switch Node and Secondary-Side Output Voltage Ripple at 12Vin and No Load (Vripple ≈ 45mVp-p)

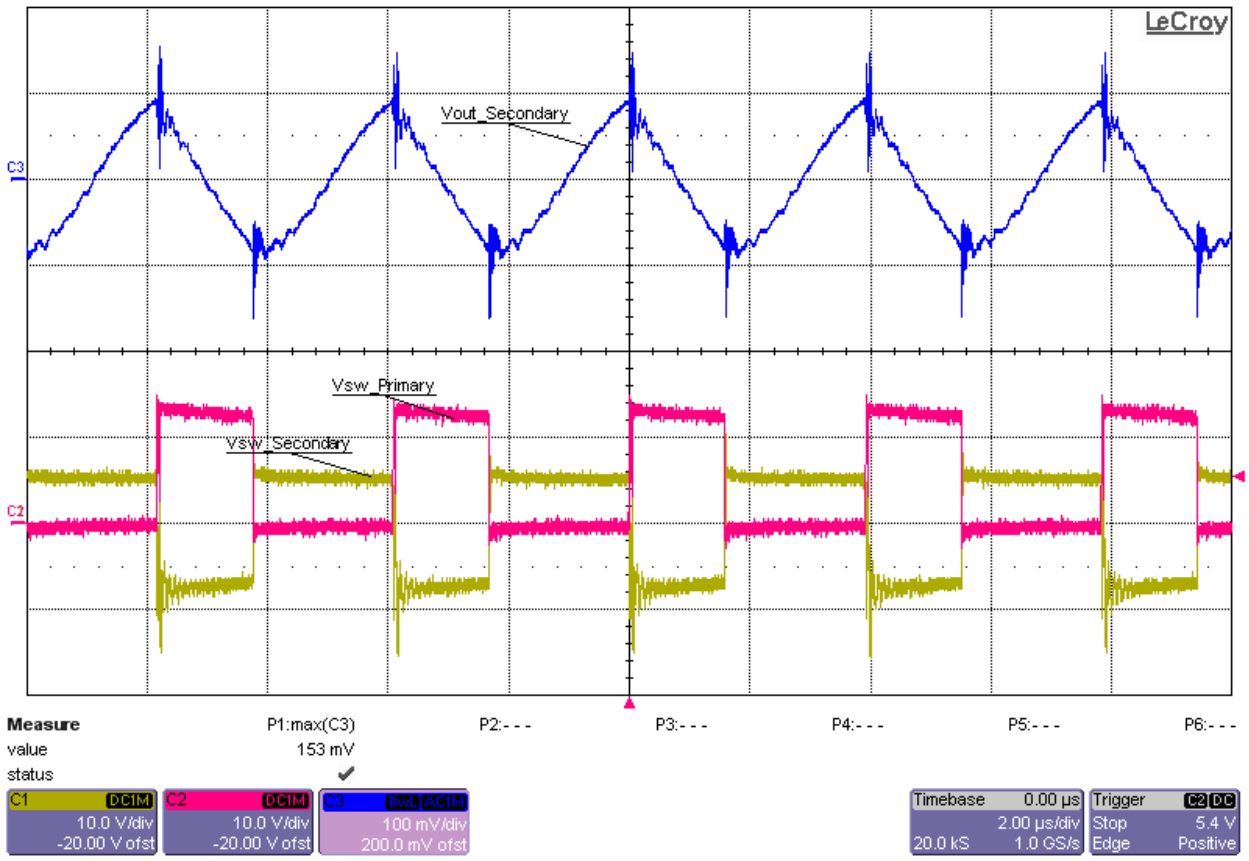


Switch Node and Secondary-Side Output Voltage Ripple at 12Vin and Full (300mA) Load

(Vripple ≈ 200mVp-p)



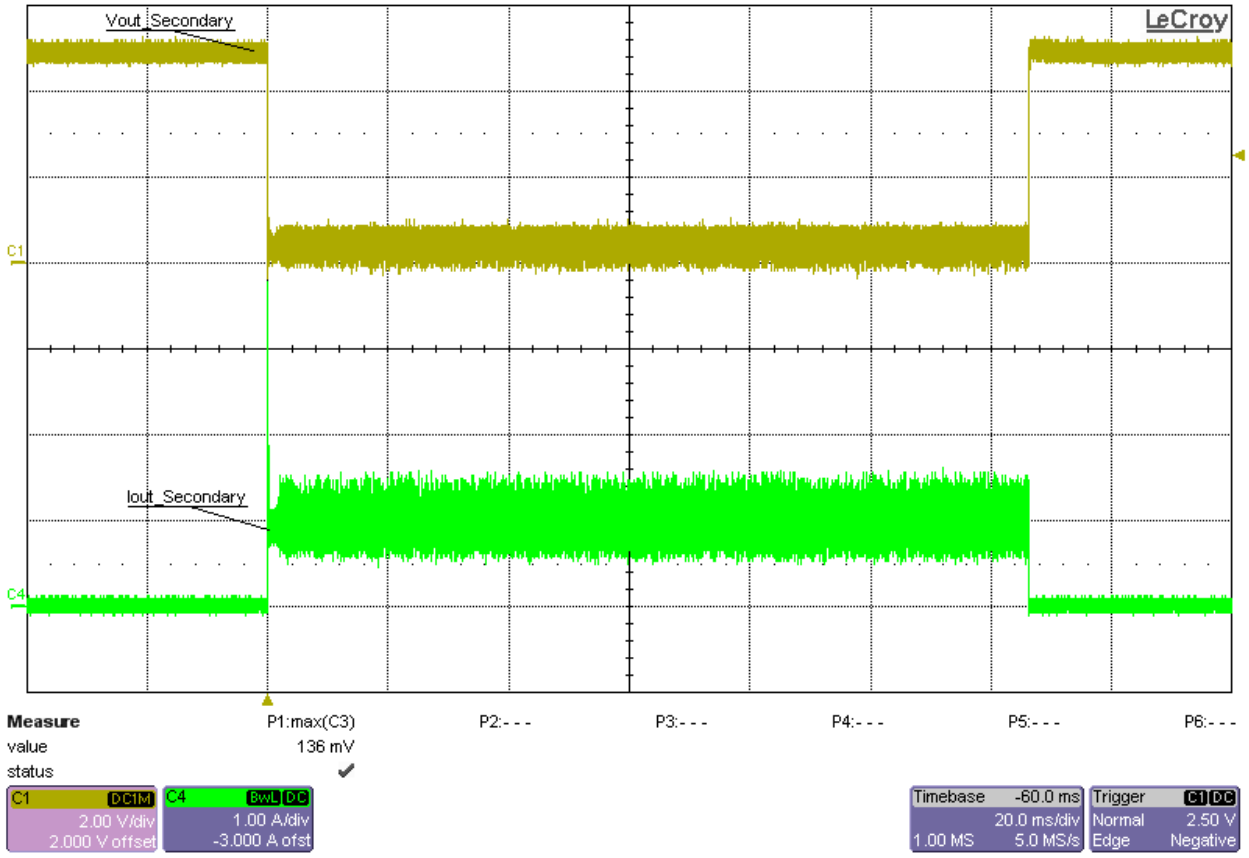
Switch Node and Secondary-Side Output Voltage Ripple at 13.2Vin and No Load (Vripple ≈ 65mVp-p)



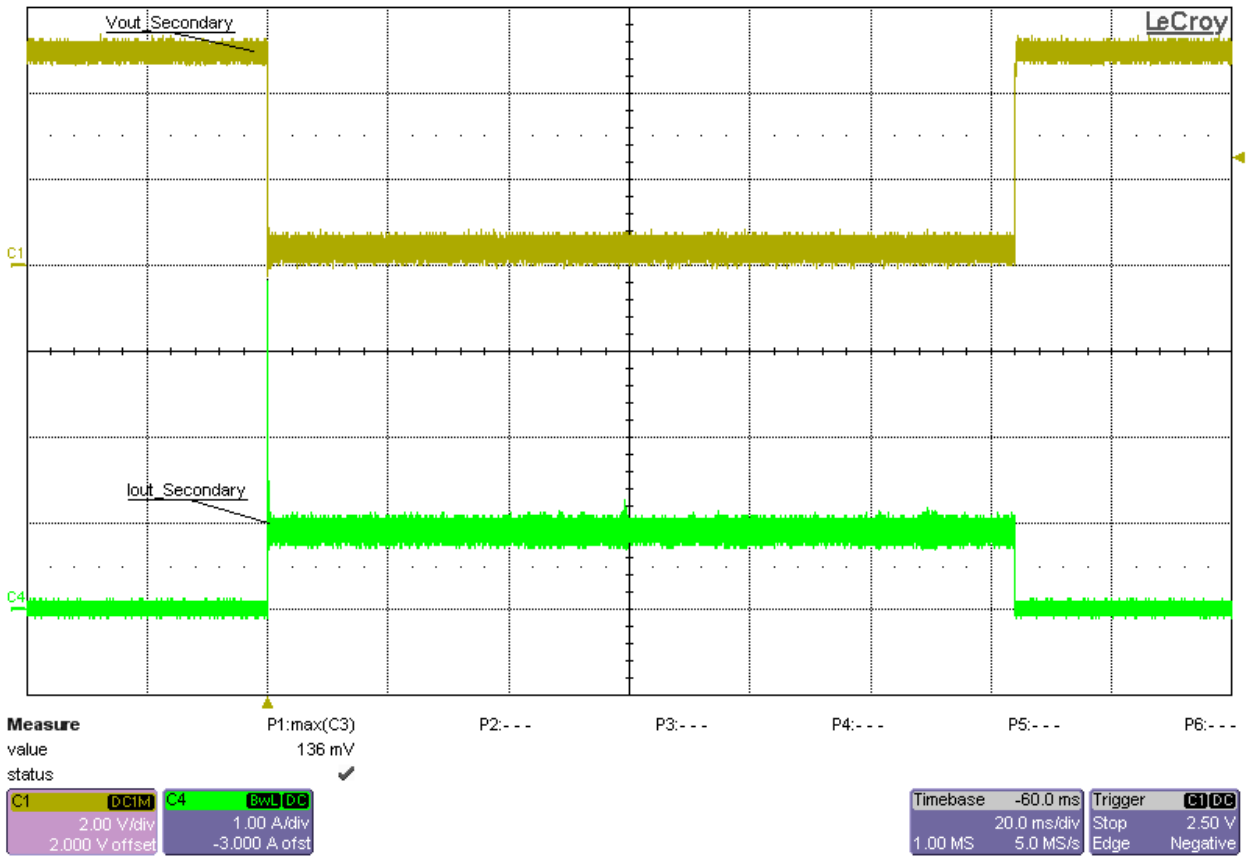
Switch Node and Secondary-Side Output Voltage Ripple at 13.2Vin and Full (300mA) Load

(Vripple ≈ 180mVp-p)

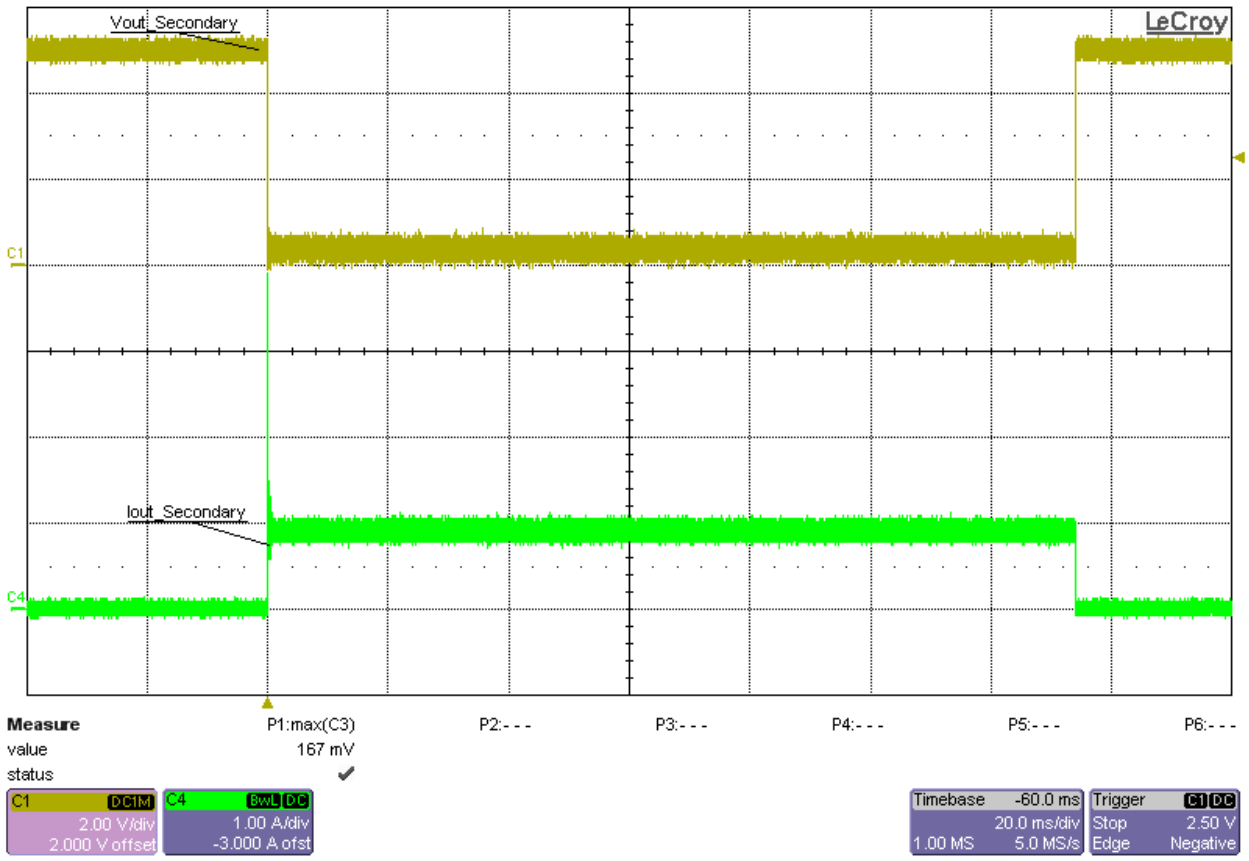
7 Short Circuit Testing



Short Circuit Application and Recovery at 10.8Vin (applied from no load, recovered into no load)



Short Circuit Application and Recovery at 12Vin (applied from no load, recovered into no load)



Short Circuit Application and Recovery at 13.2Vin (applied from no load, recovered into no load)

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